

***Short Course On Phase-Locked Loops
IEEE Circuit and System Society, San Diego, CA***

Digital Frequency Synthesizers

**Michael H. Perrott
September 16, 2009**

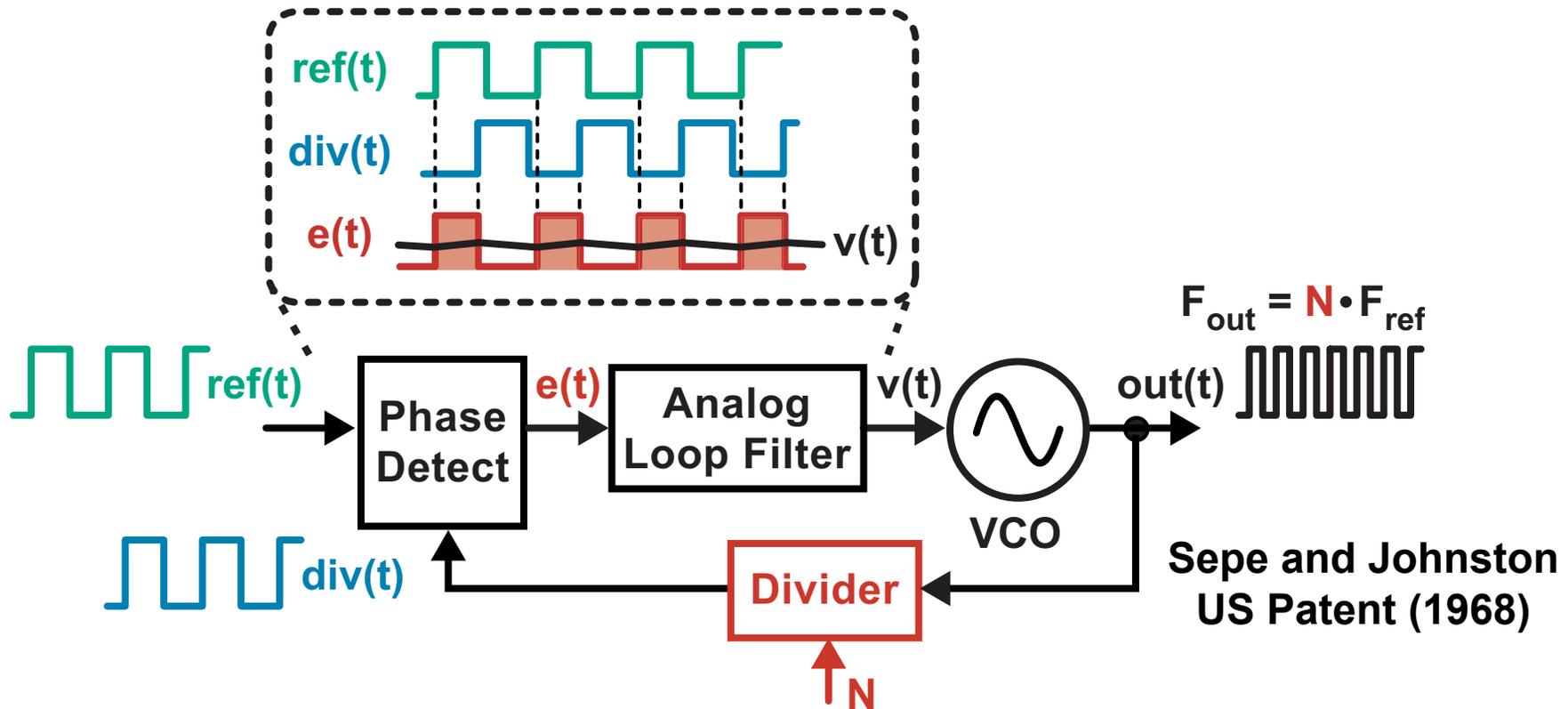
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Why Are Digital Phase-Locked Loops Interesting?

- **Performance is important**
 - Phase noise can limit wireless transceiver performance
 - Jitter can be a problem for digital processors
- **The standard analog PLL implementation is problematic in many applications**
 - Analog building blocks on a mostly digital chip pose design and verification challenges
 - The cost of implementation is becoming too high ...

Can digital phase-locked loops offer excellent performance with a lower cost of implementation?

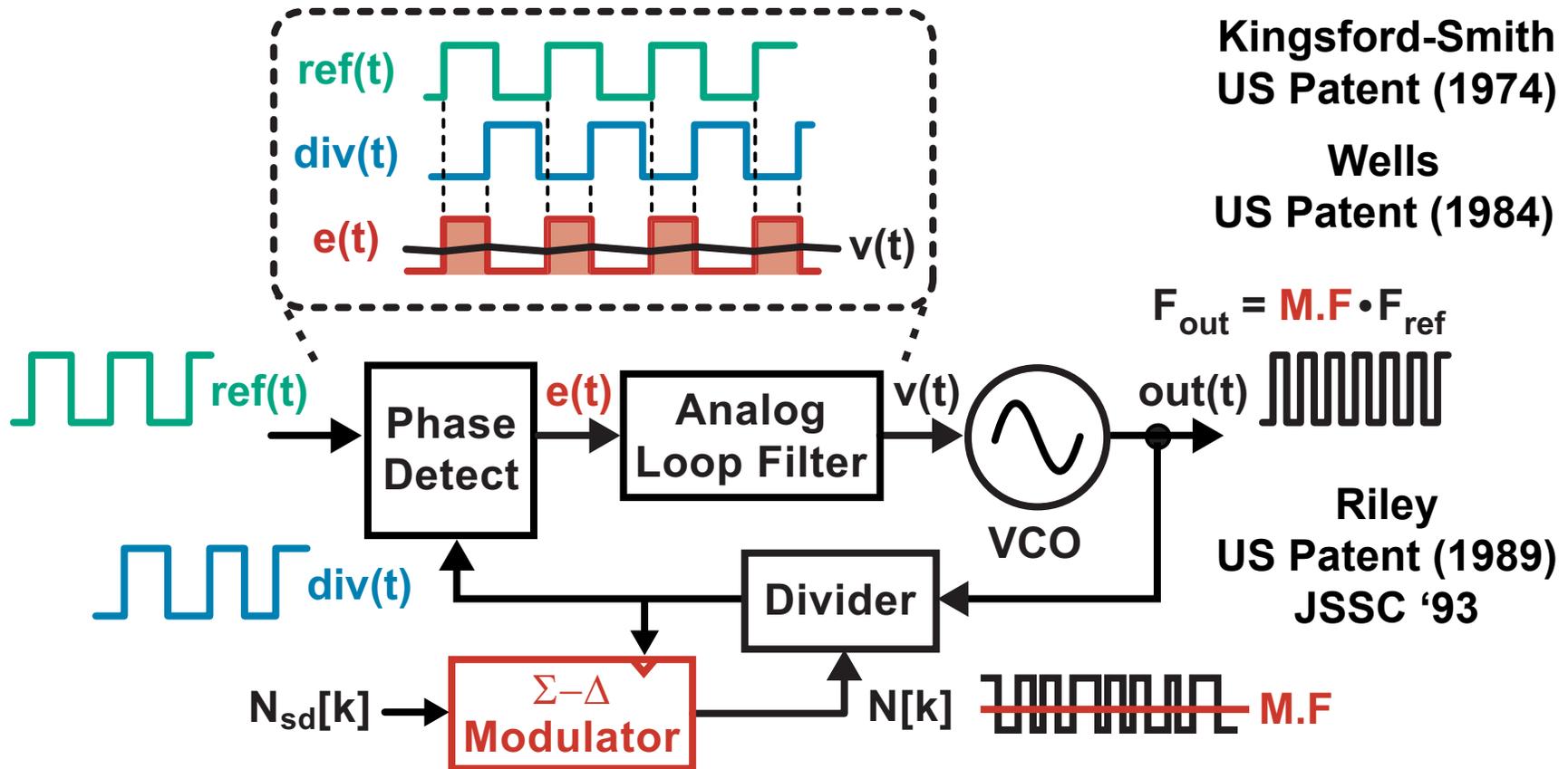
Integer-N Frequency Synthesizers



- Use digital counter structure to divide VCO frequency
 - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

Tradeoff: Resolution vs PLL Bandwidth

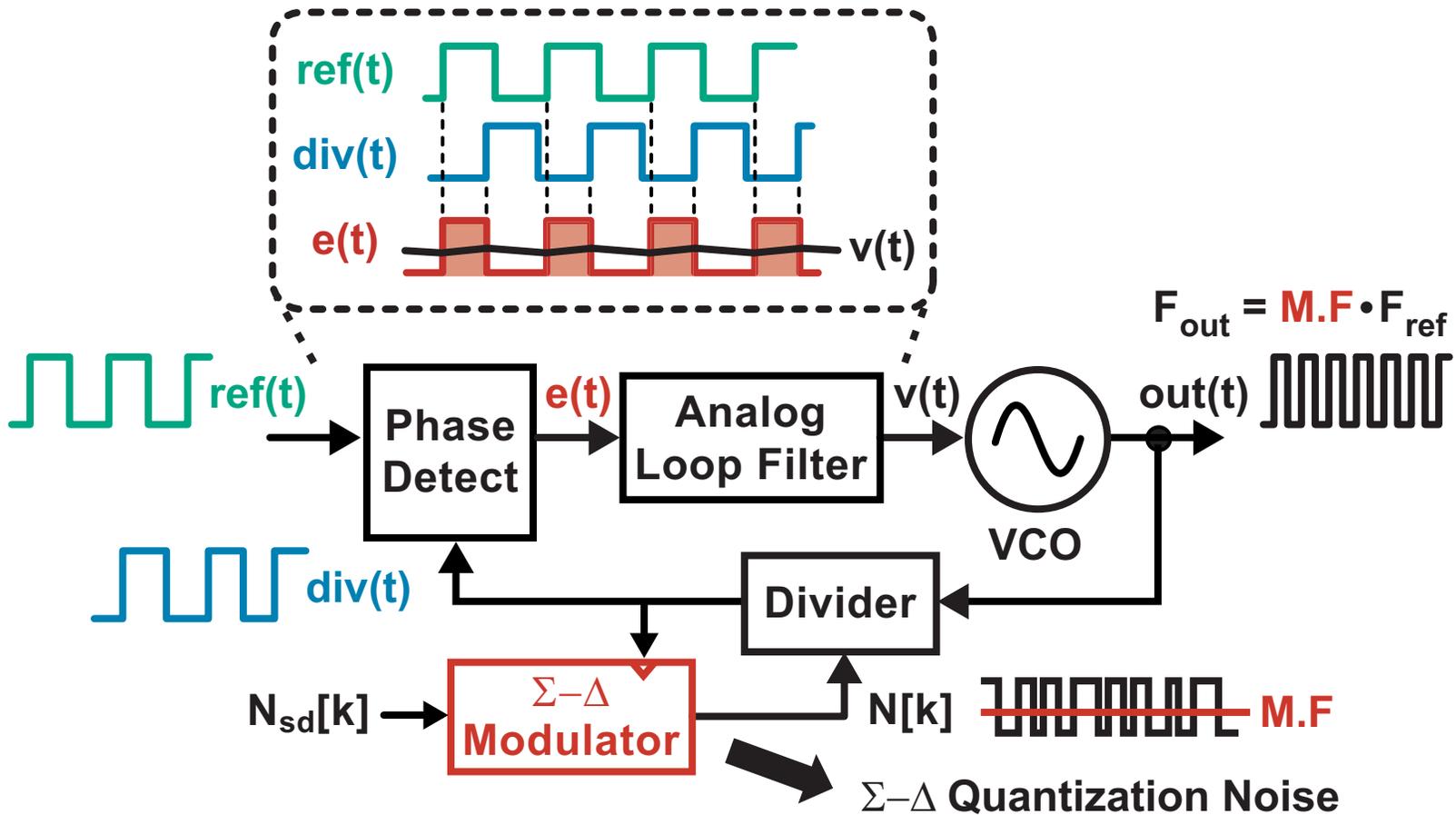
Fractional-N Frequency Synthesizers



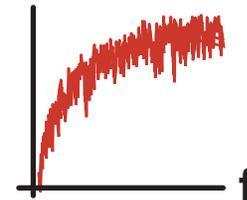
- Dither divide value to achieve fractional divide values
 - PLL loop filter smooths the resulting variations

Tradeoff: Noise versus PLL Bandwidth

The Issue of Quantization Noise

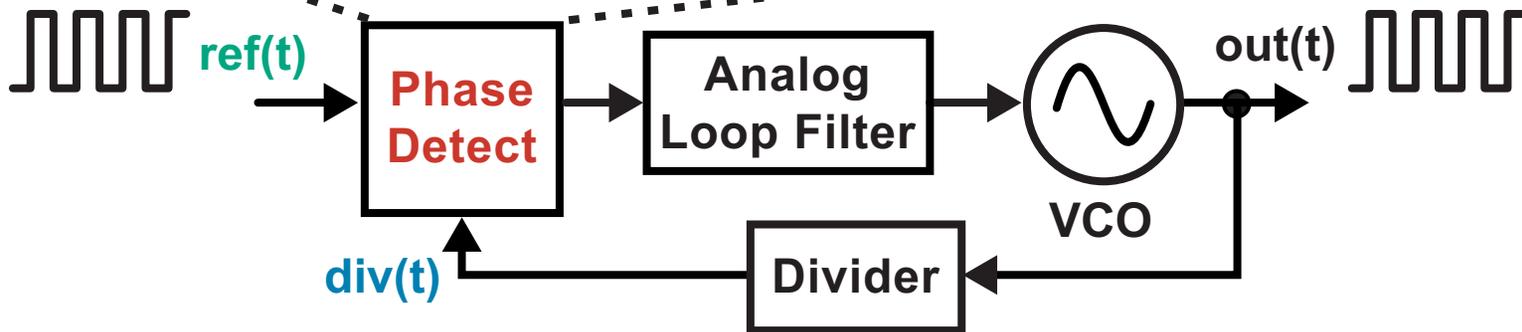
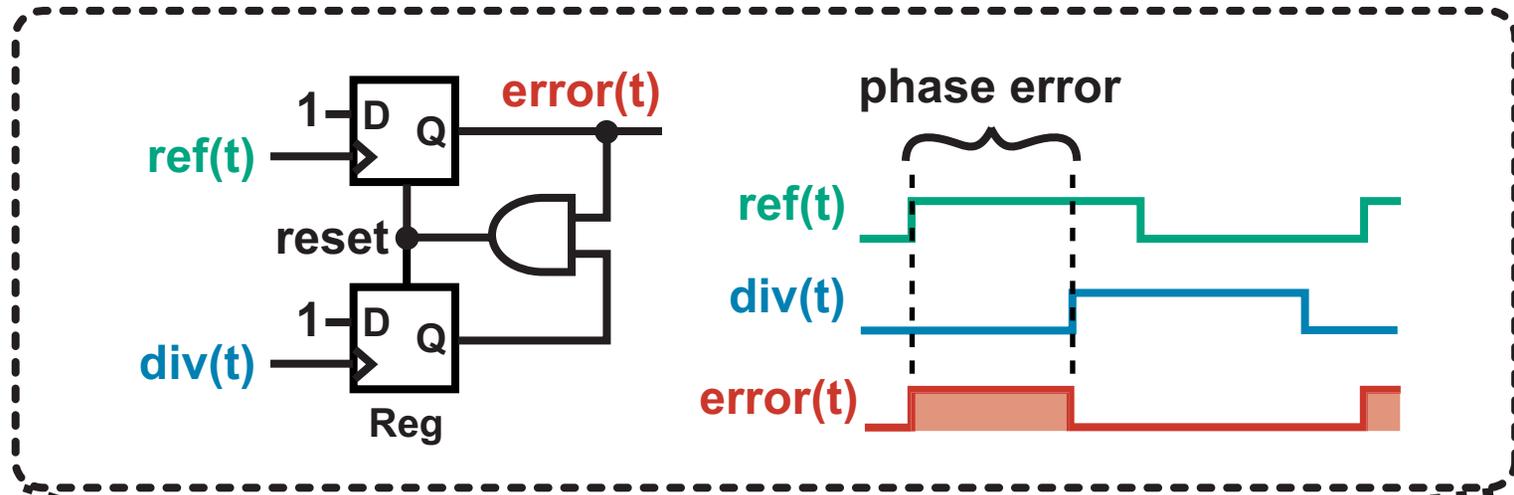


- Limits PLL bandwidth
- Increases linearity requirements of phase detector



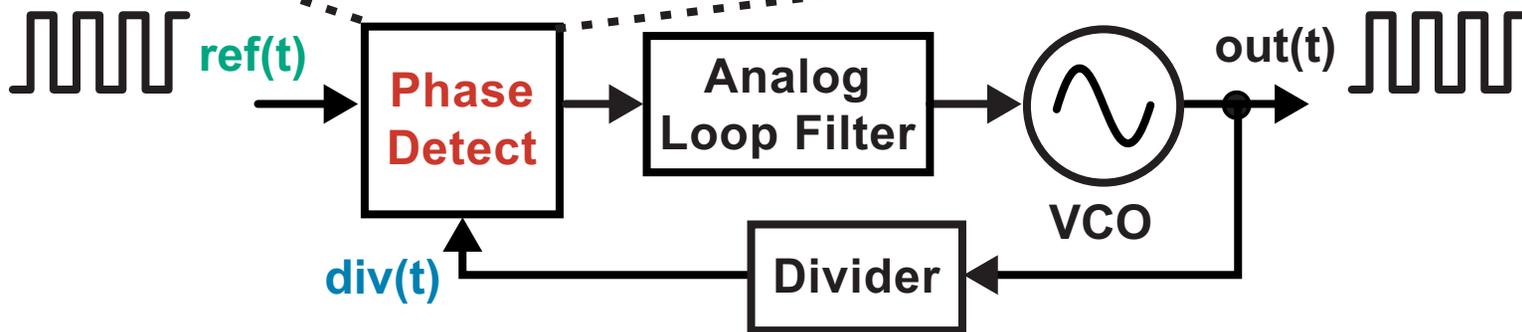
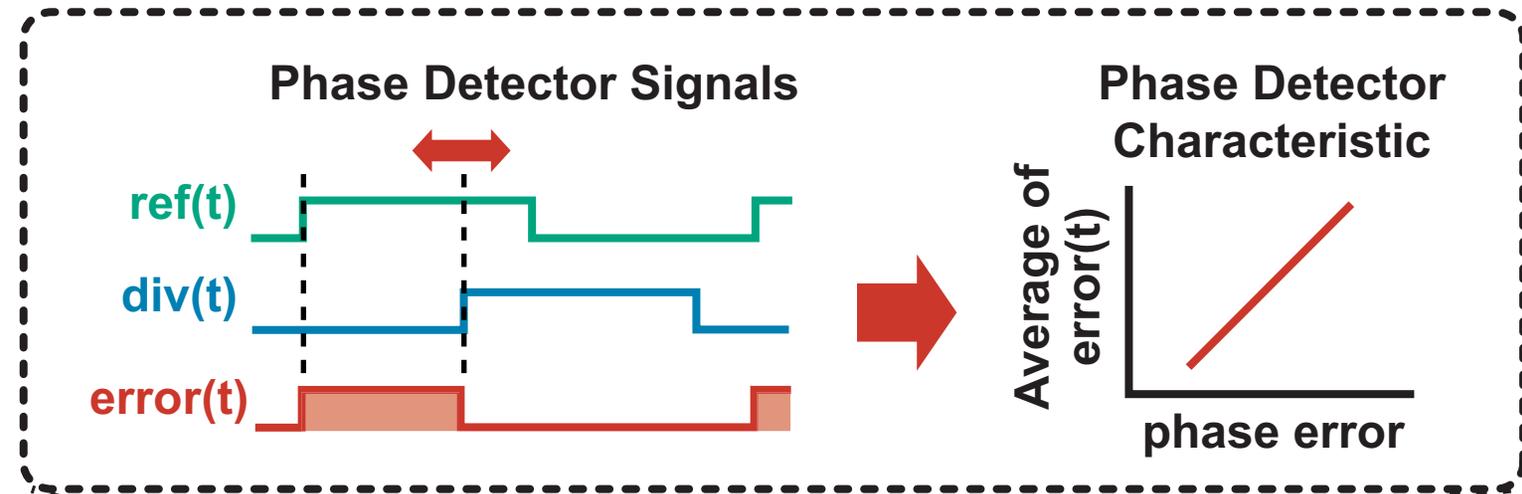
Striving for a Better PLL Implementation

Analog Phase Detection



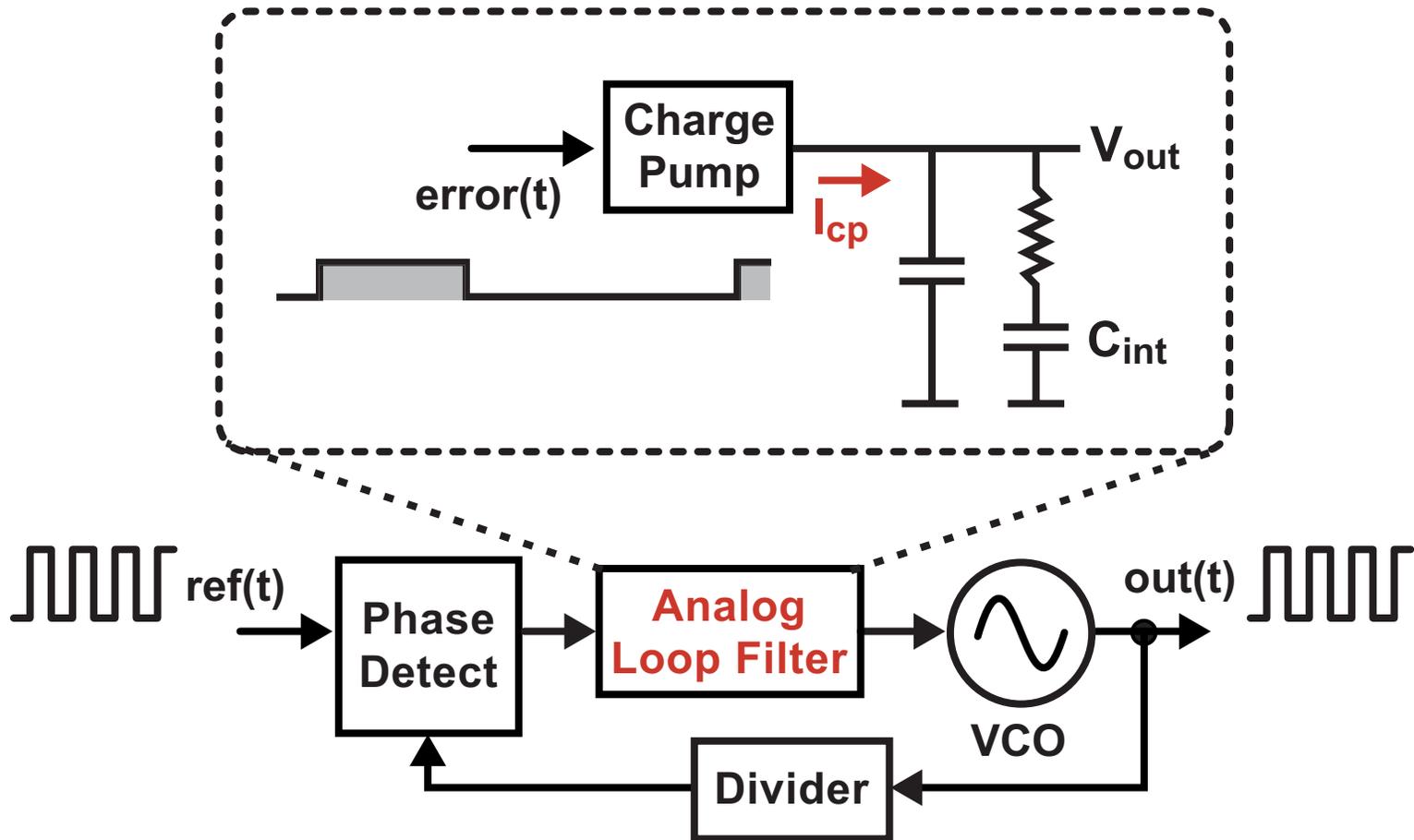
- Pulse width is formed according to phase difference between two signals
- Average of pulsed waveform is applied to VCO input

Tradeoffs of Analog Approach



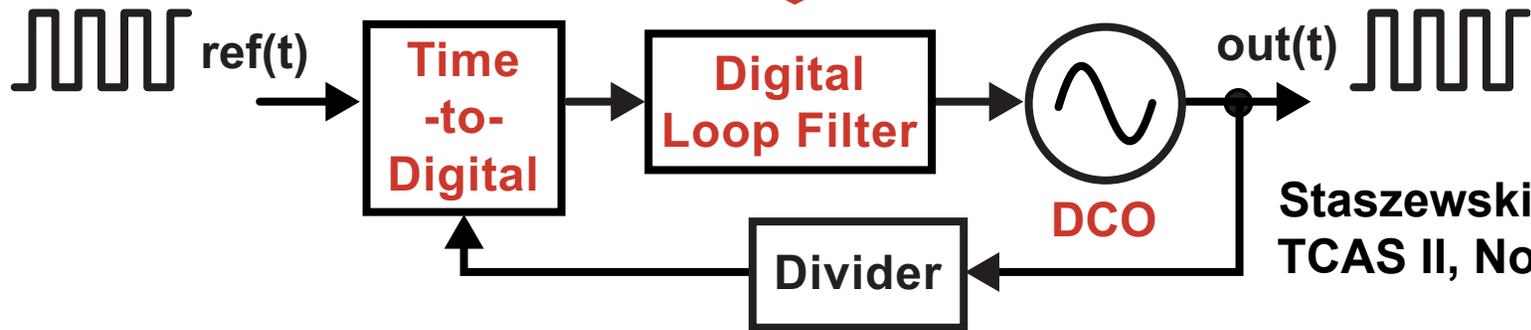
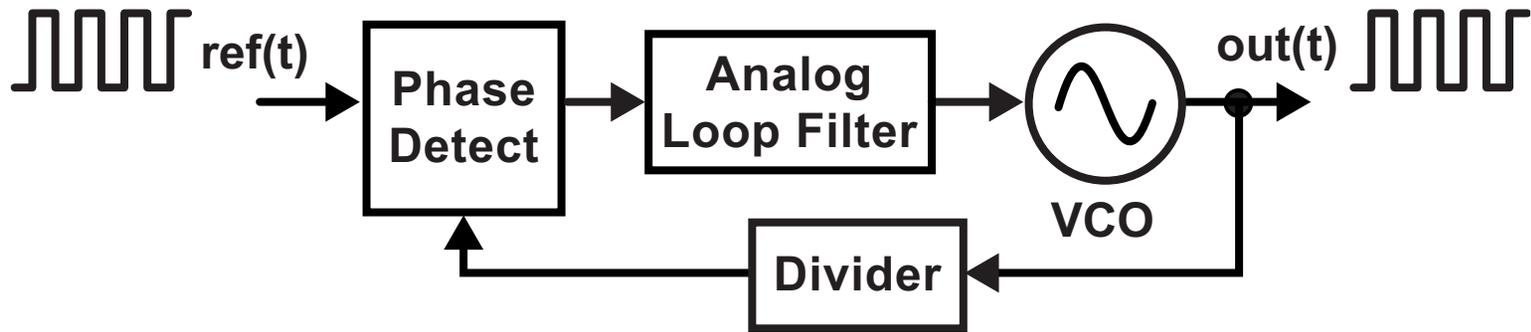
- **Benefit:** average of pulsed output is a continuous, linear function of phase error
- **Issue:** analog loop filter implementation is undesirable

Issues with Analog Loop Filter



- Charge pump: output resistance, mismatch
- Filter caps: leakage current, *large area*

Going Digital ...



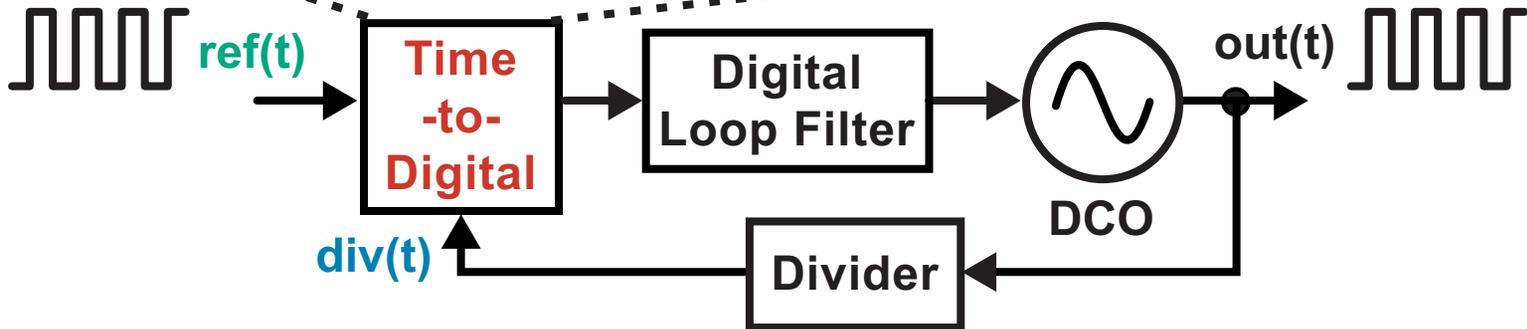
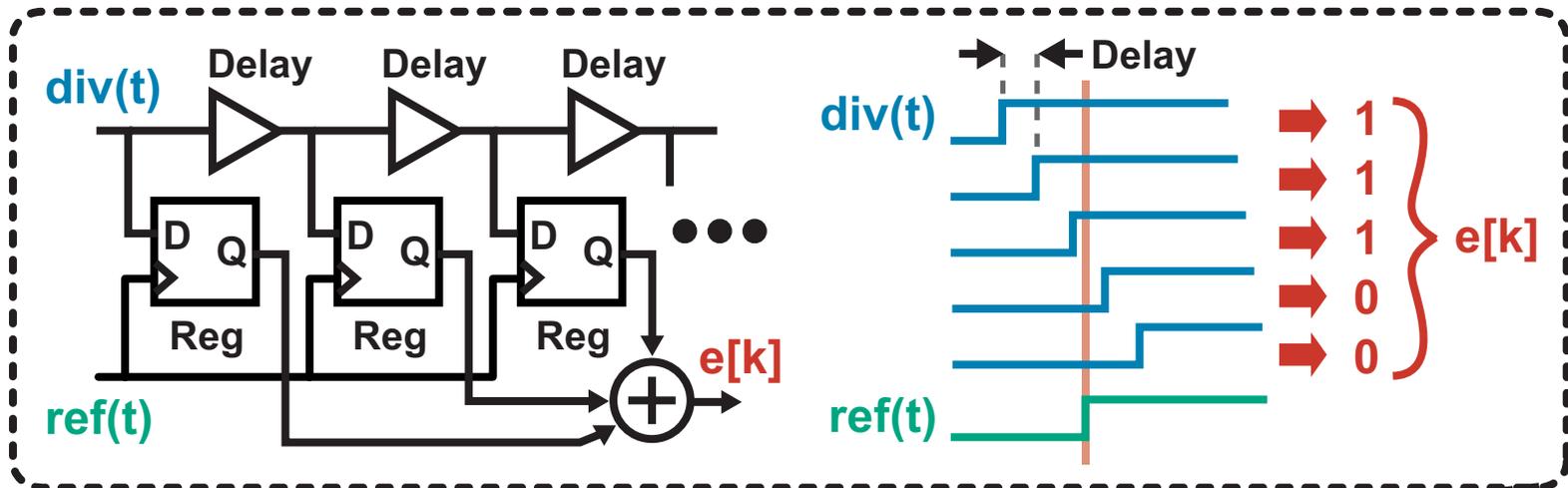
Staszewski et. al.,
TCAS II, Nov 2003

- Digital loop filter: compact area, insensitive to leakage
- Challenges:
 - Time-to-Digital Converter (TDC)
 - Digitally-Controlled Oscillator (DCO)

Outline of Talk

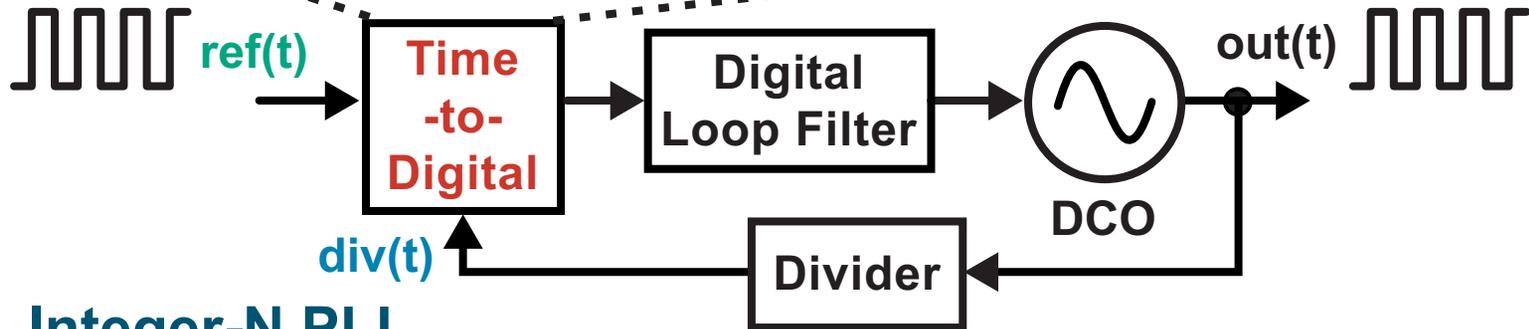
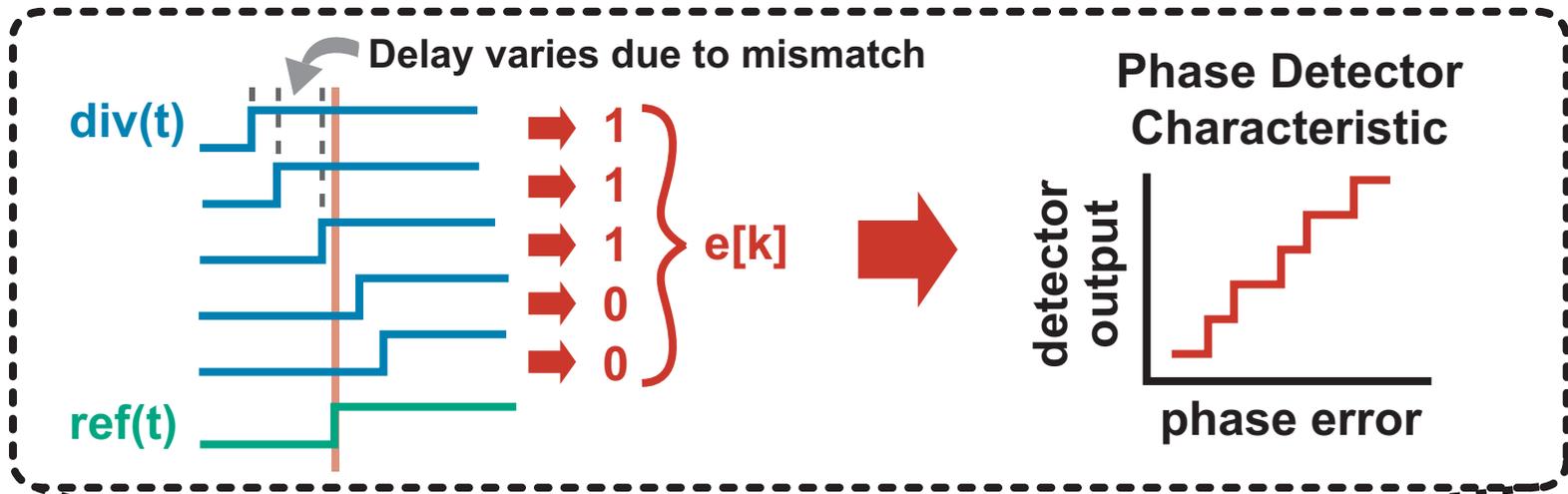
- **Overview of Key Blocks (TDC and DCO)**
- **Modeling & CAD Tools**
- **High Performance TDC design**
- **Quantization Noise Cancellation**
- **DCO based on an efficient passive DAC structure**
- **Divider Design**
- **Loop Filter Design**
- **Prototype with measured Results**

Classical Time-to-Digital Converter



- Resolution set by a “Single Delay Chain” structure
 - Phase error is measured with delays and registers
- Corresponds to a flash architecture

Impact of Limited Resolution and Delay Mismatch



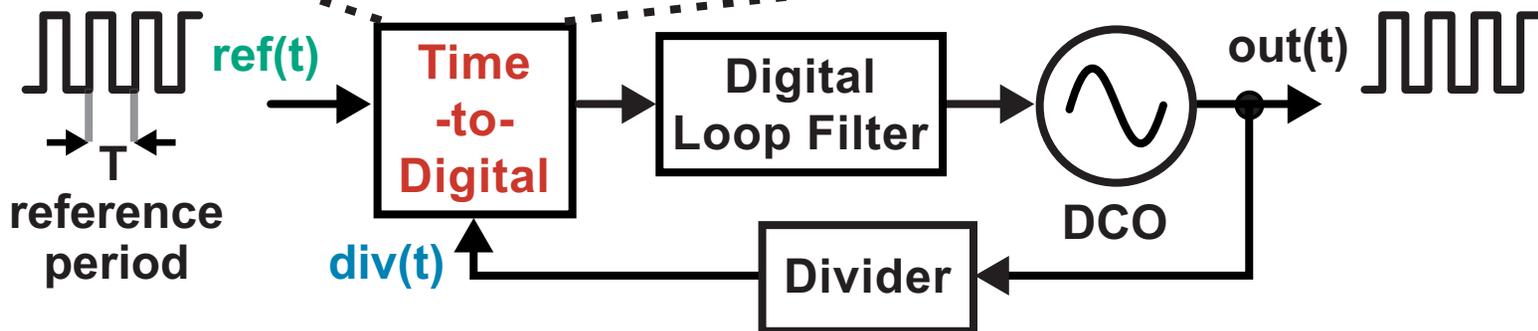
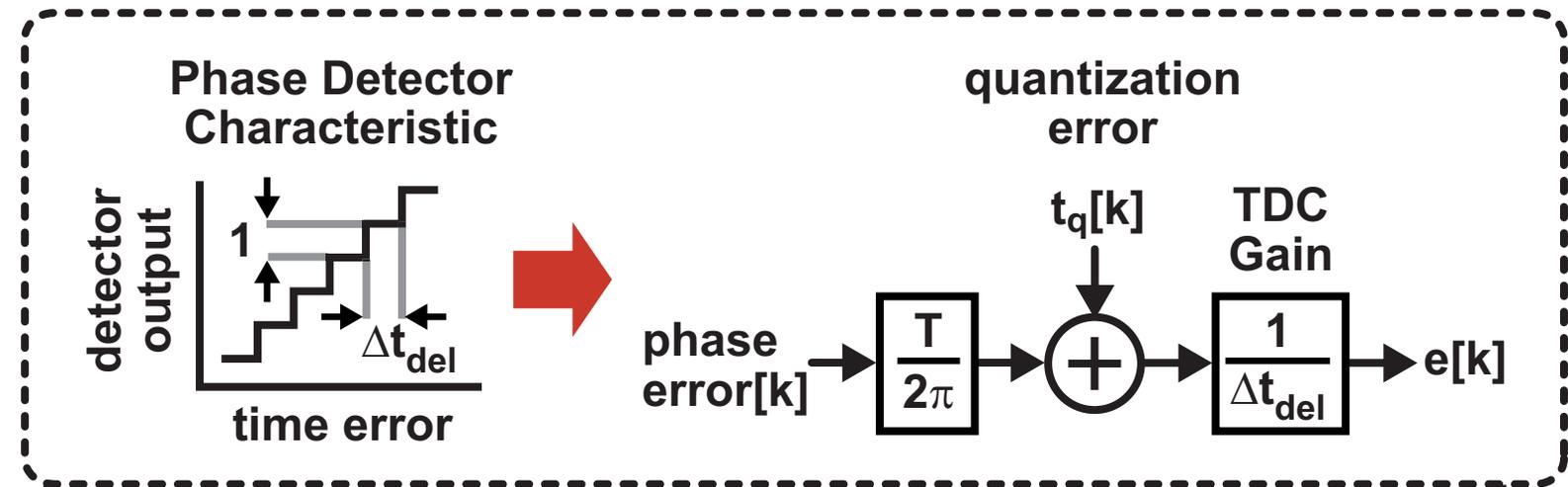
■ Integer-N PLL

- Limit cycles due to limited resolution (unless high ref noise)

■ Fractional-N PLL

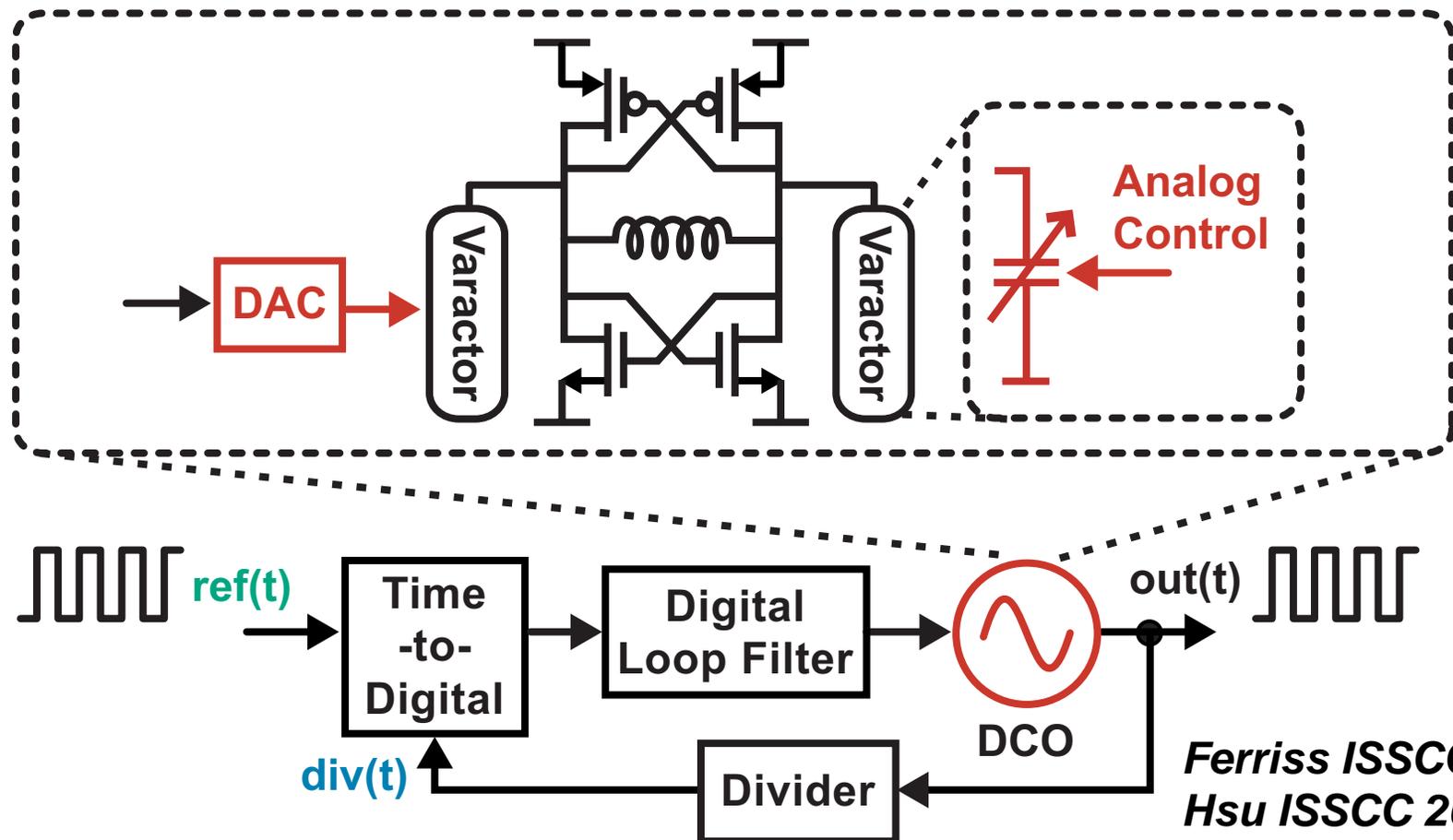
- Fractional spurs due to non-linearity from delay mismatch

Modeling of TDC



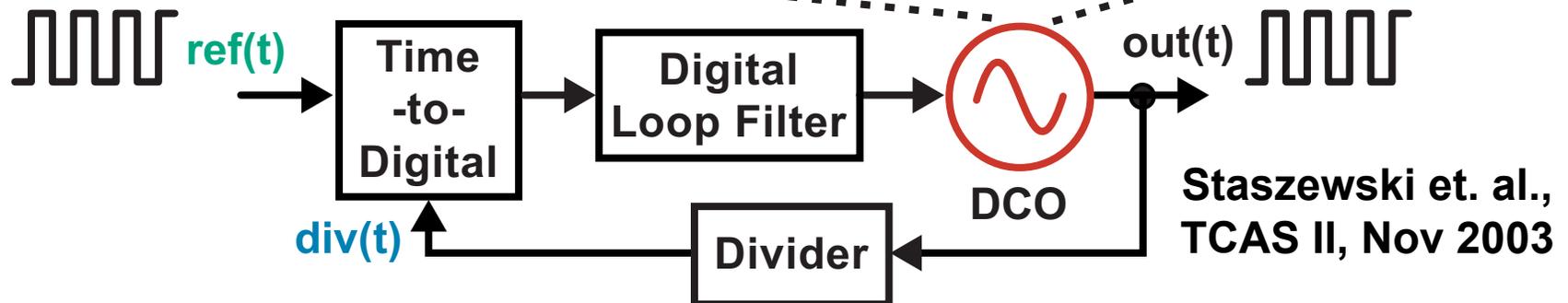
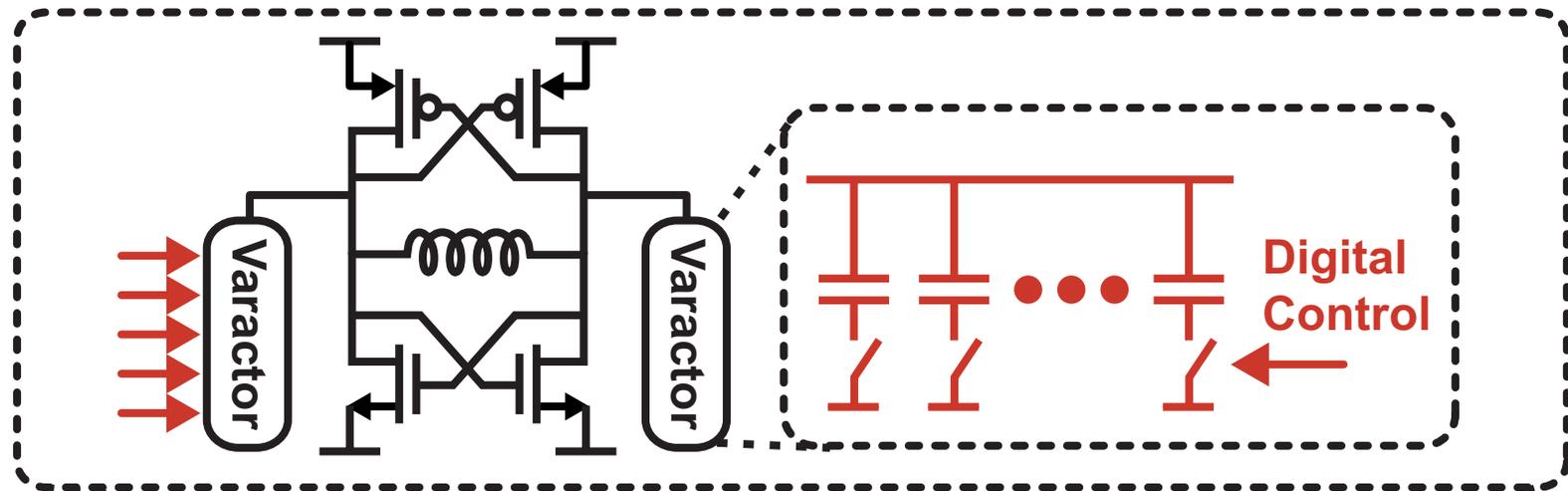
- Phase error converted to time error by scale factor: $T/2\pi$
- TDC introduces quantization error: $t_q[k]$
- TDC gain set by average delay per step: Δt_{del}

A Straightforward Approach for Achieving a DCO



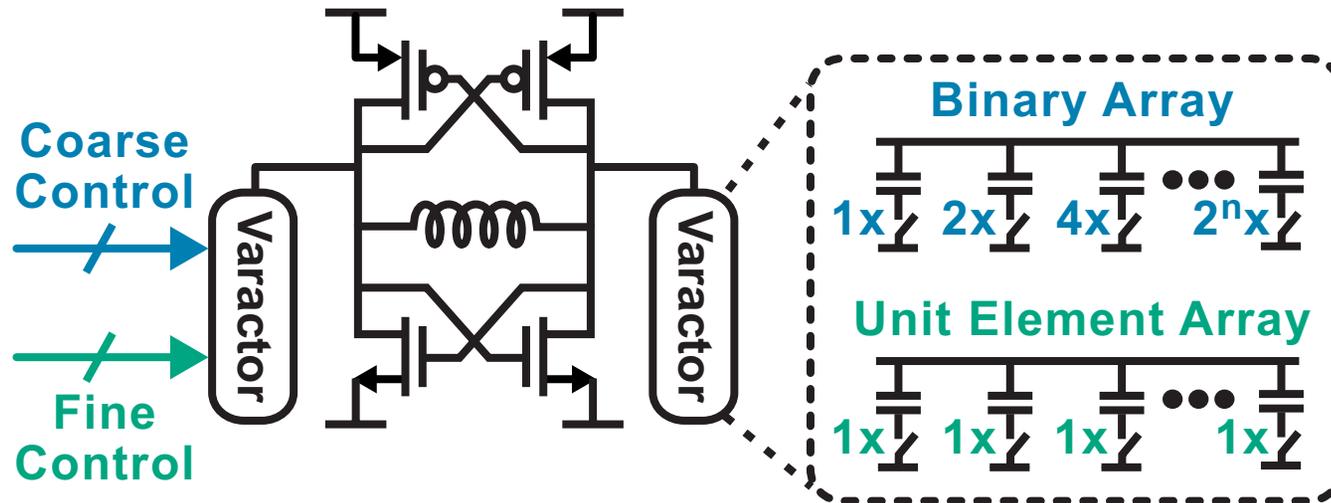
- Use a DAC to control a conventional LC oscillator
 - Allows the use of an existing VCO within a digital PLL
 - Can be applied across a broad range of IC processes

A Much More Digital Implementation



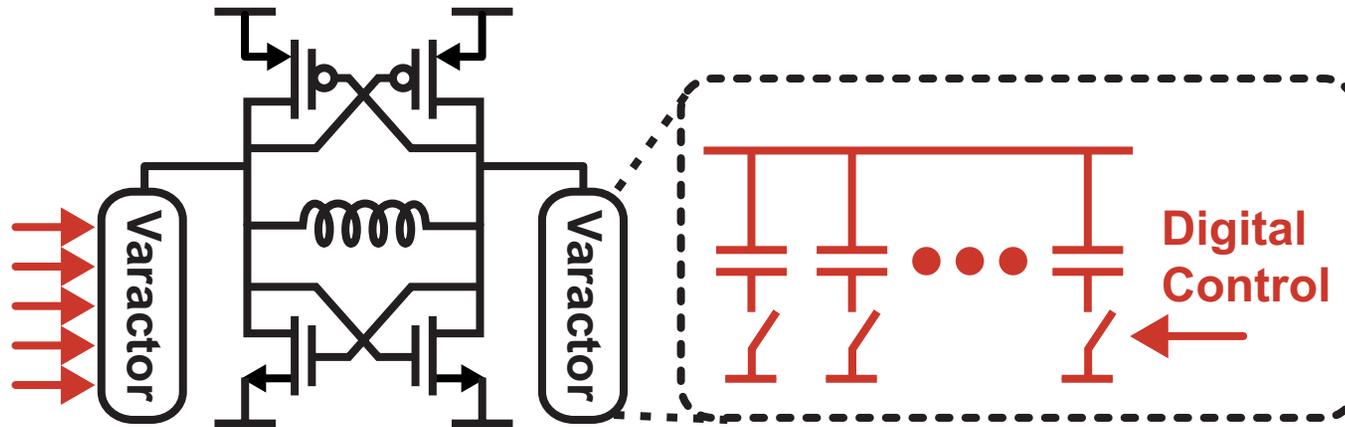
- Adjust frequency in an LC oscillator by switching in a variable number of small capacitors
 - Most effective for CMOS processes of 0.13u and below

Leveraging Segmentation in Switched Capacitor DCO



- Similar in design as *segmented* capacitor DAC structures
 - Binary array: efficient control, but may lack monotonicity
 - Unit element array: monotonic, but complex control
- Coarse and fine control segmentation of DCO
 - Coarse control: active only during initial frequency tuning (leverage binary array)
 - Fine control: controlled by PLL feedback (leverage unit element array to guarantee monotonicity)

Noise Spectrum of a Switched Cap DCO

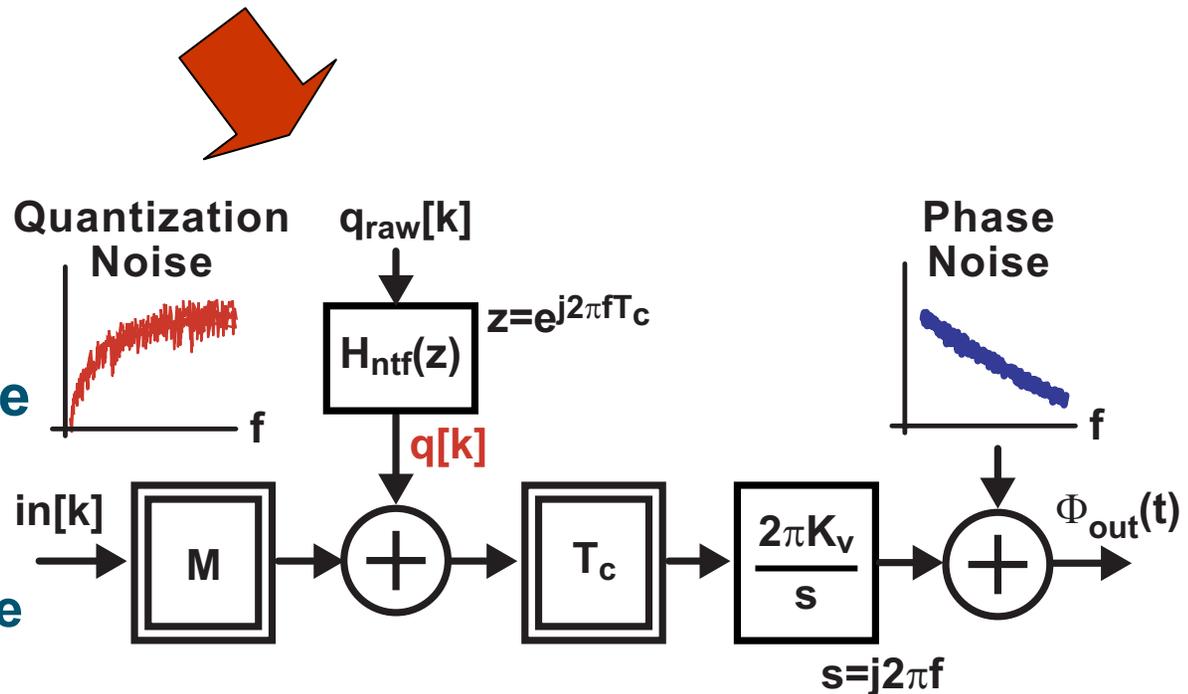


Phase noise

- Same as for conventional VCO (tank Q, etc.)

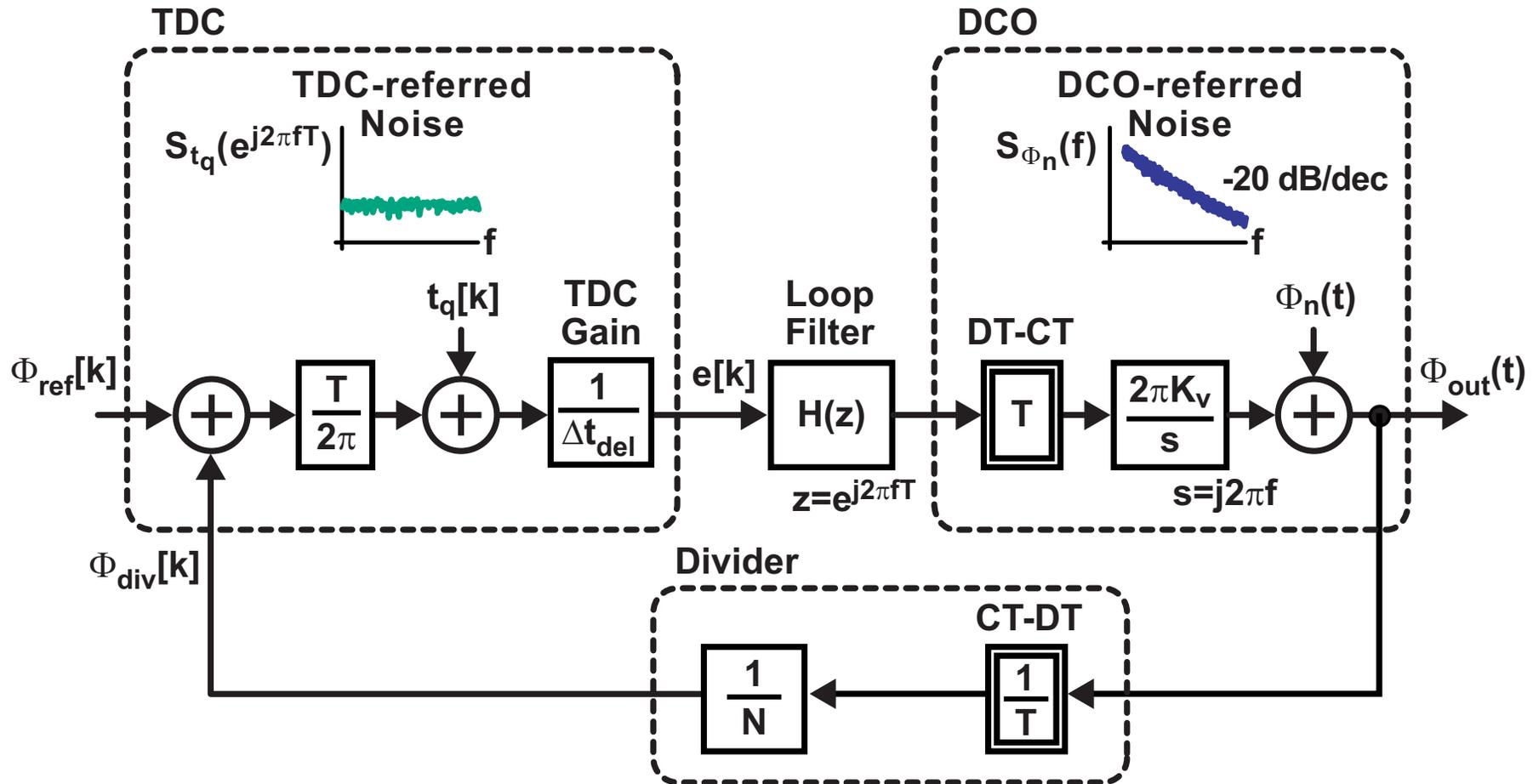
Quantization noise from dithering

- Designed to be lower than phase noise



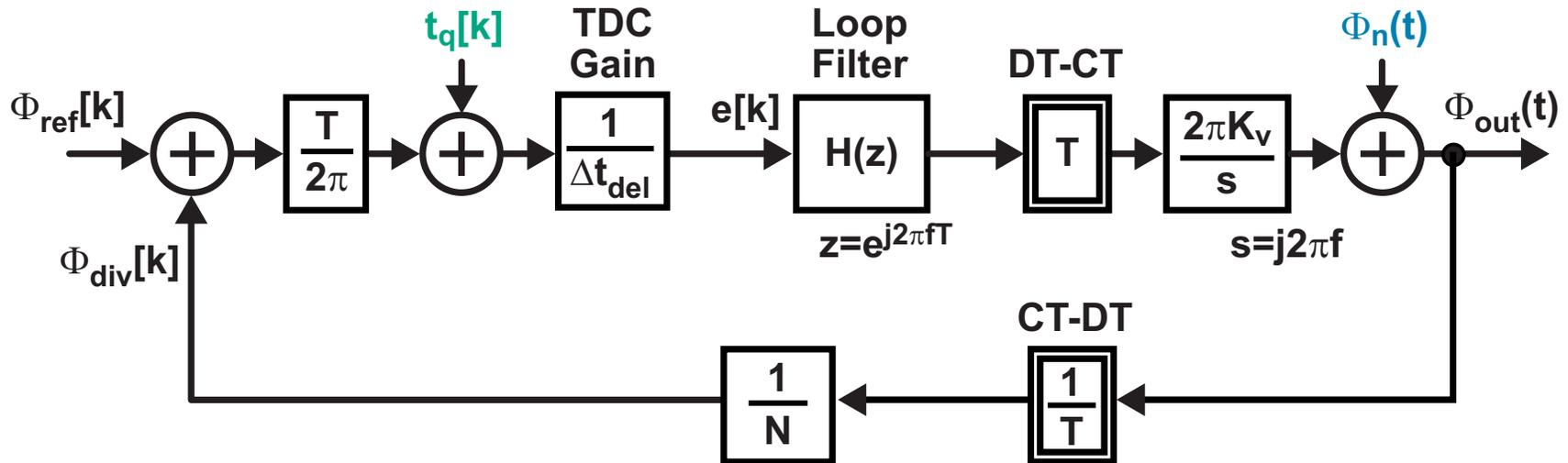
Modeling

Overall Digital PLL Model



- TDC and DCO-referred noise influence overall phase noise according to associated transfer functions to output
- Calculations involve both discrete *and* continuous time

Key Transfer Functions



- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = \frac{(1/\Delta t_{del})H(e^{j2\pi fT})T2\pi K_v/(2\pi jf)}{1 + (1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

- **DCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_n} = \frac{1}{1 + (1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

Transfer Function Parameterization Calculations

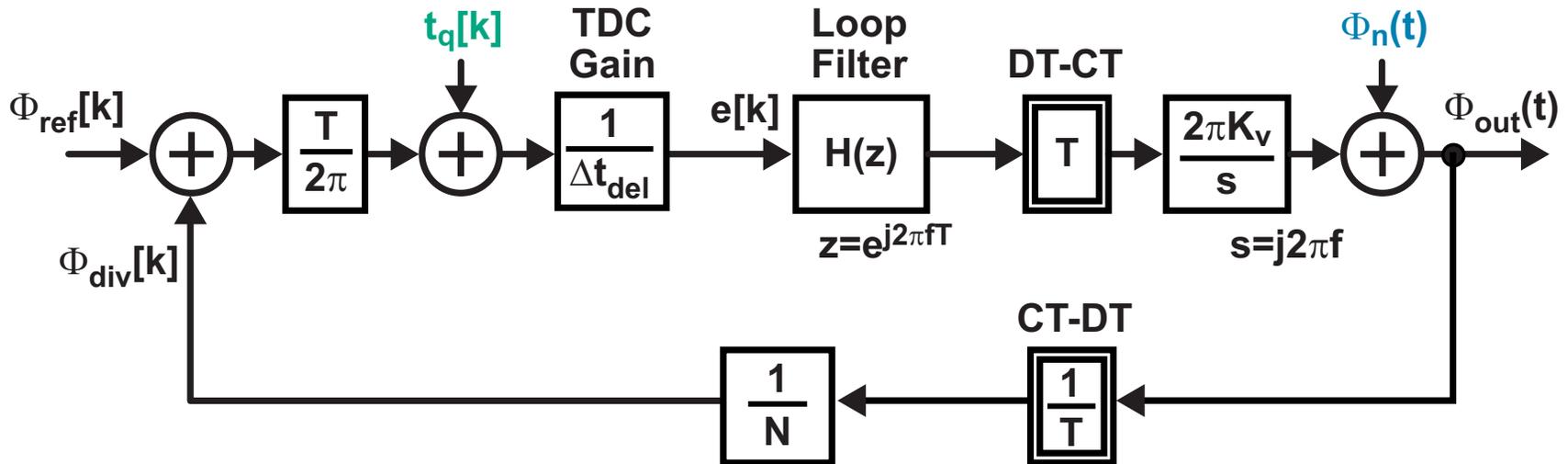
- TDC-referred noise

$$\begin{aligned}\frac{\Phi_{out}}{t_q} &= \frac{(1/\Delta t_{del})H(e^{j2\pi fT})T2\pi K_v/(2\pi jf)}{1 + (1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)} \\ &= \frac{2\pi NA(f)}{1 + A(f)} = 2\pi NG(f)\end{aligned}$$

- DCO-referred noise

$$\begin{aligned}\frac{\Phi_{out}}{\Phi_n} &= \frac{1}{1 + (1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)} \\ &= \frac{1}{1 + A(f)} = \frac{1 + A(f) - A(f)}{1 + A(f)} = 1 - G(f)\end{aligned}$$

Key Observations



- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = 2\pi N G(f)$$



Lowpass with a DC gain of $2\pi N$

- **DCO-referred noise**

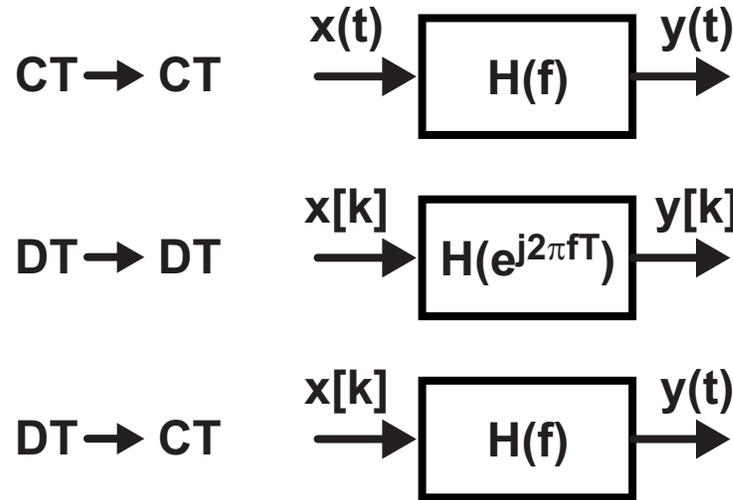
$$\frac{\Phi_{out}}{\Phi_n} = 1 - G(f)$$



Highpass with a high frequency gain of 1

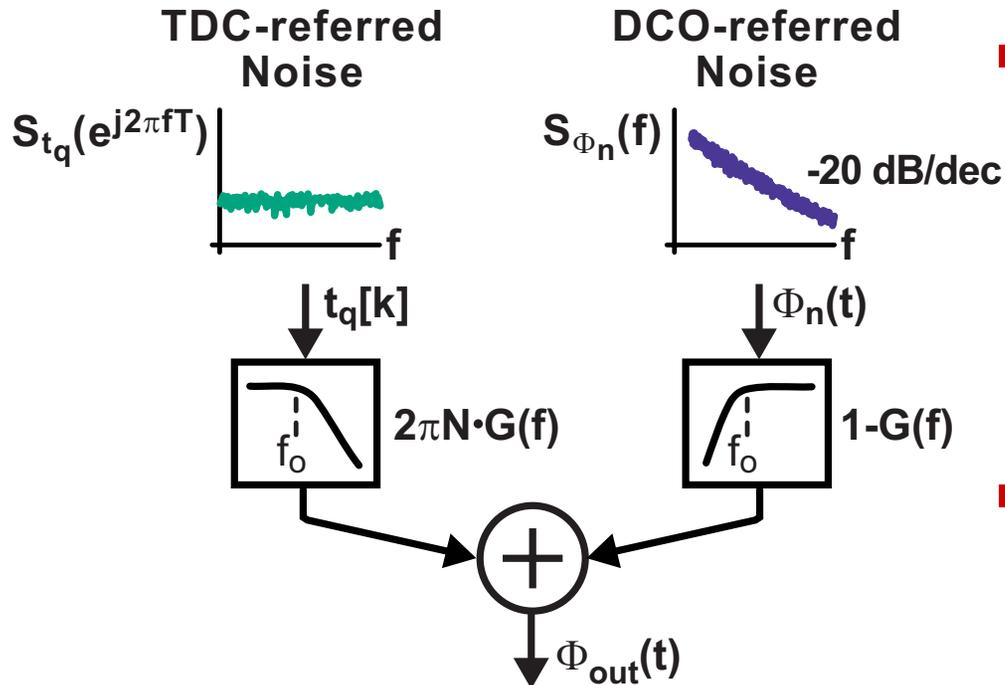
How do we calculate the output phase noise?

Spectral Density Calculations



- **CT → CT** $S_y(f) = |H(f)|^2 S_x(f)$
- **DT → DT** $S_y(e^{j2\pi fT}) = |H(e^{j2\pi fT})|^2 S_x(e^{j2\pi fT})$
- **DT → CT** $S_y(f) = \frac{1}{T} |H(f)|^2 S_x(e^{j2\pi fT})$

Phase Noise Calculation

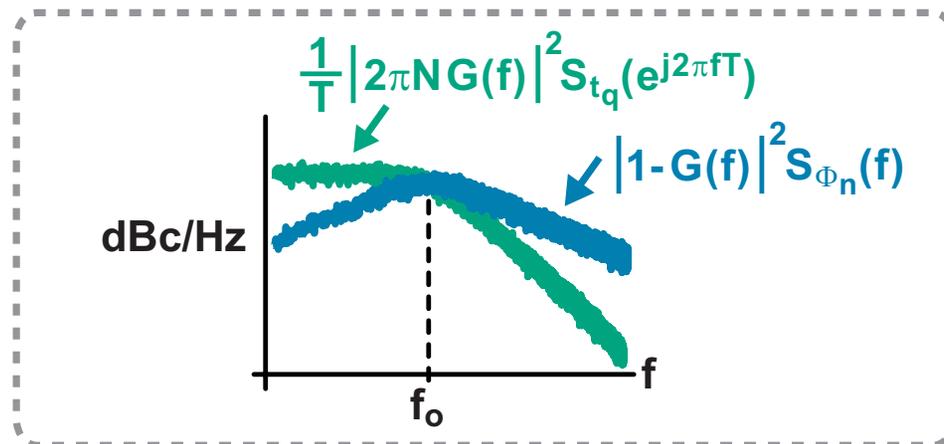


■ TDC noise

- DT to CT calculation
- Dominates PLL phase noise at low frequency offsets

■ DCO noise

- CT to CT calculation
- Dominates PLL phase noise at high frequency offsets



Example Calculation for Delay Chain TDC

- Ref freq = $1/T = 50$ MHz,
Out freq = 3.6 GHz

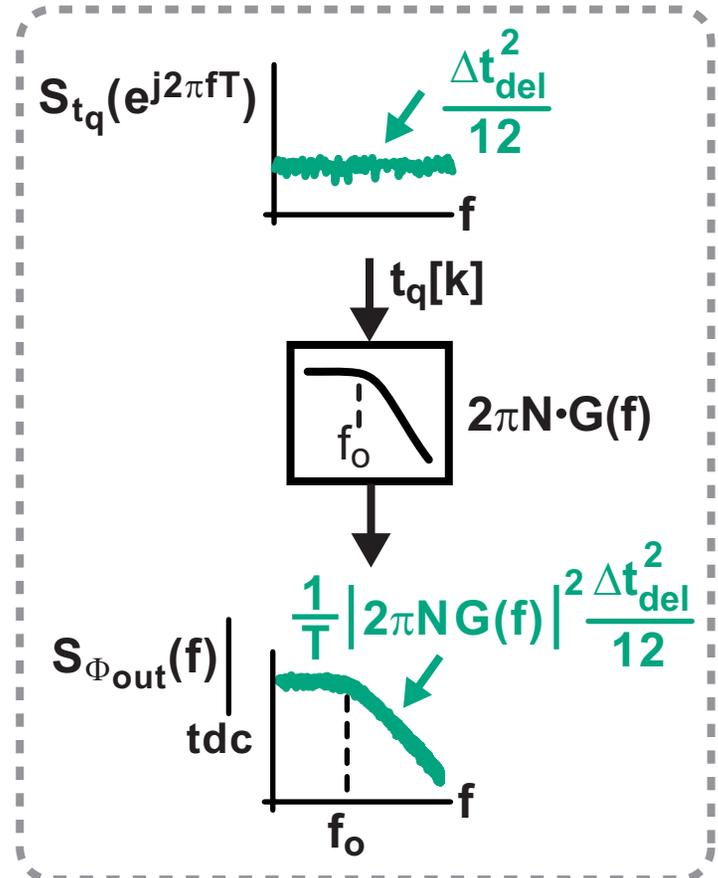
$$\Rightarrow N = \frac{3600}{50} = 72$$

- Inverter delay = $\Delta t_{del} = 20$ ps

$$\begin{aligned} S_{\Phi_{out}}(f) \Big|_{tdc} &= \frac{1}{T} |2\pi N G(f)|^2 \frac{\Delta t_{del}^2}{12} \\ &= 3.4 \cdot 10^{-10} |G(f)|^2 \end{aligned}$$

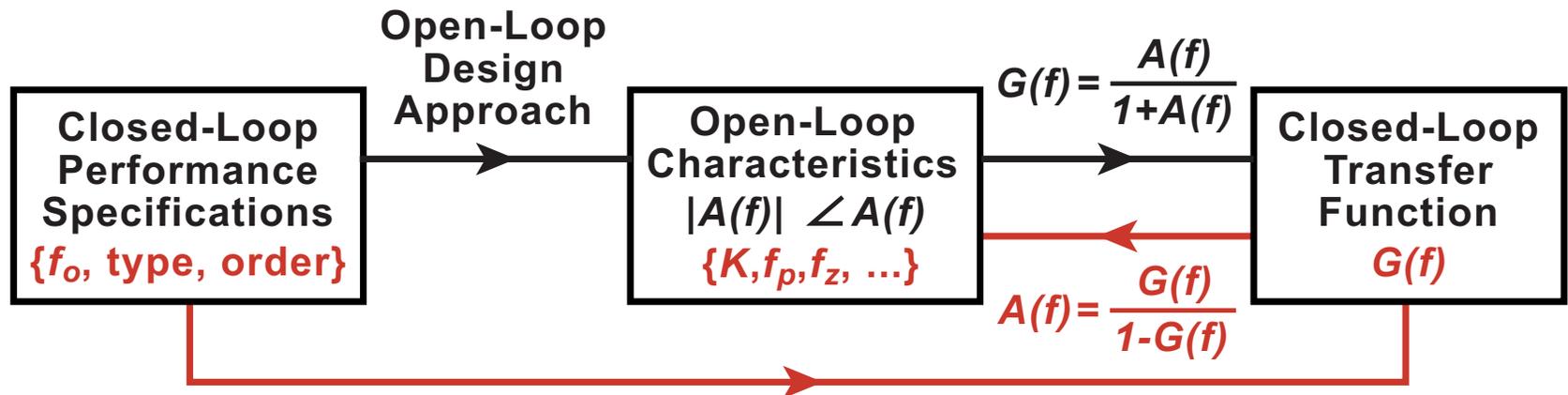
- Note: $G(f) = 1$ at low offset frequencies

$$10 \log(3.4 \cdot 10^{-10}) = -94.7 \text{ dBc/Hz (at low offset freq.)}$$



CAD Tools

Closed Loop PLL Design Approach



Lau and Perrott,
DAC, June 2003

- **Classical open loop approach**
 - Indirectly design $G(f)$ using bode plots of $A(f)$
- **Proposed closed loop approach**
 - Directly design $G(f)$ by examining impact of its specifications on phase noise (and settling time)
 - Solve for $A(f)$ that will achieve desired $G(f)$

Implemented in *PLL Design Assistant Software*

<http://www.cppsim.com>

Evaluate Phase Noise with 500 kHz PLL Bandwidth

■ Key PLL parameters:

- $G(f)$: 500 kHz BW, Type II, 2nd order rolloff
- TDC noise: -94.7 dBc/Hz
- DCO noise: -153 dBc/Hz at 20 MHz offset (3.6 GHz carrier)

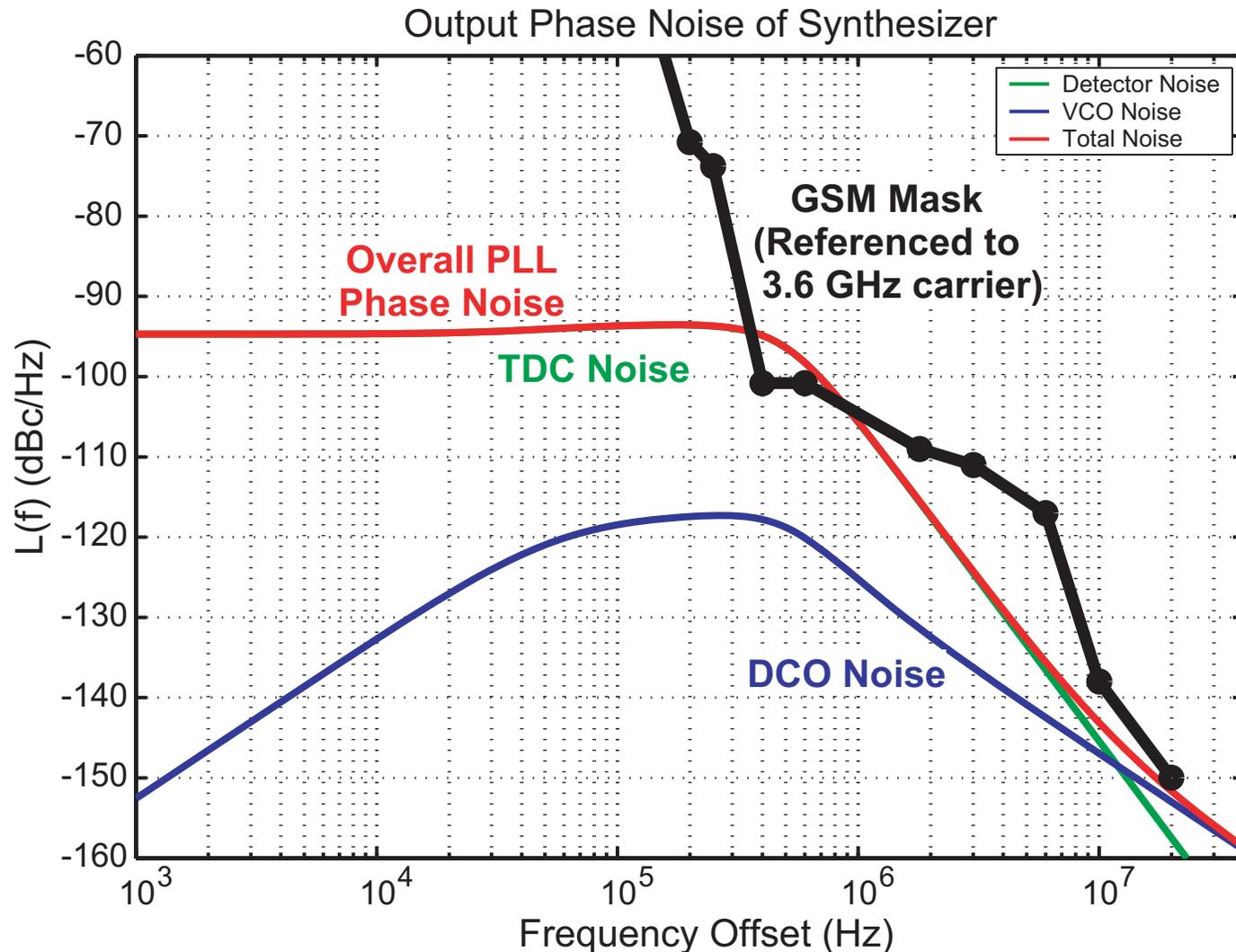
The screenshot shows the PLL Design Assistant software interface. The window title is "PLL Design Assistant". The interface is divided into several sections:

- Dynamic Parameters:** Includes fields for f_o (500e3 Hz), order (radio buttons for 1, 2, 3), shape (radio buttons for Butter, Bessel, Cheby1, Cheby2, Elliptical), ripple (dB), type (radio buttons for 1, 2), and f_z/f_o (1/10).
- Noise Parameters:** Includes fields for ref. freq (50e6 Hz), out freq. (3.6e9 Hz), Detector (-94.7 dBc/Hz), VCO (-153 dBc/Hz), and freq. offset (20e6 Hz). There are also radio buttons for S-D (1, 2, 3, 4, 5) and On/Off buttons.
- Resulting Open Loop Parameters:** Shows K (7.509e+011), fp (7.655e+005 Hz), fz (5.000e+004 Hz), and Qp. Each has an "alter:" button.
- Resulting Plots and Jitter:** Includes an "Apply" button, radio buttons for Pole/Zero Diagram, Step Response, and Noise Plot, and a field for rms jitter (980.788 fs).

A red dashed circle highlights the Dynamic Parameters and Noise Parameters sections.

PLL Design Assistant
Written by Michael Perrott (<http://www-mtl.mit.edu/~perrott>)

Calculated Phase Noise Spectrum with 500 kHz BW



TDC noise too high for GSM mask with 500 kHz PLL bandwidth

Change PLL Bandwidth to 100 kHz

■ Key PLL parameters:

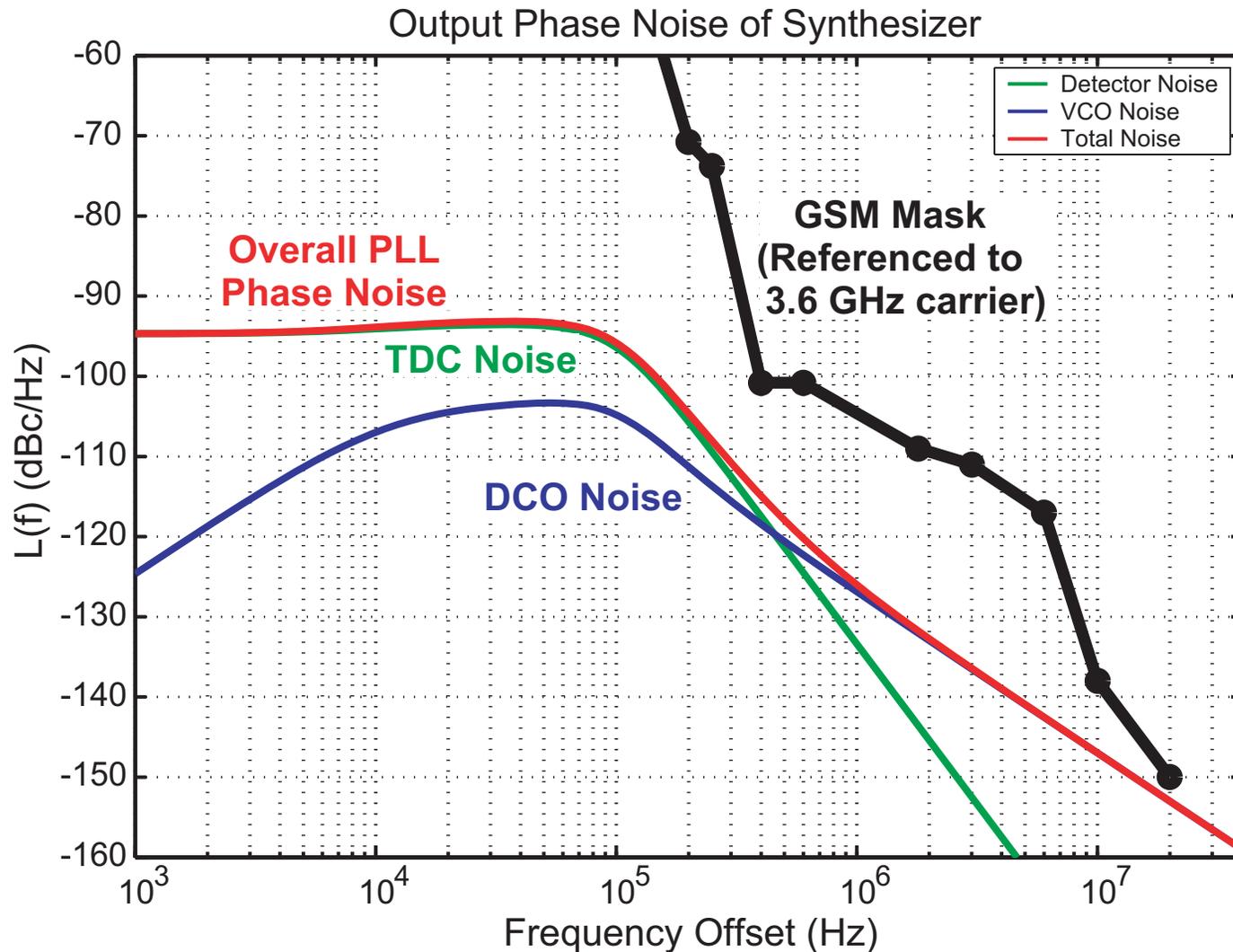
- **G(f): 100 kHz BW**, Type = 2, 2nd order rolloff
- TDC noise: -94.7 dBc/Hz
- DCO noise: -153 dBc/Hz at 20 MHz offset (3.6 GHz carrier)

The screenshot shows the PLL Design Assistant software interface. The window title is "PLL Design Assistant". The interface is divided into several sections:

- Dynamic Parameters:** Contains fields for f_o (set to 100e3 Hz), order (set to 2), shape (Butter selected), ripple (dB), type (set to 2), and f_z/f_o (set to 1/10).
- Noise Parameters:** Contains fields for ref. freq (50e6 Hz), out freq. (3.6e9 Hz), Detector (-94.7 dBc/Hz), VCO (-153 dBc/Hz), and freq. offset (20e6 Hz). There are also S-D options (1, 2, 3, 4, 5) and On/Off buttons.
- Resulting Open Loop Parameters:** Shows K (3.004e+010), f_p (1.531e+005 Hz), f_z (1.000e+004 Hz), and Qp. Each has an "alter:" field and an On/Off button.
- Resulting Plots and Jitter:** Includes an "Apply" button, plot type options (Pole/Zero Diagram, Transfer Function, Step Response, Noise Plot), and numerical values for jitter (1e3, 40e6, -160, -60) and rms jitter (464.961 fs).

At the bottom of the window, it says "PLL Design Assistant" and "Written by Michael Perrott (<http://www-mtl.mit.edu/~perrott>)".

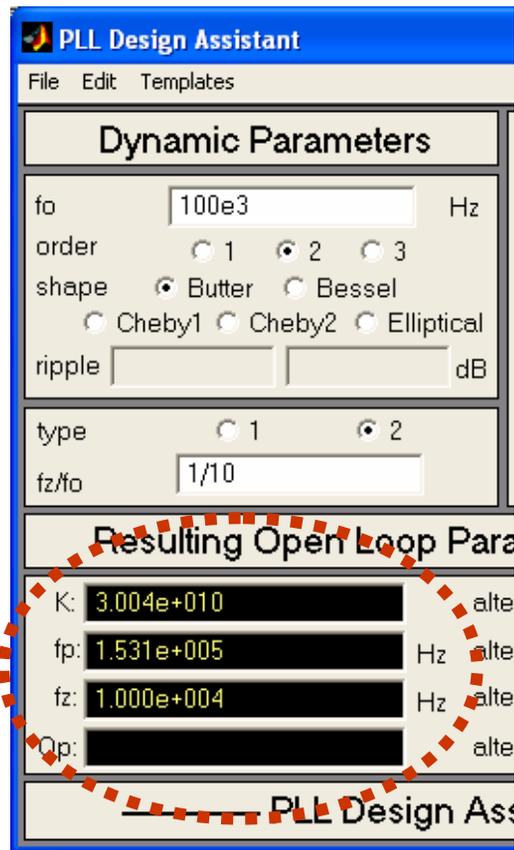
Calculated Phase Noise Spectrum with 100 kHz BW



GSM mask is met with 100 kHz PLL bandwidth

Loop Filter Design using PLL Design Assistant

- **PLL Design Assistant allows fast loop filter design**
 - See Section 4 of Supplemental Slides
 - Assumption: $Type = 2$, 2^{nd} order rolloff



$$H(z) = K_{LF} \left(\frac{1}{1 - z^{-1}} \right) \frac{1 - b_1 z^{-1}}{1 - a_1 z^{-1}}$$

■ Where:

$$a_1 = \frac{1}{1 + w_p T} \quad b_1 = \frac{1}{1 + w_z T}$$

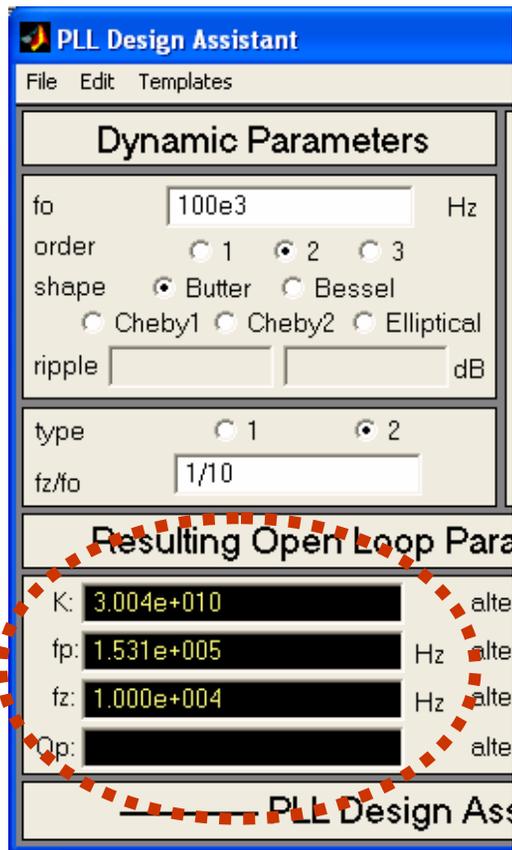
$$K_{LF} = \left(\frac{\Delta t_{del}}{T/N} \right) \frac{K}{K_v} \left(\frac{w_p}{w_z} \right) \frac{a_1}{b_1} T$$

- **PLL Design Assistant provides the values of K , $w_p = 2\pi f_p$, $w_z = 2\pi f_z$**

Example Digital Loop Filter Calculation

Assumptions

- Ref freq ($1/T$) = 50 MHz, Out freq = 3.6 GHz (so $N = 72$)
- $\Delta t_{del} = 20$ ps, $K_v = 12$ kHz/unit cap
- 100 kHz bandwidth, Type = 2, 2nd order rolloff



$$H(z) = K_{LF} \left(\frac{1}{1 - z^{-1}} \right) \frac{1 - b_1 z^{-1}}{1 - a_1 z^{-1}}$$

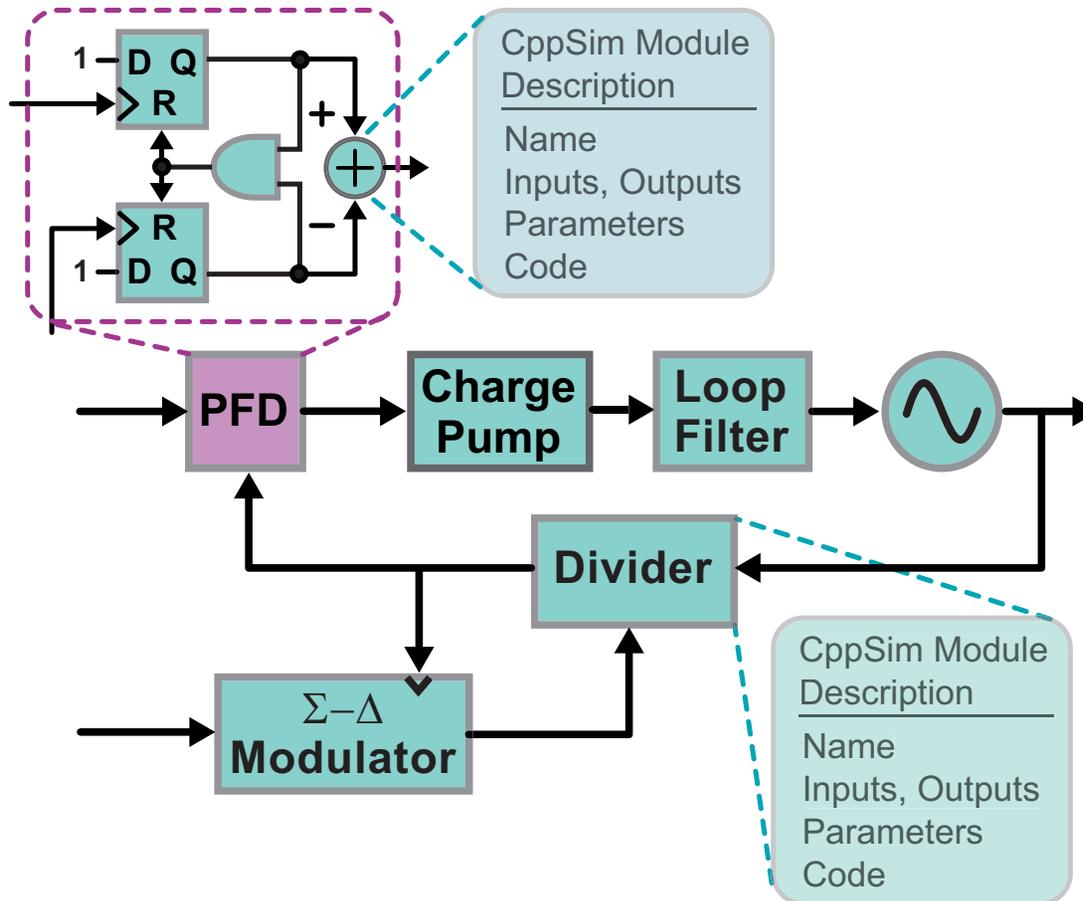
$$b_1 = \frac{1}{1 + 2\pi 10\text{kHz}/50\text{MHz}} = .9987$$

$$a_1 = \frac{1}{1 + 2\pi 153\text{kHz}/50\text{MHz}} = .9811$$

$$K_{LF} = \left(\frac{\Delta t_{del}}{T/N} \right) \frac{3 \cdot 10^{10}}{12\text{kHz}} \frac{153}{10} \frac{.9811}{.9987} \frac{1}{50\text{MHz}}$$

$$= \left(\frac{\Delta t_{del}}{T/N} \right) 0.75 = \left(\frac{\Delta t_{del}}{T_{dco}} \right) 0.75$$

Verify Calculations Using C++ Behavioral Modeling

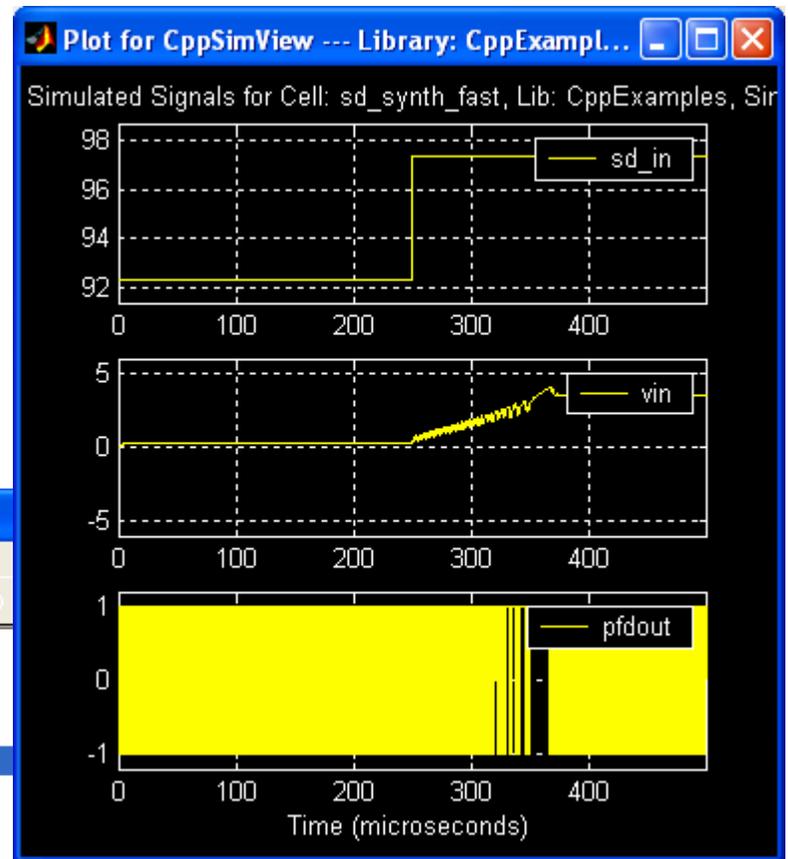
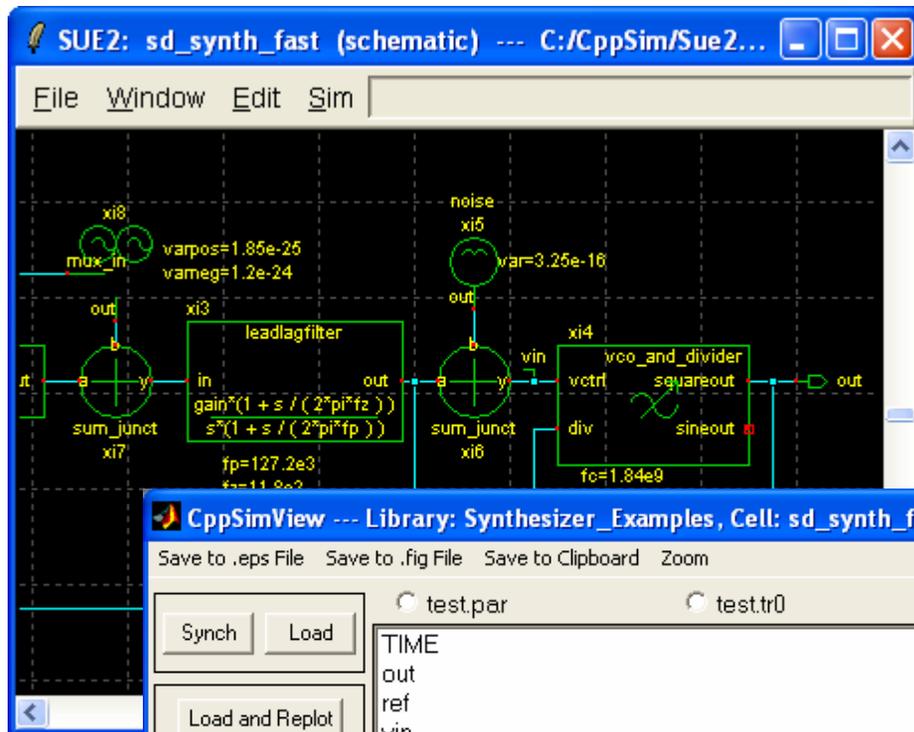


- **Schematic**
 - Hierarchical description of *system topology*

- **Code blocks**
 - Specification of *module behavior* using **templated C++ code**

- **Behavioral environment allows efficient architectural investigation and validation of calculations**
 - Fast simulation speed is essential for design investigation

CppSim – A Fast C++ Behavioral Simulator



CppSimView --- Library: Synthesizer_Examples, Cell: sd_synth_fast

Save to .eps File Save to .fig File Save to Clipboard Zoom

Synch Load

Load and Replot

Reset Node List

Back Forward

Create Matlab Code

test.par test.tr0

TIME
out
ref
vin
pfdout
sd_in
div_val
xi12_xor_out

plotsig(x.'sd_in;vin;pfdout')

CppSim: C++ Behavioral Simulation

Written by Michael Perrott (<http://www-mtl.mit.edu/~perrott>)

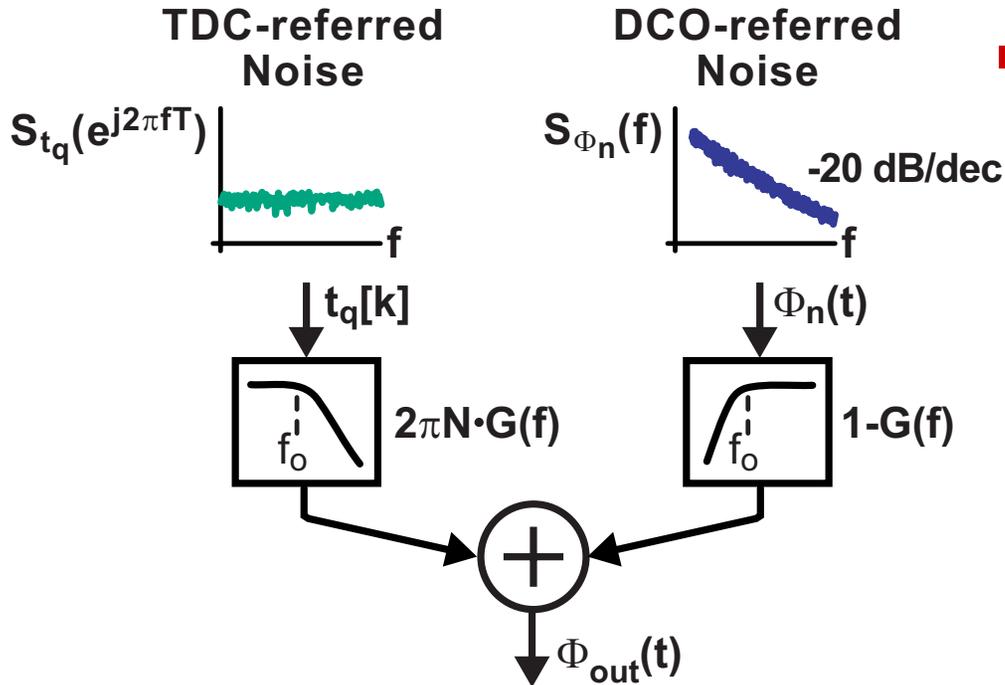
<http://www.cppsim.com>

How Do We Improve TDC Performance?

Two Key Issues:

- **TDC resolution**
- **Mismatch**

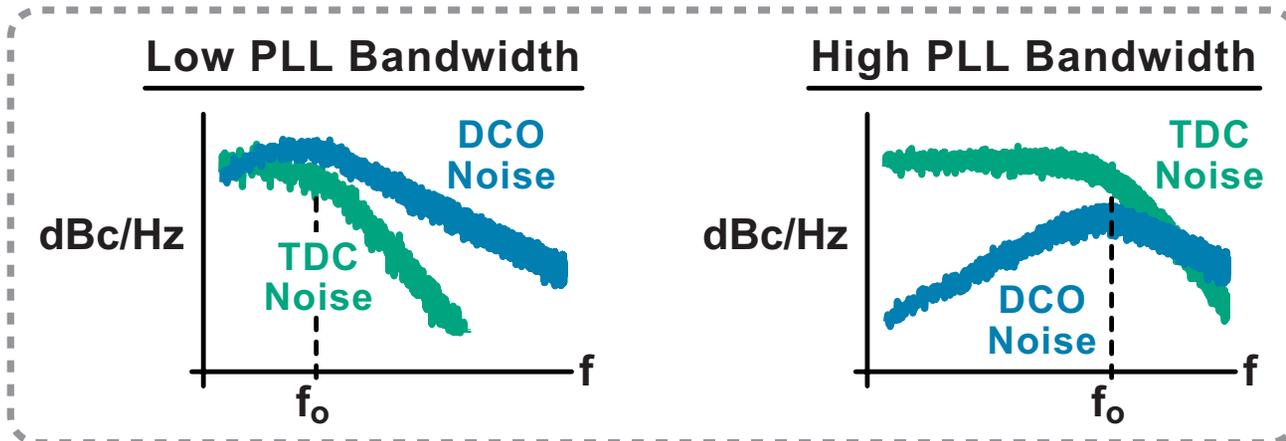
Motivation



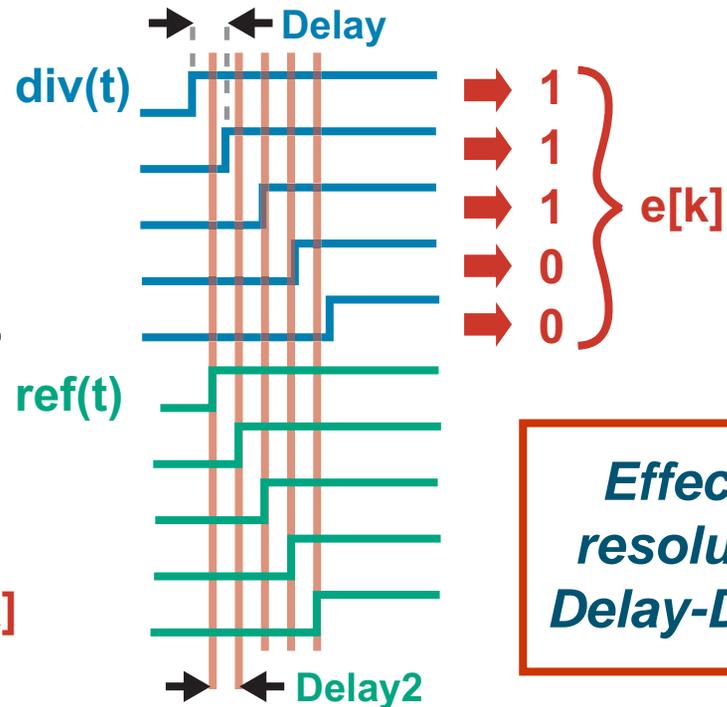
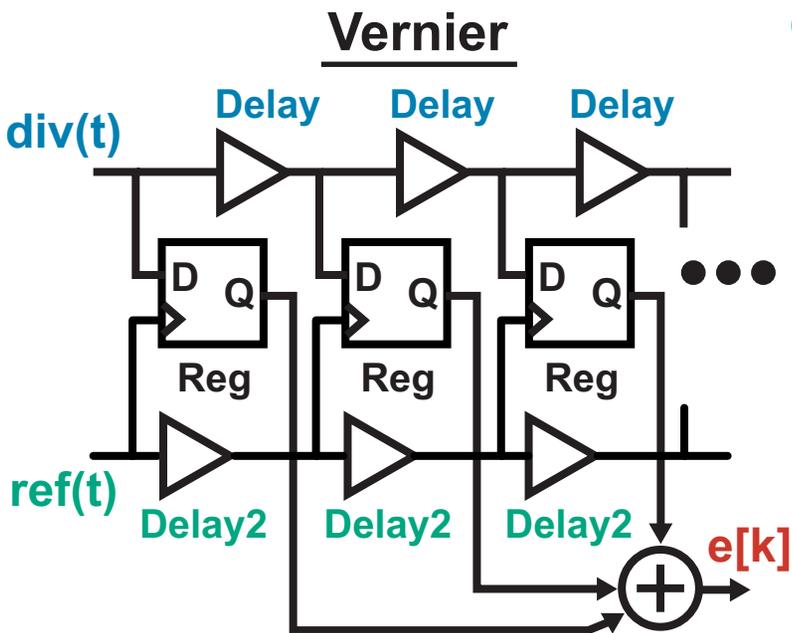
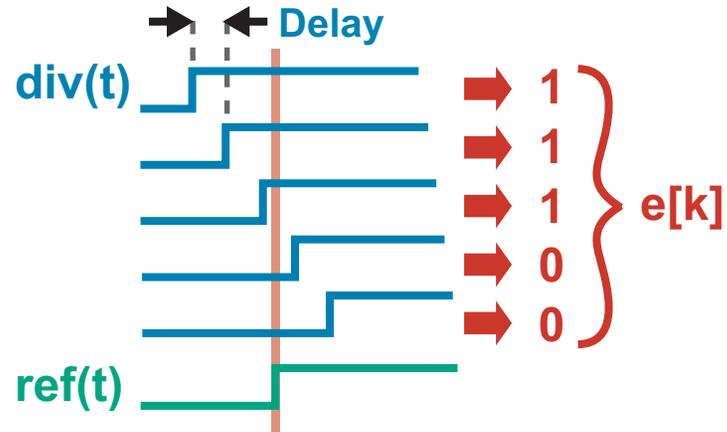
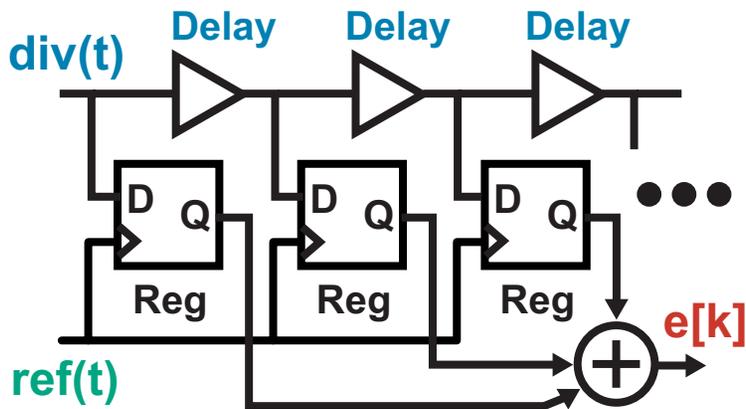
- PLL bandwidth dramatically influences relative impact of TDC and VCO noise

Want high PLL bandwidth?

➔ Need low TDC Noise



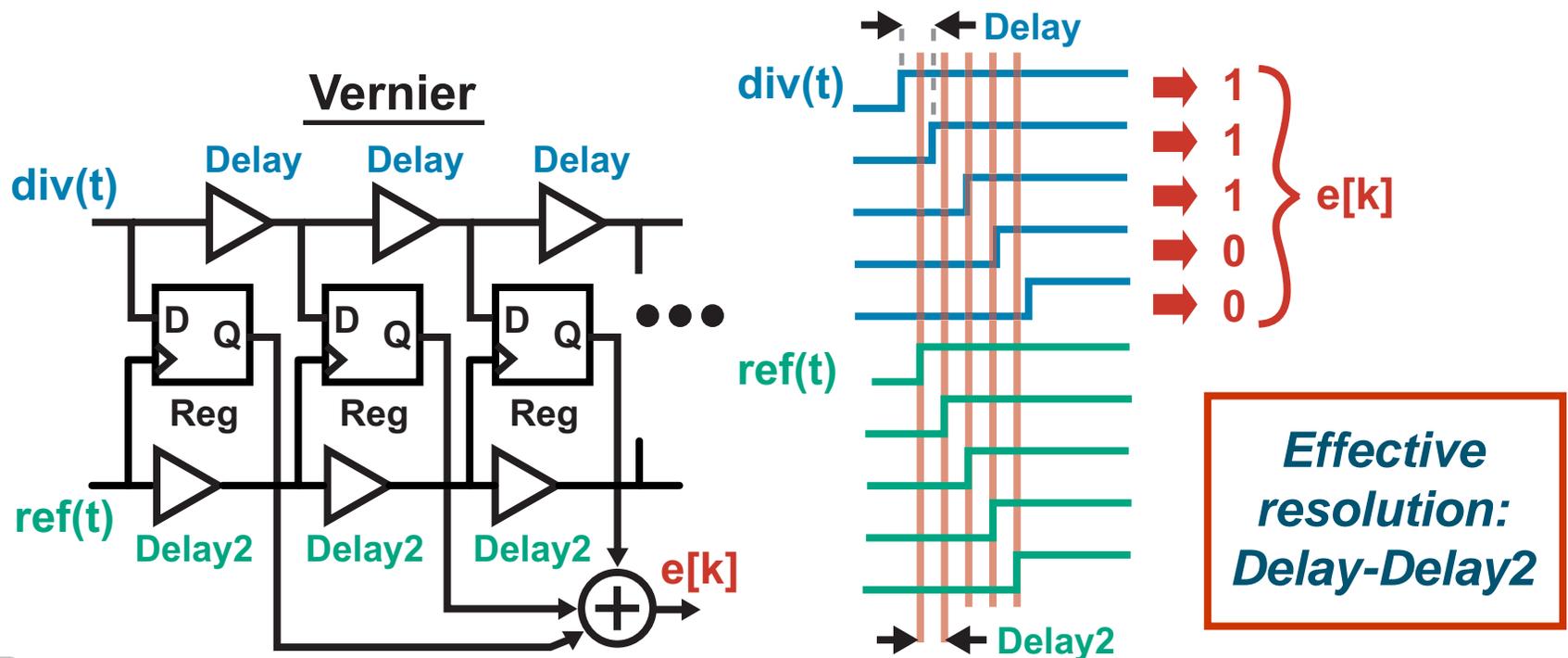
Improve Resolution with Vernier Delay Technique



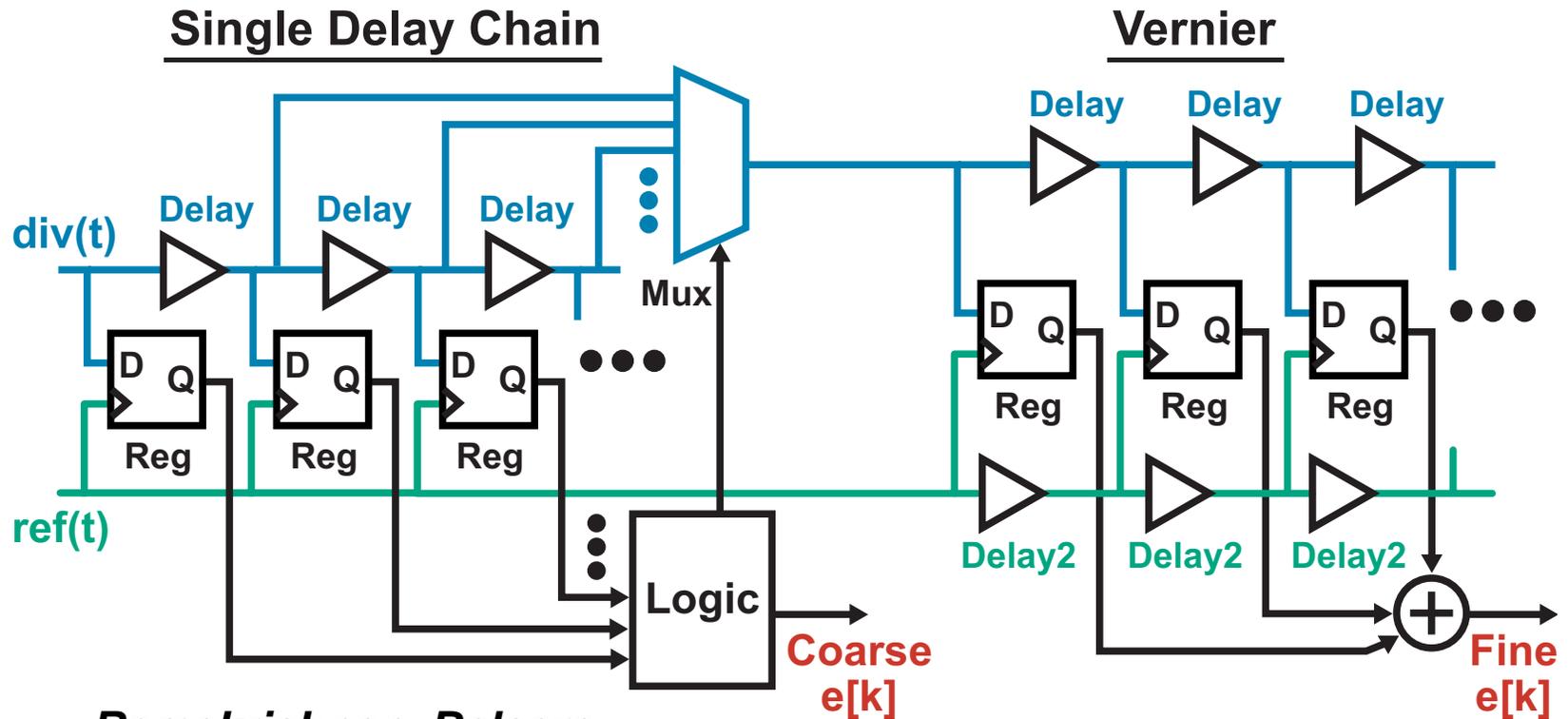
**Effective resolution:
Delay-Delay2**

Issues with Vernier Approach

- Mismatch issues are more severe than the single delay chain TDC
 - Reduced delay is formed as *difference* of two delays
- Large measurement range requires large area
 - Initial PLL frequency acquisition may require a large range

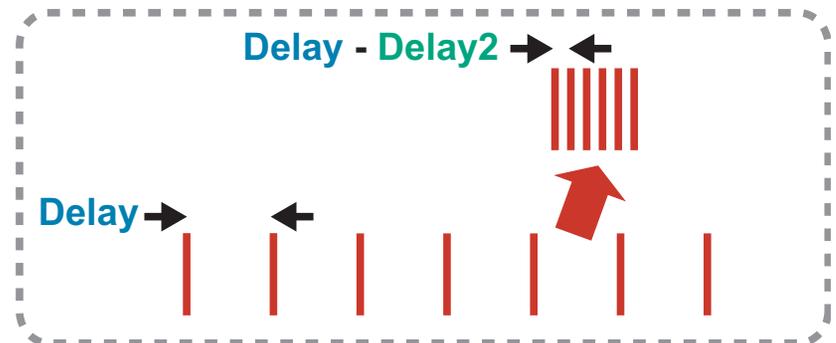


Two-Step TDC Architecture Allows Area Reduction

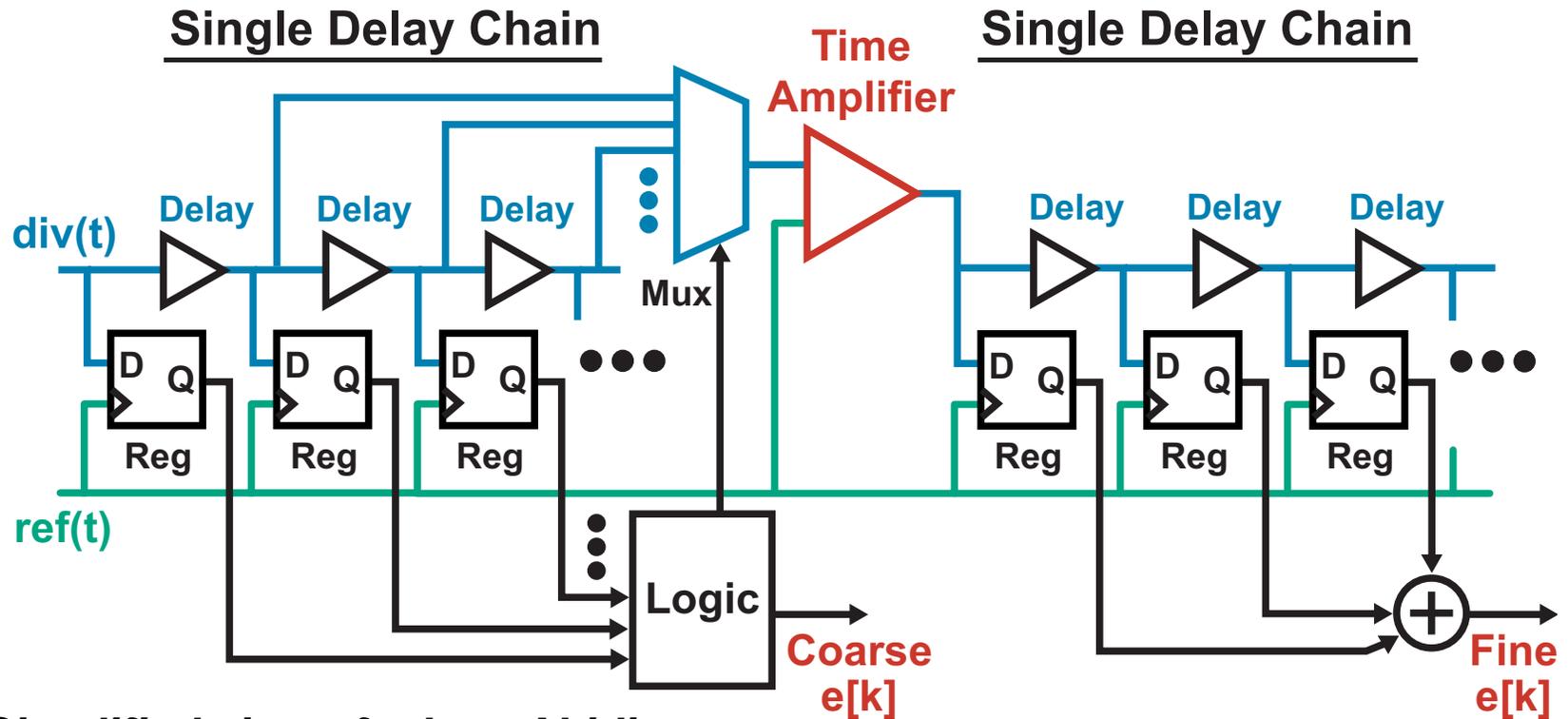


Ramakrishnan, Balsara
VLSID '06

- Single delay chain provides coarse resolution
- (Folded) Vernier provides fine resolution

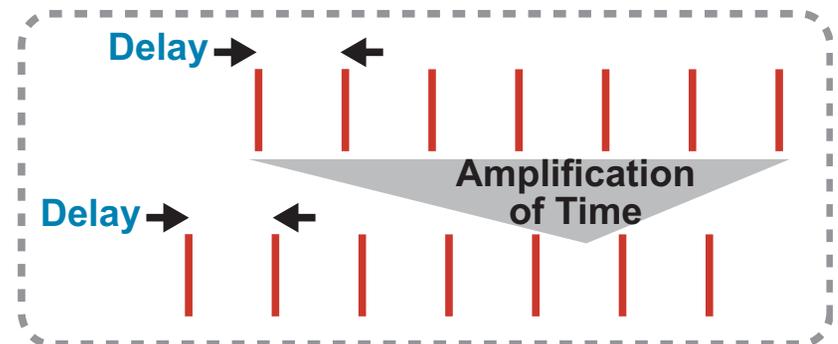


Two-Step TDC Using Time Amplification

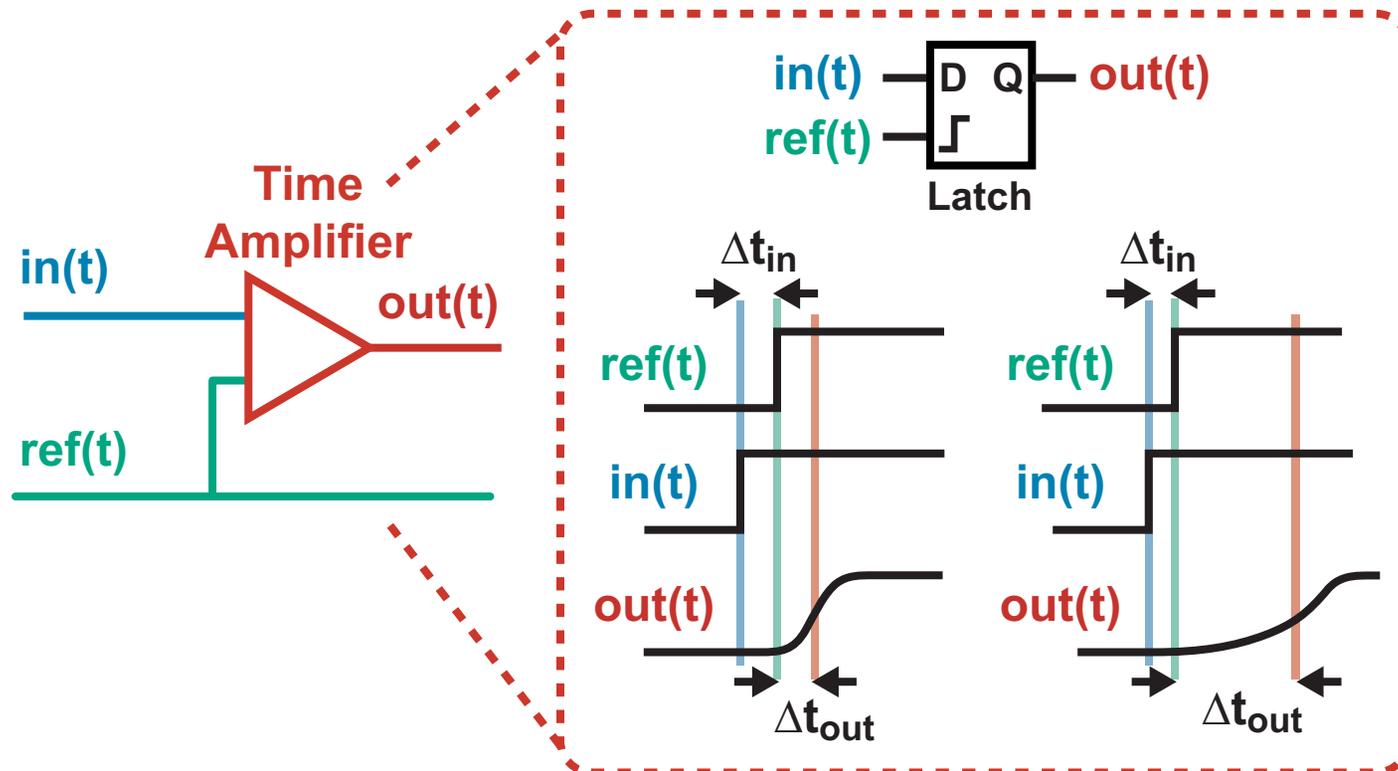


Simplified view of: Lee, Abidi
VLSI 2007

- Single delay chain provides coarse and fine resolution
- Time amplification is used to improve resolution



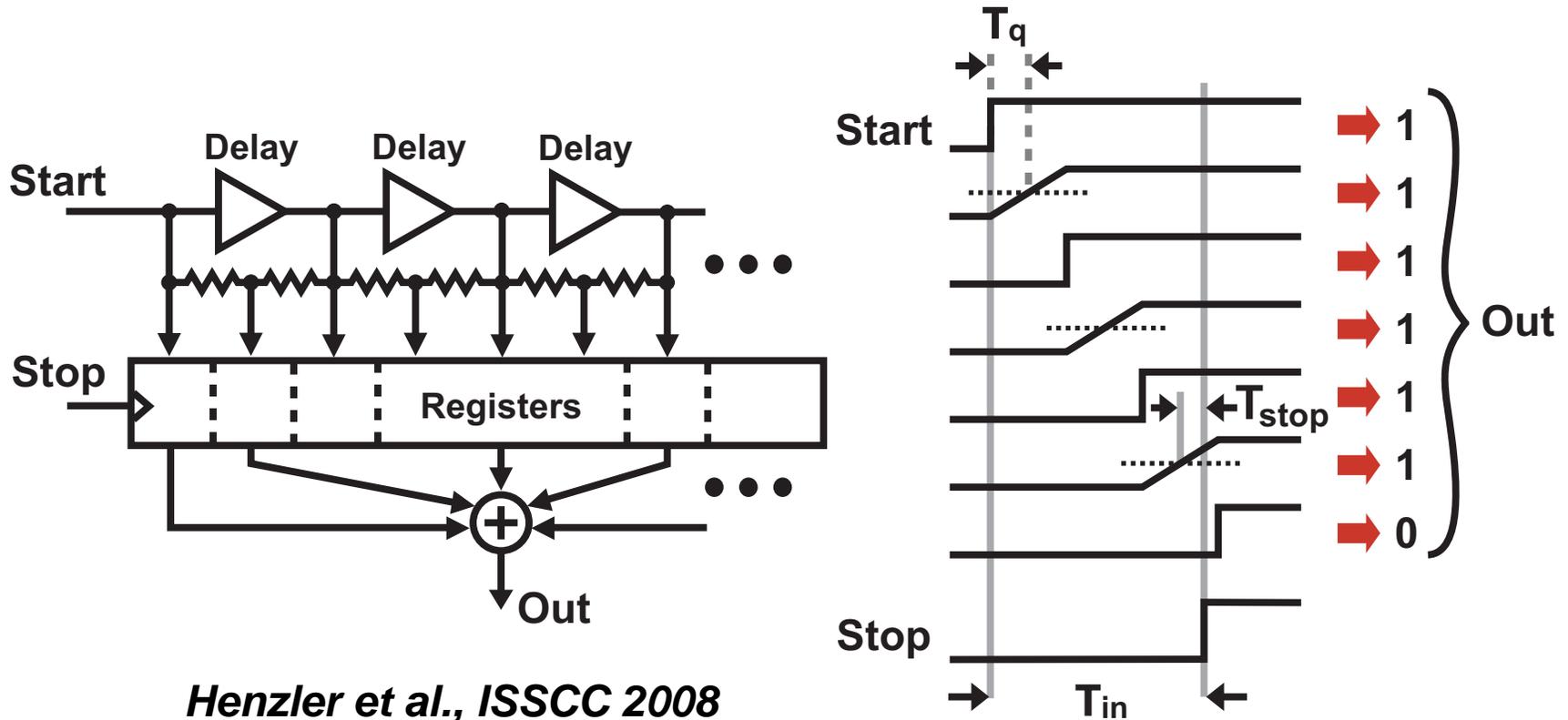
Leveraging Metastability to Create a Time Amplifier



*Simplified view of: Abas, et al., Electronic Letters, Nov 2002
(note that actual implementation uses SR latch)*

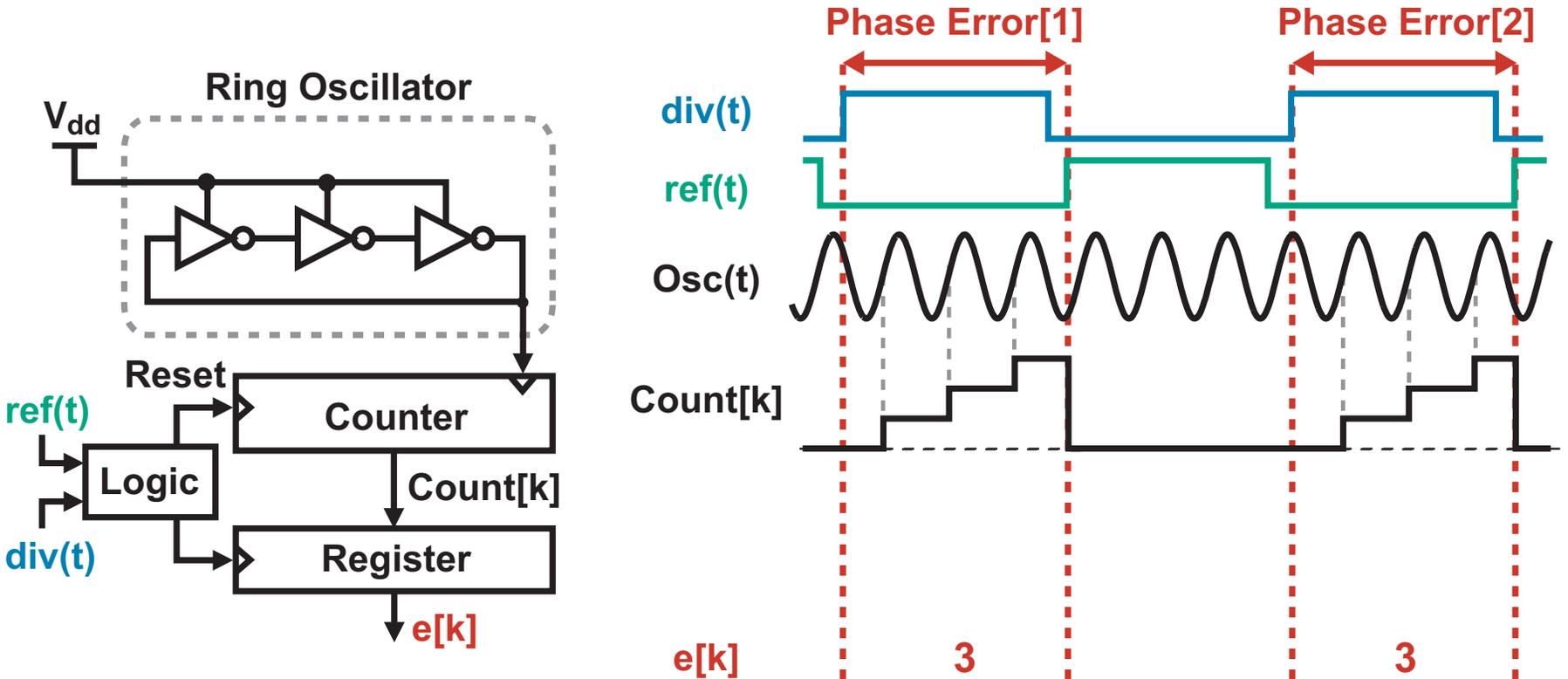
- **Metastability leads to progressively slower output transitions as setup time on latch is encroached upon**
 - Time difference at input is amplified at output

Interpolating time-to-digital converter



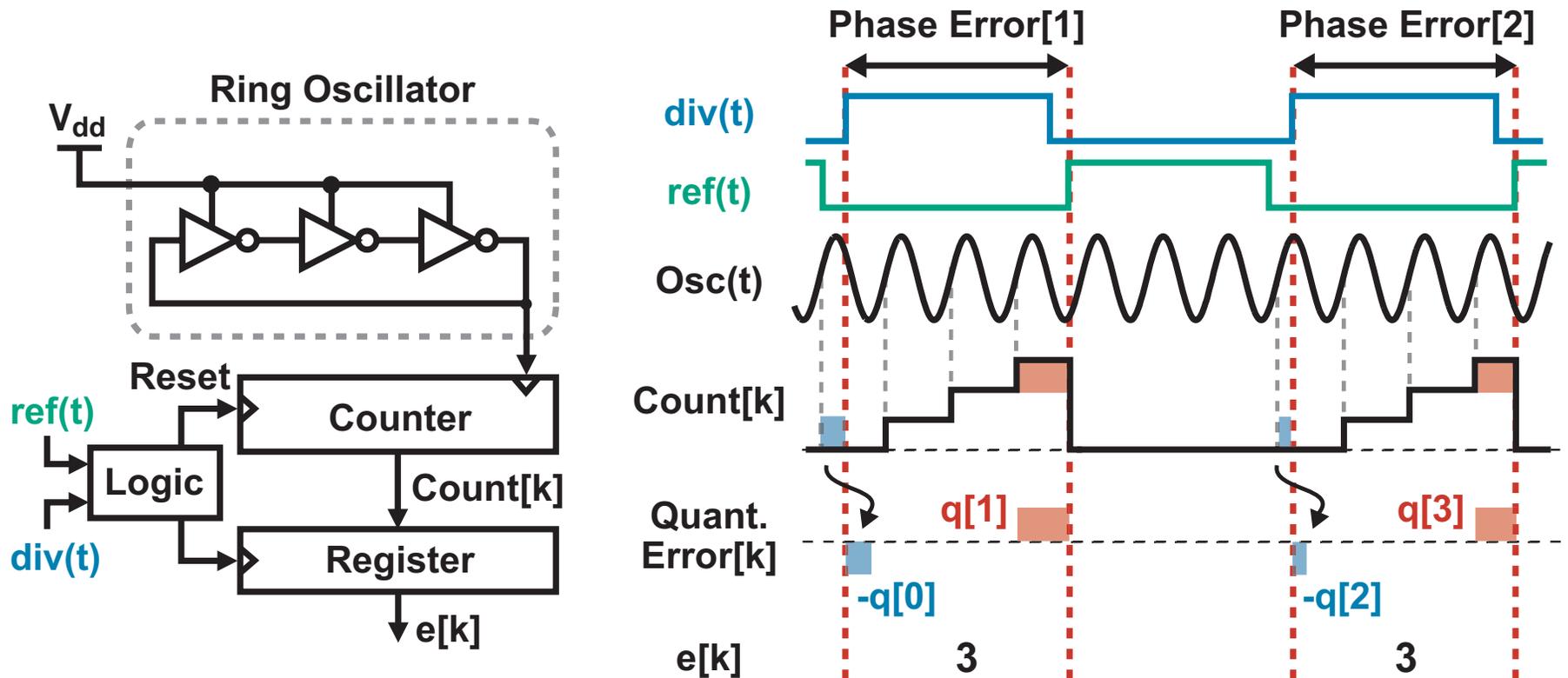
- Interpolate between edges to achieve fine resolution
- Cyclic approach can also be used for large range

An Oscillator-Based TDC



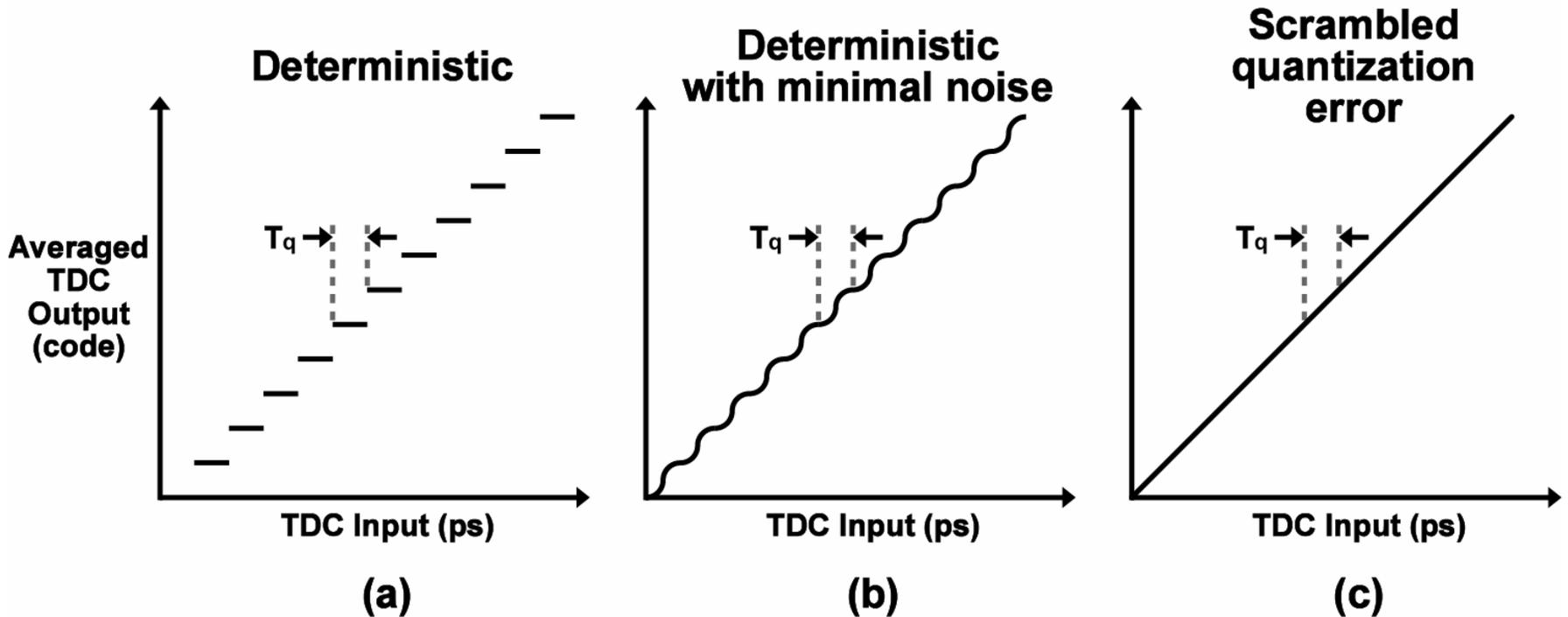
- Output $e[k]$ corresponds to the number of oscillator edges that occur during the measurement time window
- Advantages
 - Extremely large range can be achieved with compact area
 - Quantization noise is scrambled across measurements

A Closer Look at Quantization Noise Scrambling



- Quantization error occurs at beginning and end of each measurement interval
- As a rough approximation, assume error is uncorrelated between measurements
 - Averaging of measurements improves effective resolution

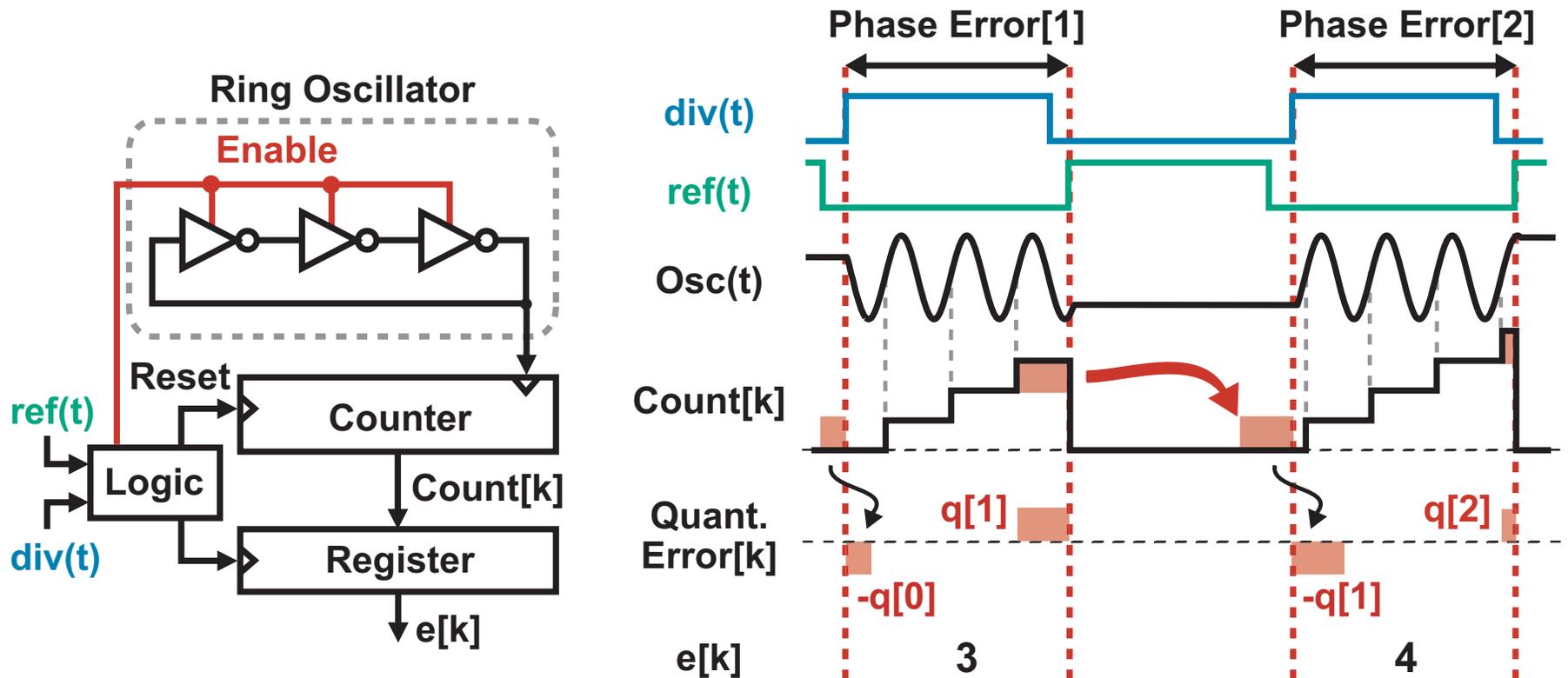
Deterministic quantizer error vs. scrambled error



- **Deterministic TDC do not provide inherent scrambling**
- **For oversampling benefit, *TDC error must be scrambled!***
- **Some systems provide input scrambling ($\Delta\Sigma$ fractional-N PLL), while some others do not (integer-N PLL)**

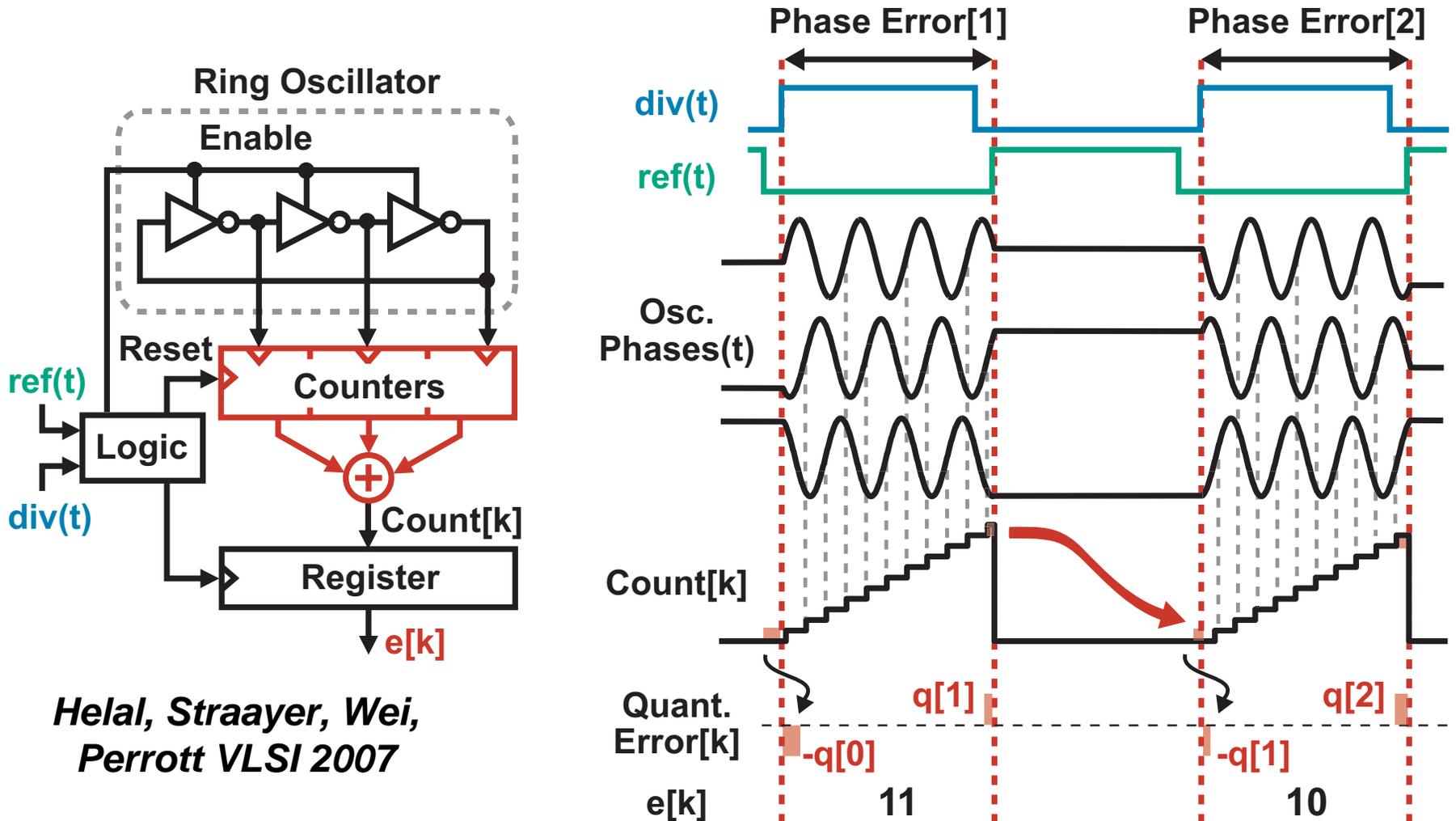
Proposed GRO TDC Structure

A Gated Ring Oscillator (GRO) TDC



- Enable ring oscillator only during measurement intervals
 - Hold the state of the oscillator between measurements
- Quantization error becomes first order noise shaped!
 - $e[k] = \text{Phase Error}[k] + q[k] - q[k-1]$
 - Averaging dramatically improves resolution!

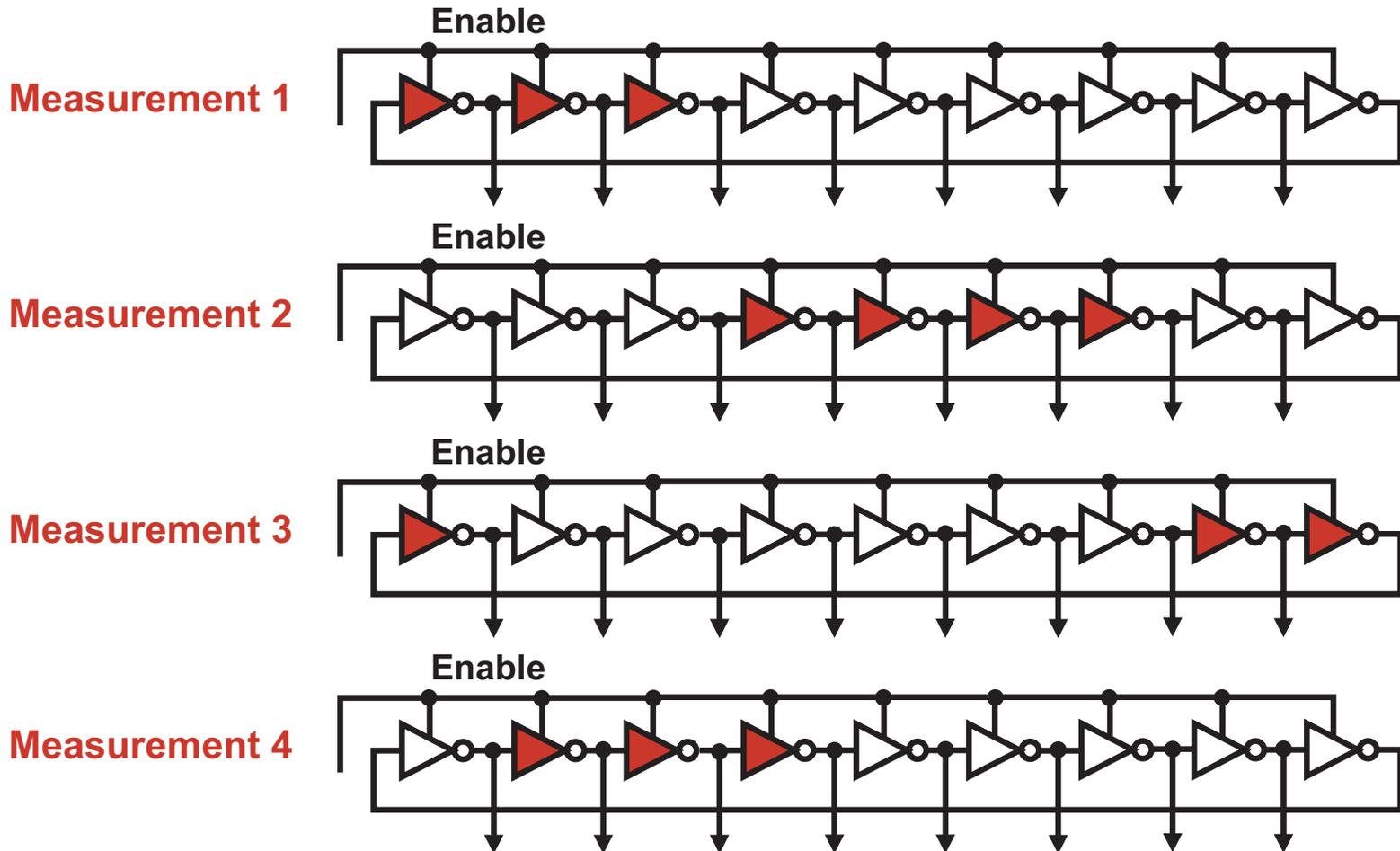
Improve Resolution By Using All Oscillator Phases



Helal, Straayer, Wei,
Perrott VLSI 2007

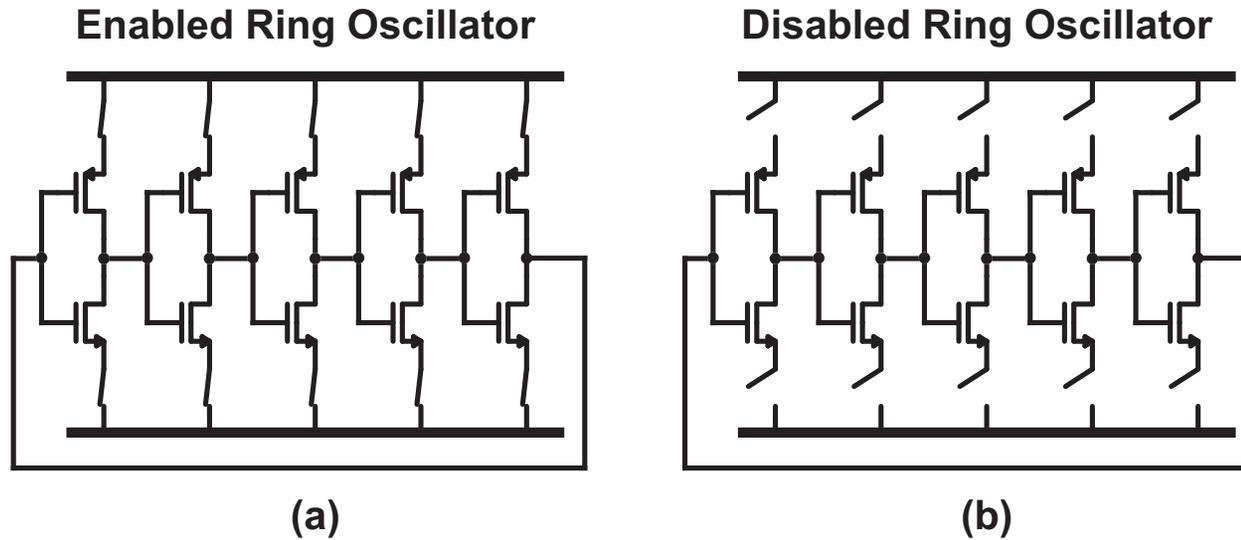
- Raw resolution is set by inverter delay
- Effective resolution is dramatically improved by averaging

GRO TDC Also Shapes Delay Mismatch

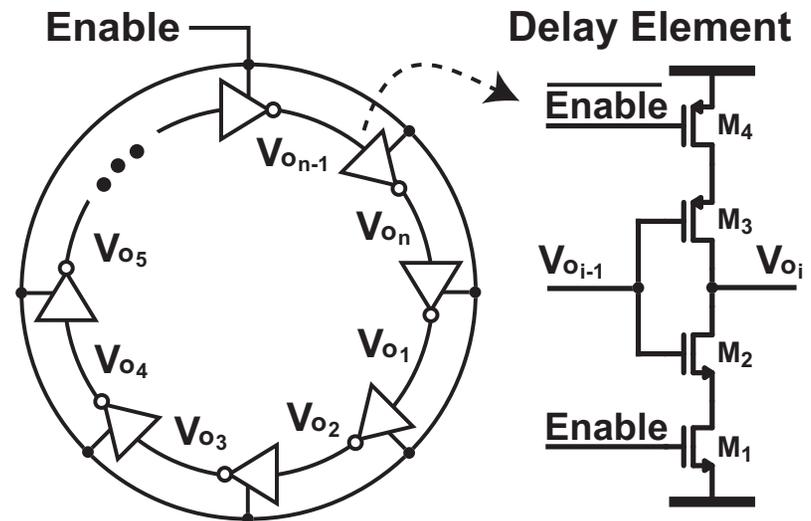


- Barrel shifting occurs through delay elements across different measurements
- Mismatch between delay elements is first order shaped!

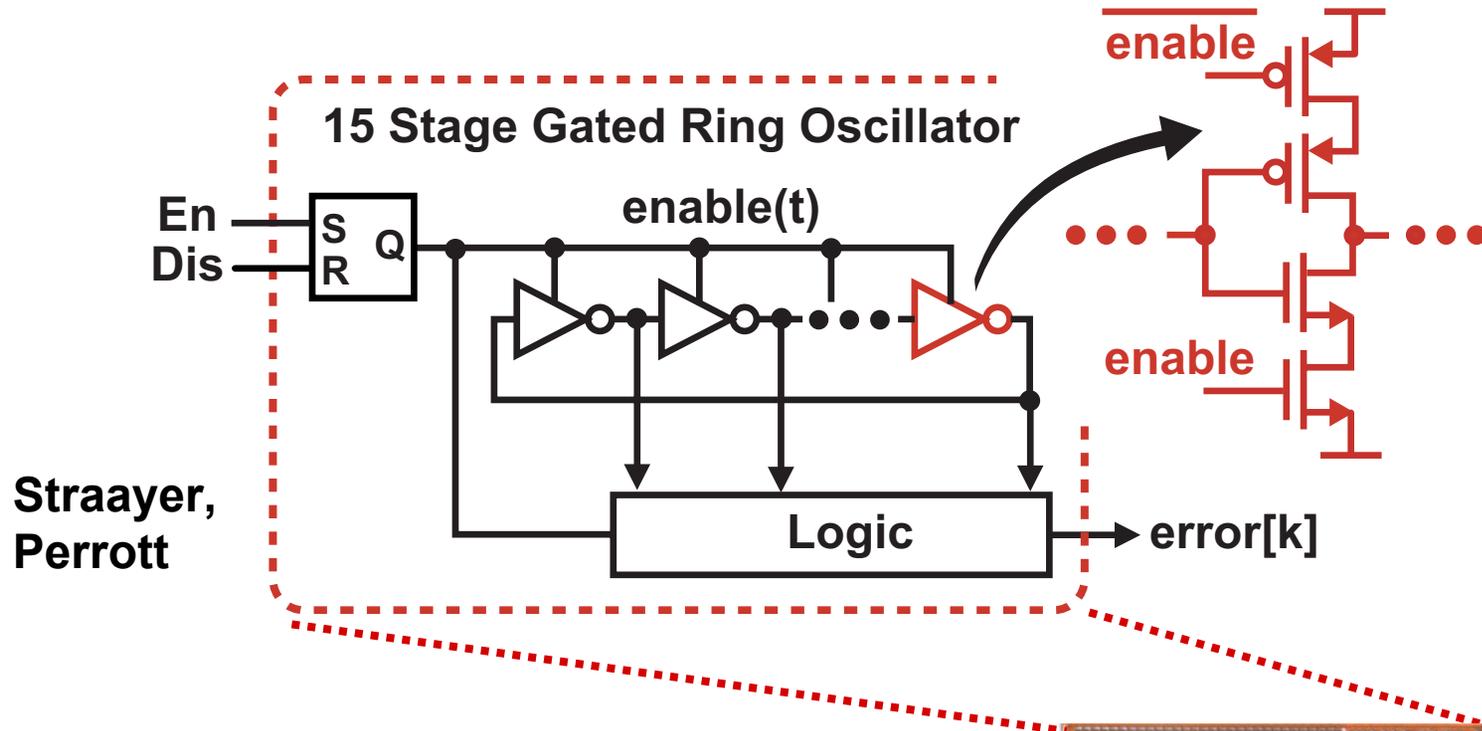
Simple gated ring oscillator inverter-based core



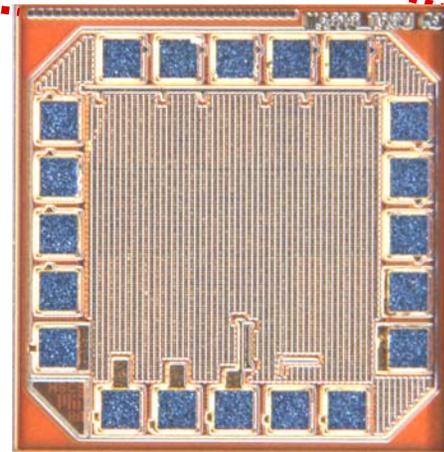
Gate the oscillator by switching the inverter cores to the power supply



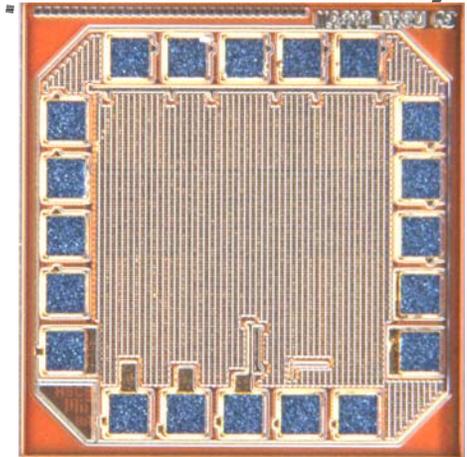
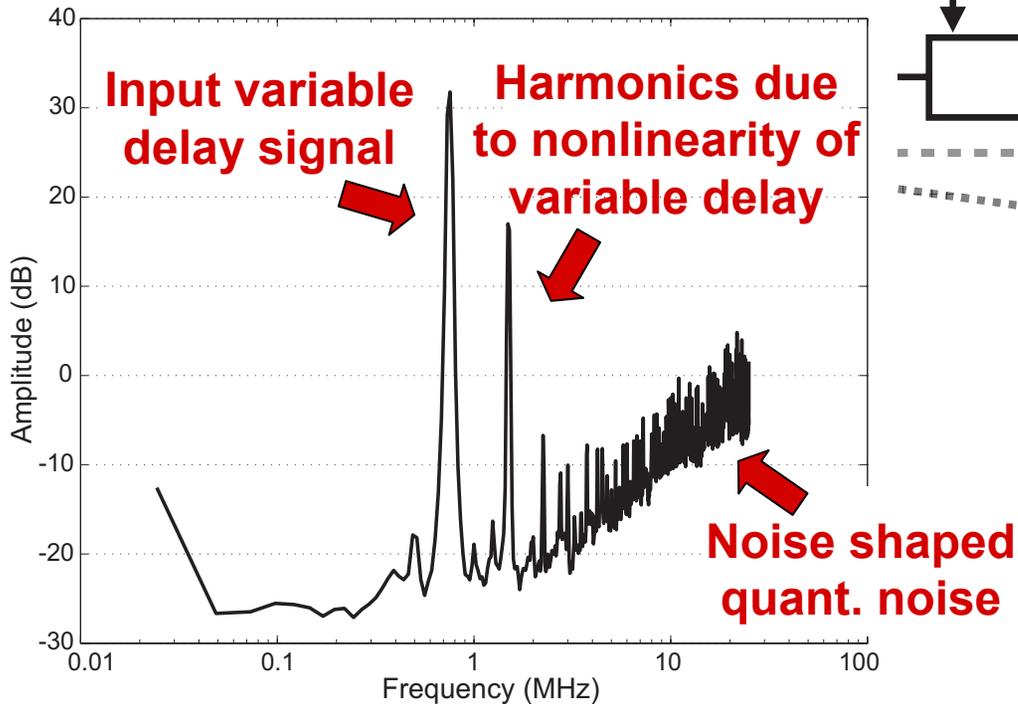
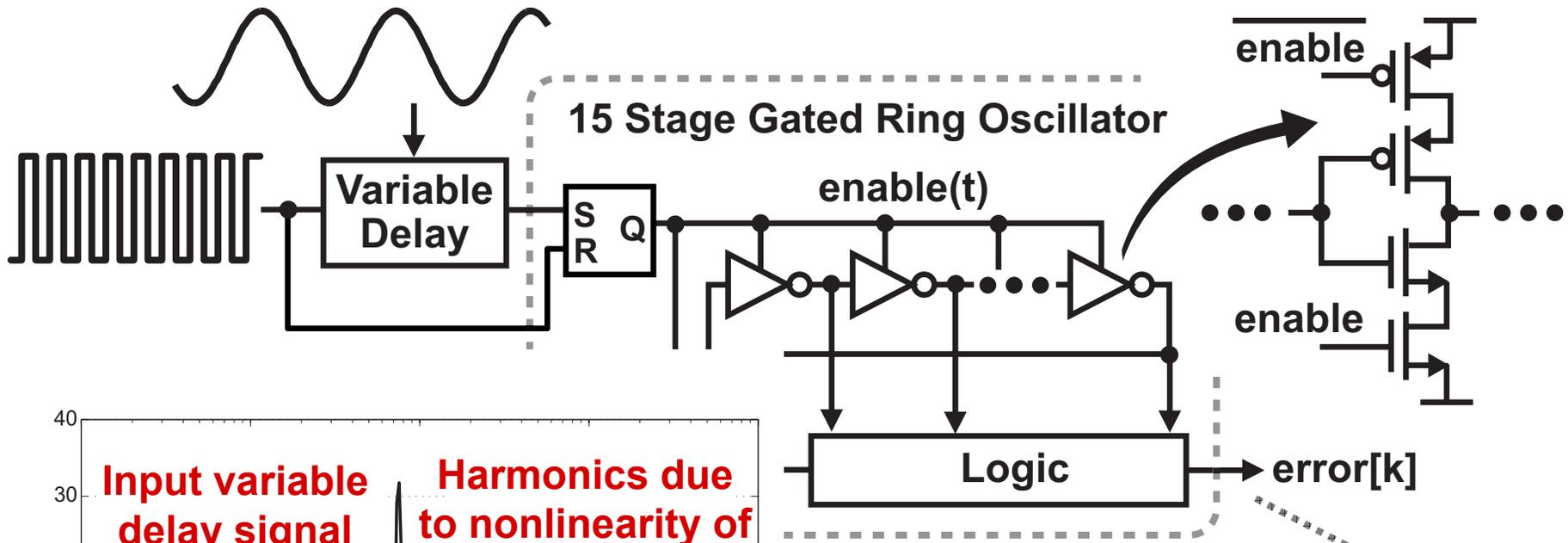
GRO Prototype



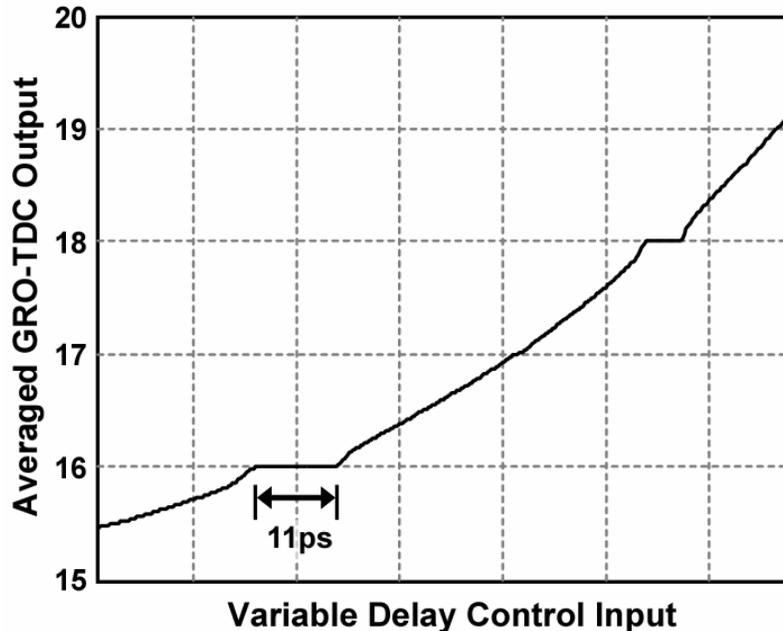
- GRO implemented as a custom 0.13 μm CMOS IC



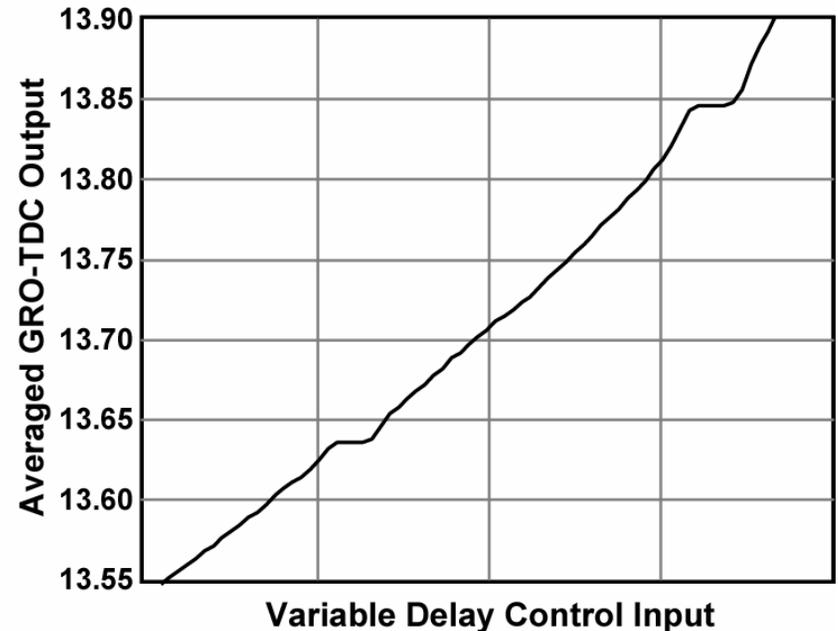
Measured GRO Results Confirm Noise Shaping



Measured deadzone behavior of inverter-based GRO



(a)

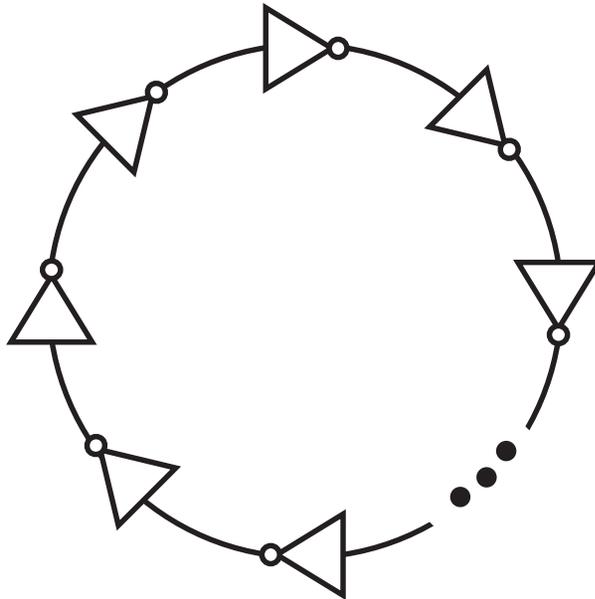


(b)

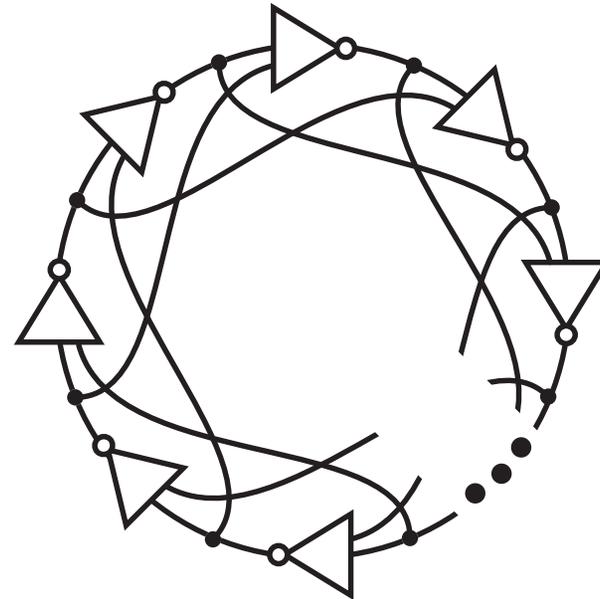
- Deadzones were caused by errors in gating the oscillator
- GRO “injection locked” to an integer ratio of F_s
- Behavior occurred for almost all integer boundaries, and some fractional values as well
- Noise shaping benefit was limited by this gating error

Next Generation GRO: Multi-path oscillator concept

Single Input
Single Output

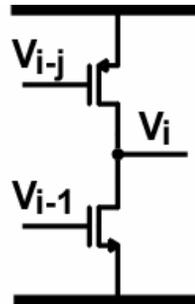


Multiple Inputs
Single Output



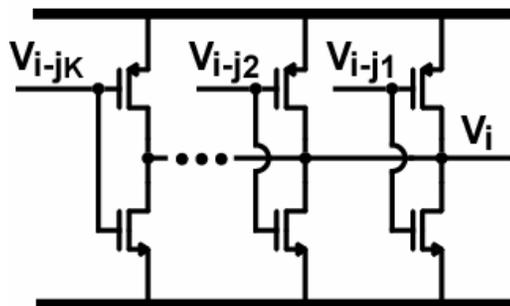
- Use multiple inputs for each delay element instead of one
- Allow each stage to optimally begin its transition based on information from the entire GRO phase state
- Key design issue is to ensure primary mode of oscillation

Multi-path inverter core



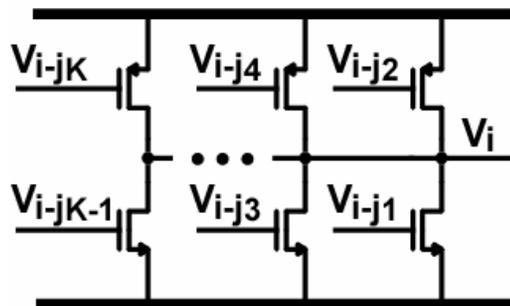
Lee, Kim, Lee
JSSC 1997

(a) Asymmetrically skewed inverter

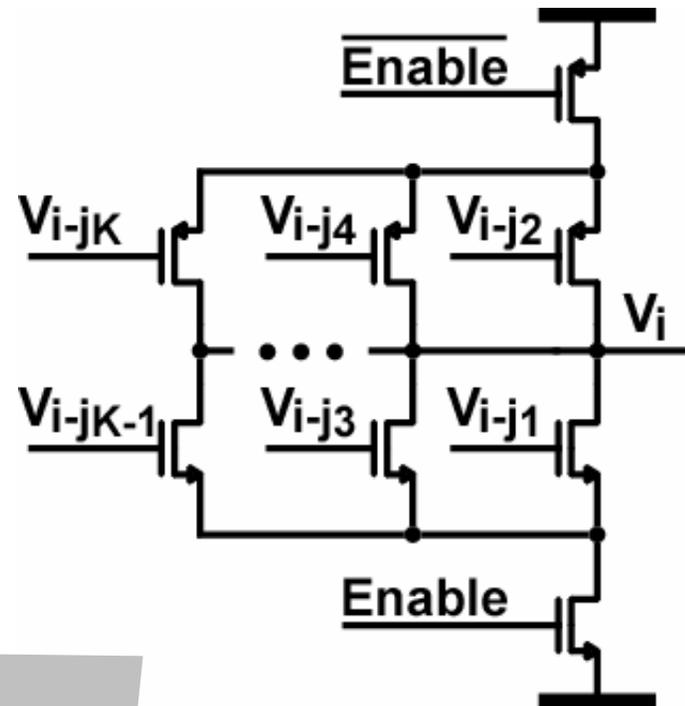


Mohan, et. al.,
CICC 2005

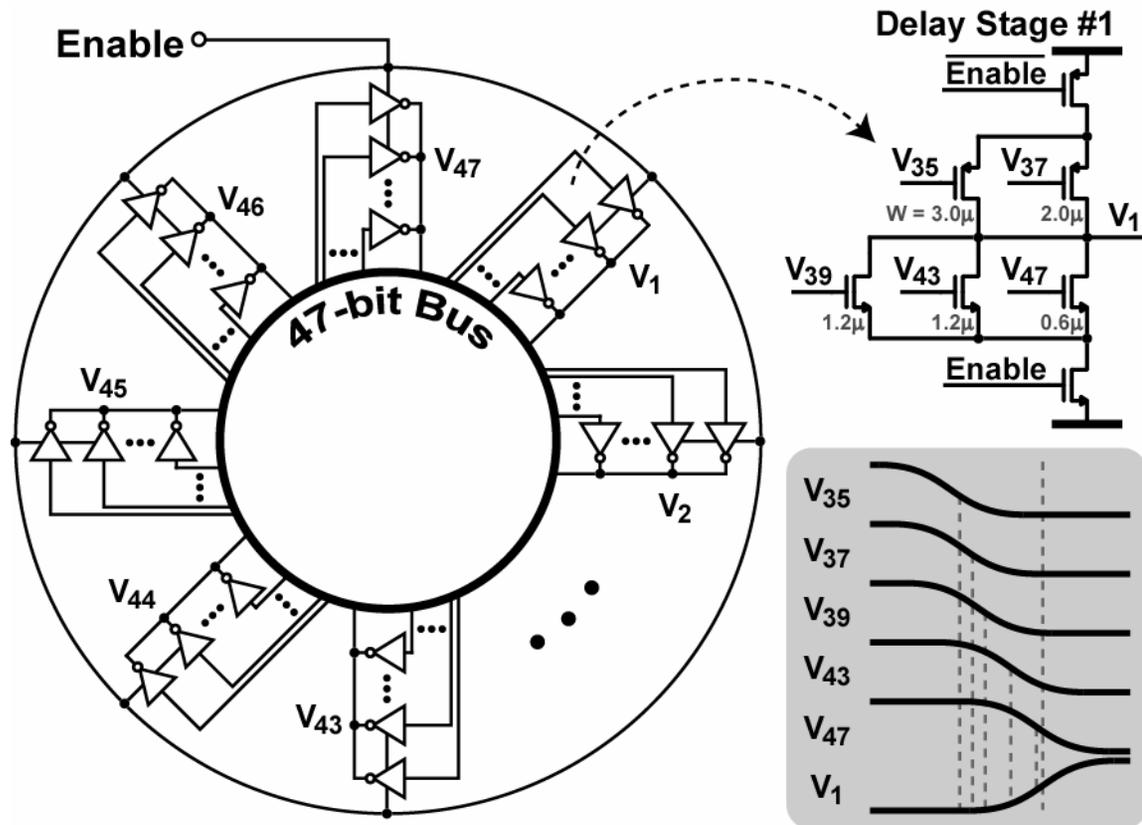
(b) Multiple skewed inverters



(c) Unrestricted connections



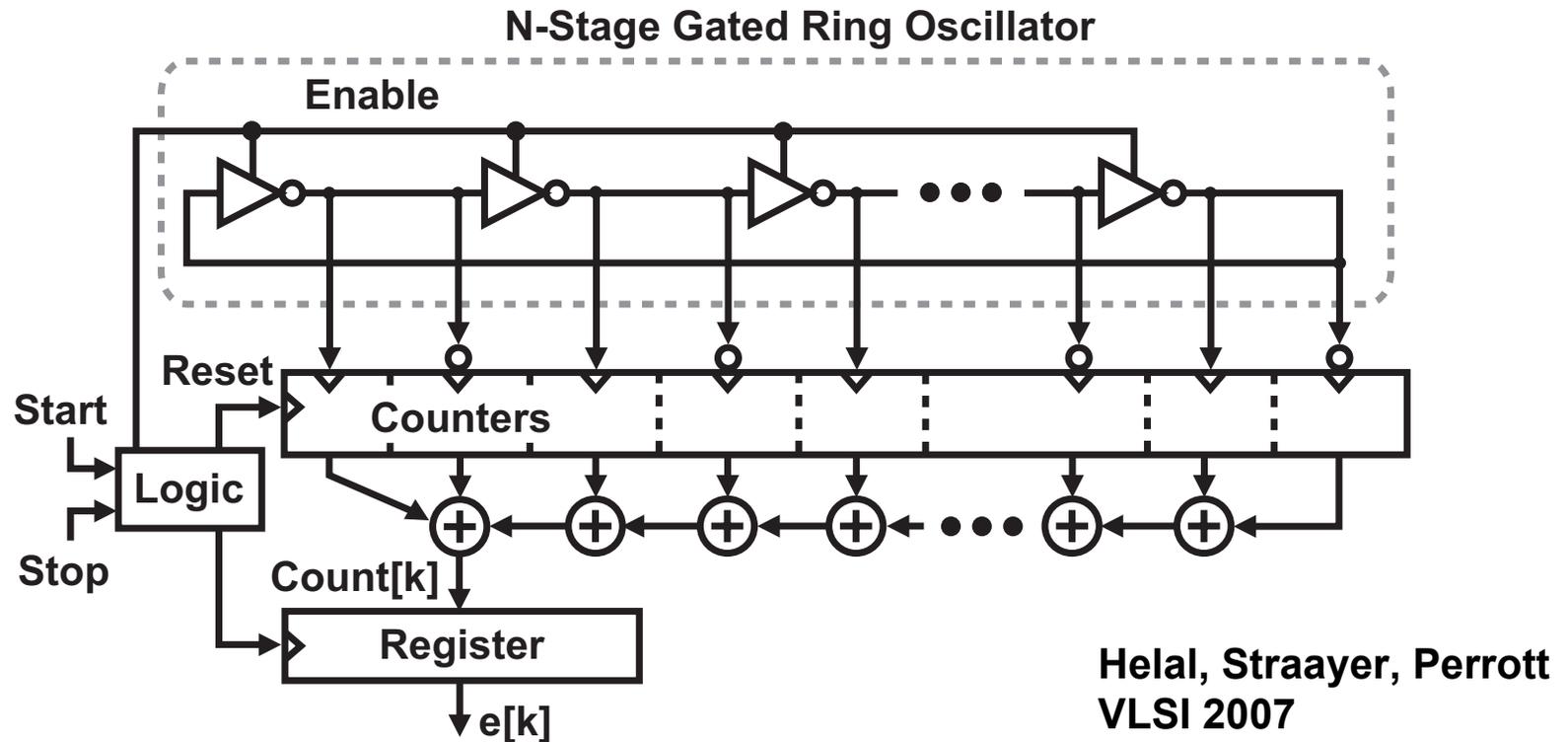
Proposed multi-path gated ring oscillator



Hsu, Straayer, Perrott
ISSCC 2008

- Oscillation frequency near 2GHz with 47 stages...
- Reduces effective delay per stage by a factor of 5-6!
- Represents a factor of 2-3 improvement compared to previous multi-path oscillators

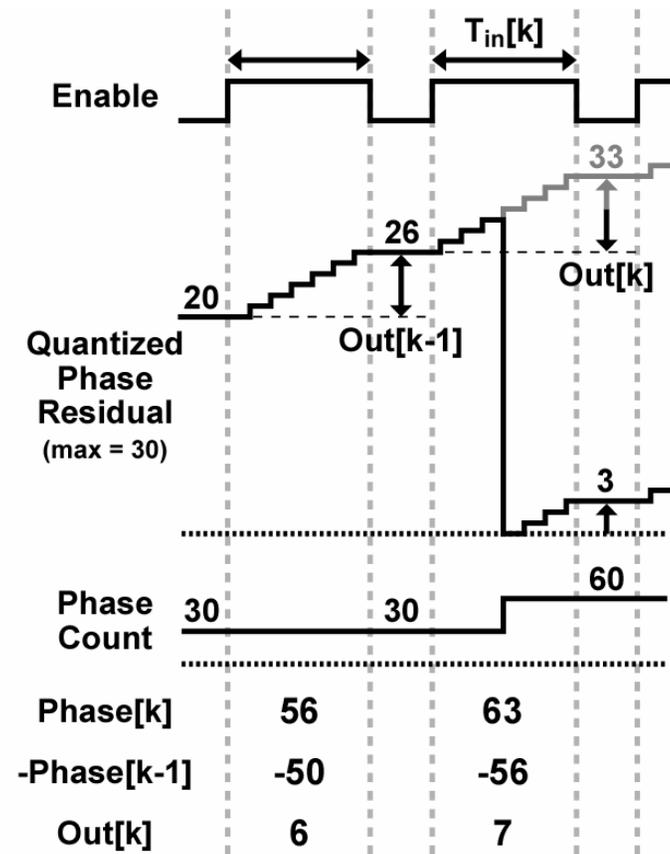
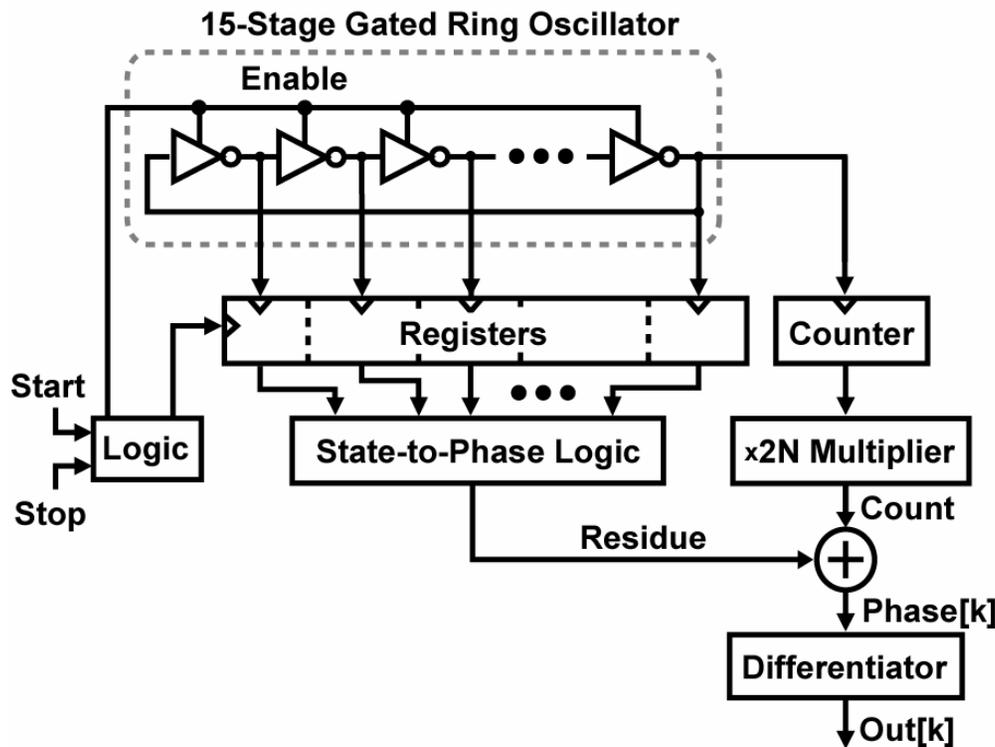
A simple measurement approach...



- 2 counters per stage * 47 stages = 94 counters each at 2GHz
- Power consumption for these counters is unreasonable

Need a more efficient way to measure the multi-path GRO

Count Edges by Sampling Phase

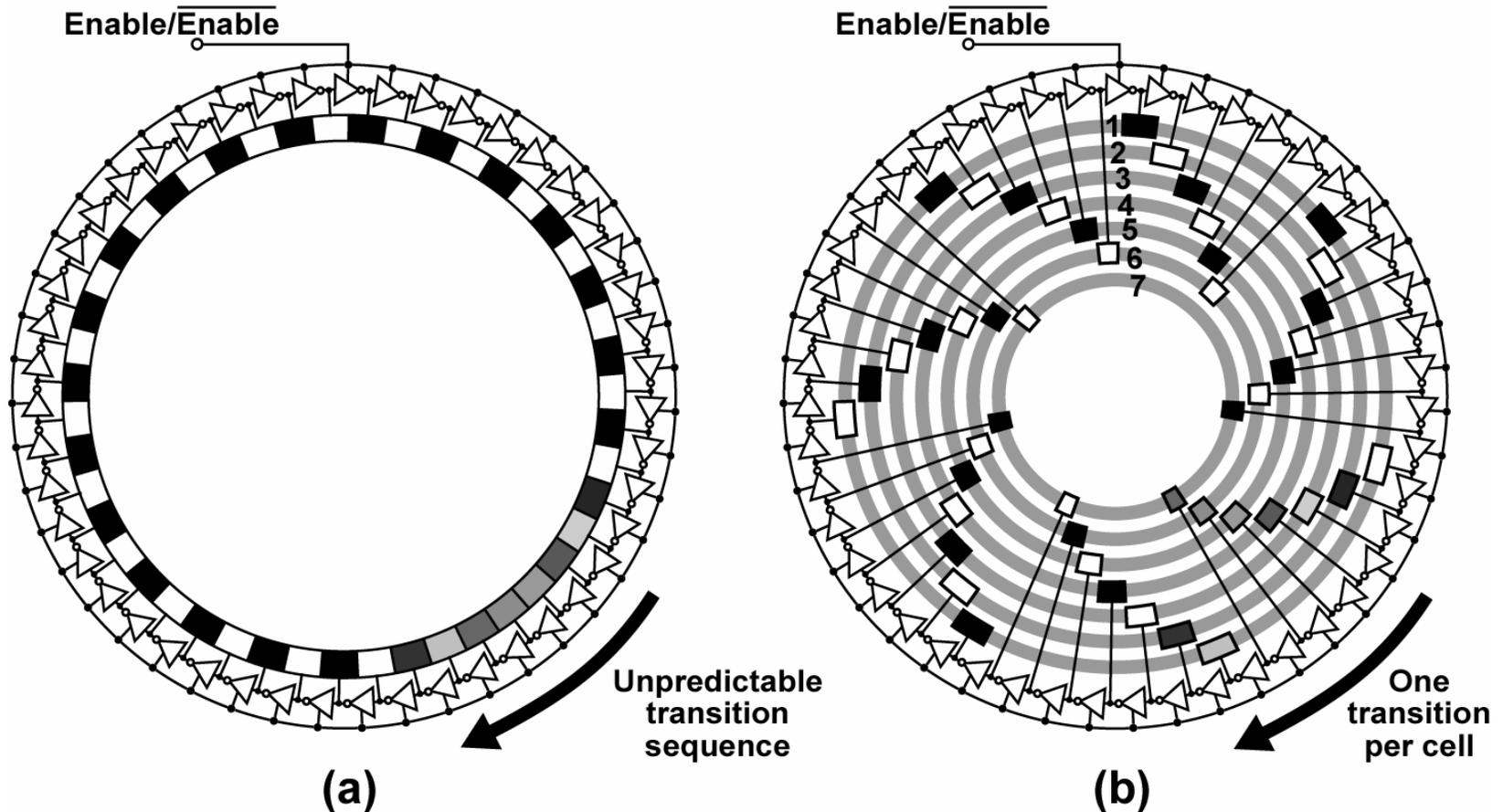


- Calculate phase from:

- A single counter for coarse phase information (keeps track of phase wrapping)
- GRO phase state for fine count information

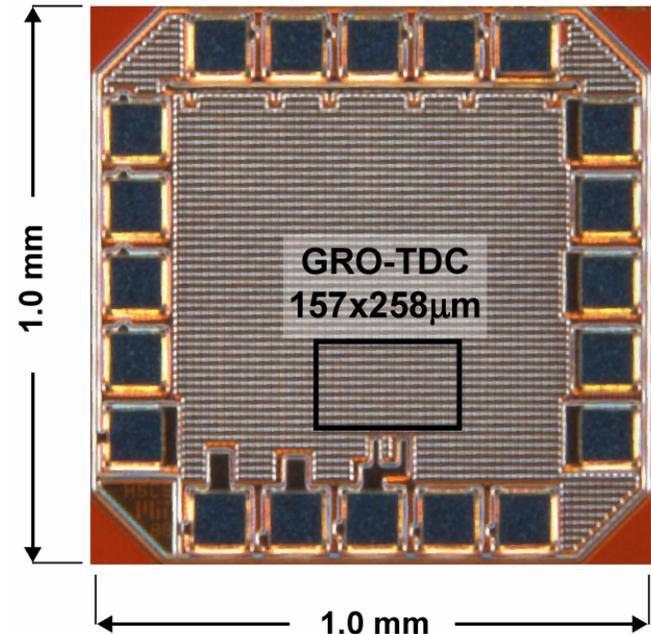
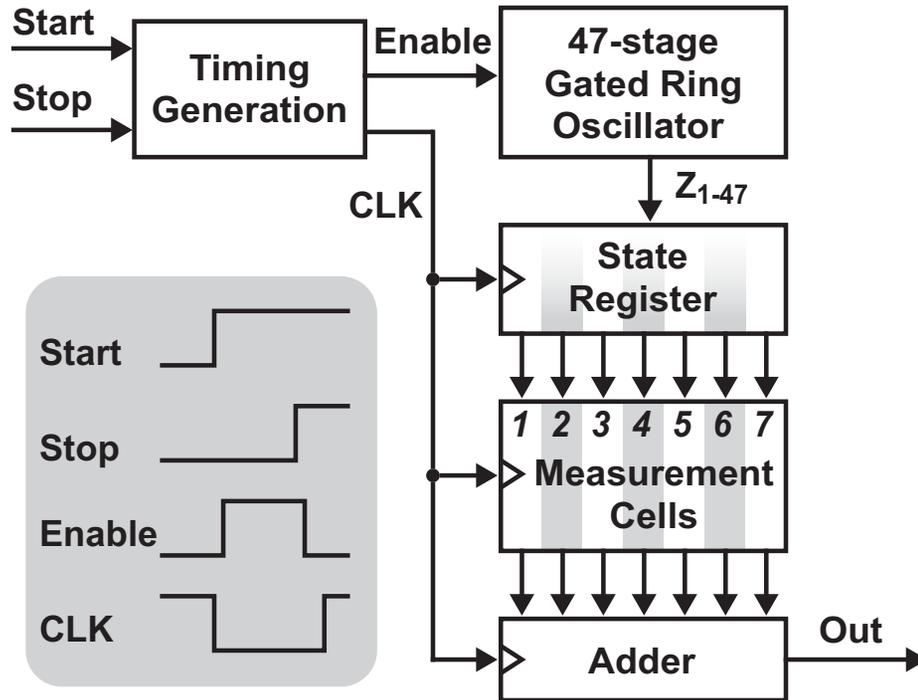
- 1 counter and N registers → much more efficient

Proposed Multi-Path Measurement Structure



- Multi-path structure leads to ambiguity in edge position
- Partition into 7 cells to avoid such ambiguity
 - Requires 7 counters rather than 1, but power still OK

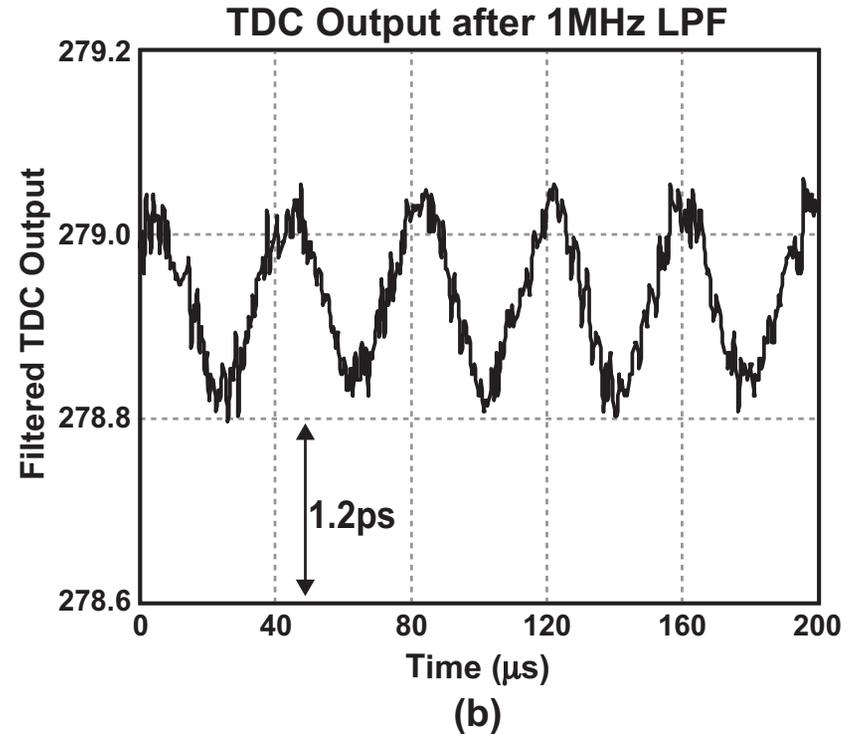
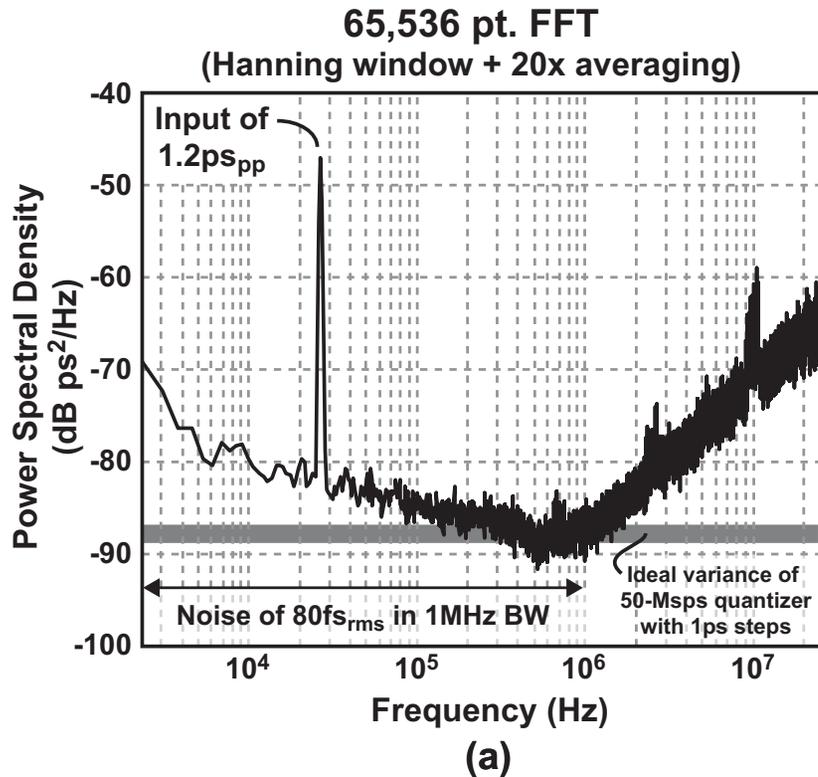
Prototype 0.13 μm CMOS multi-path GRO-TDC



Straayer et al., VLSI 2008

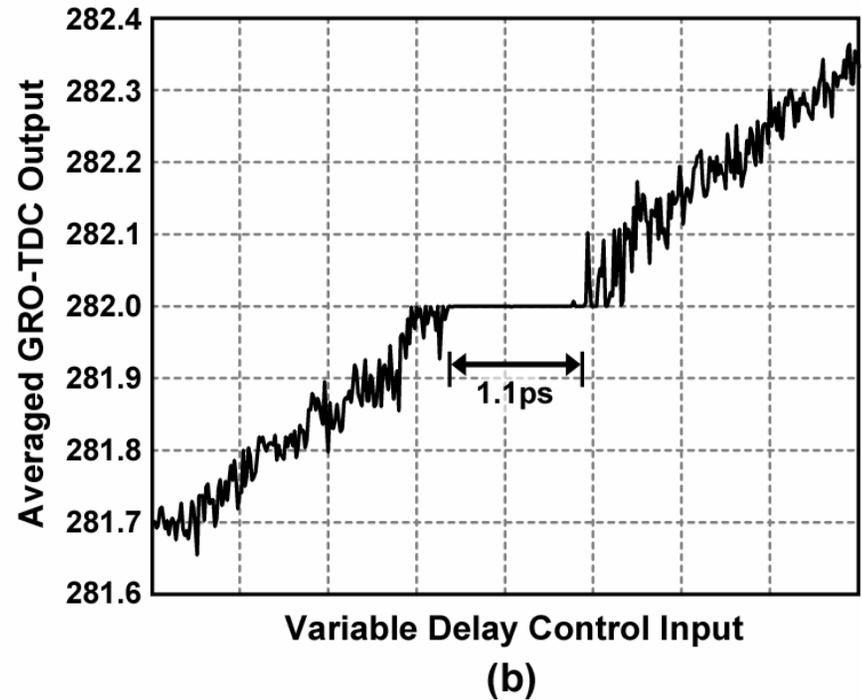
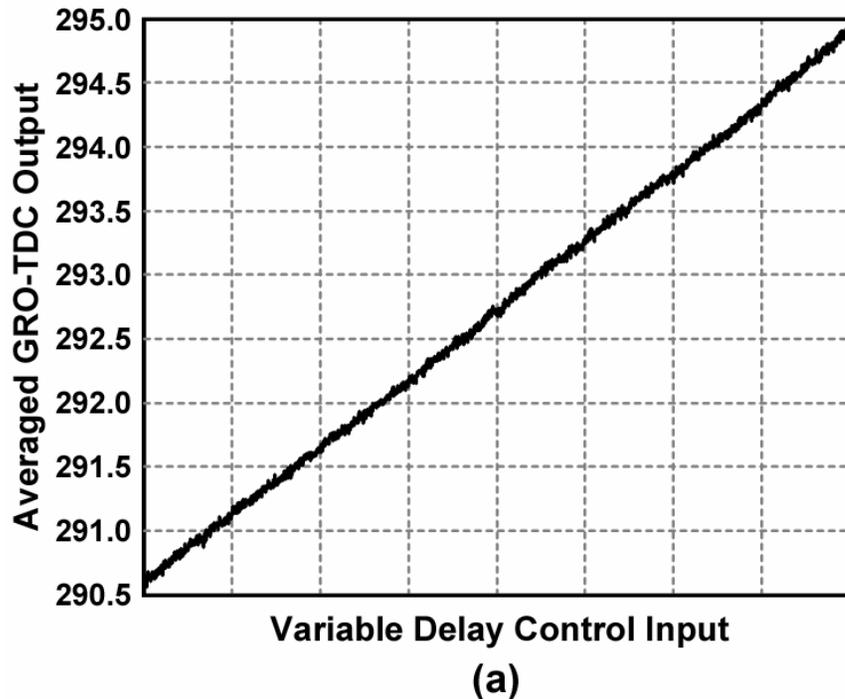
- **Two implemented versions:**
 - 8-bit, 500MSPs
 - 11-bit, 100MSPs version
- **2-21mW power consumption depending on input duty cycle**

Measured noise-shaping of multi-path GRO



- Data collected at 50Mps
- More than 20dB of noise-shaping benefit
- 80fs_{rms} integrated error from 2kHz-1MHz
- Floor primarily limited by 1/f noise (up to 0.5-1MHz)

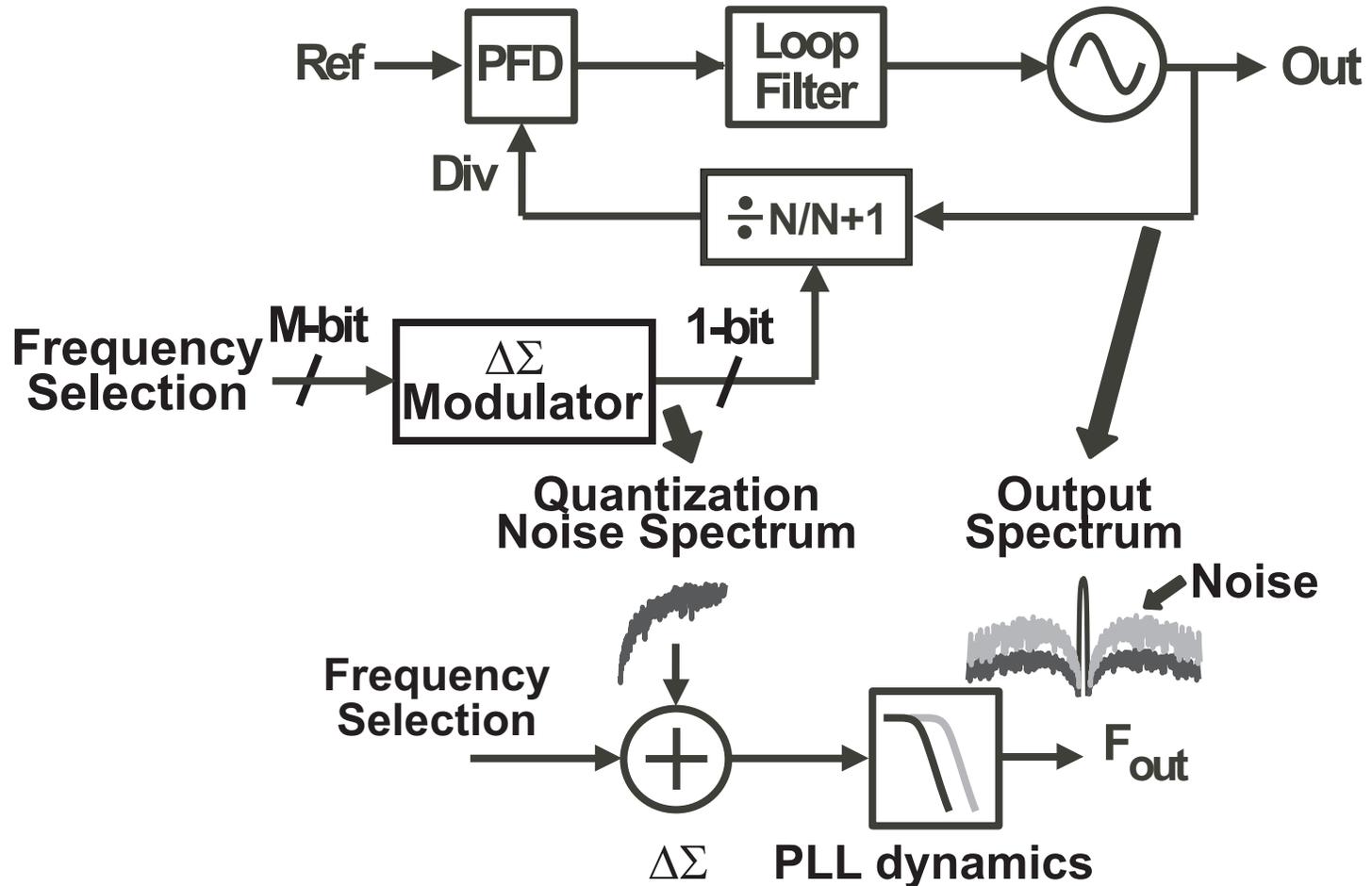
Measured deadzone behavior for multi-path GRO



- Only deadzones for outputs that are multiples of $2N$
 - 94, 188, 282, etc.
 - No deadzones for other even or odd integers, fractional output
- Size of deadzone is reduced by 10x

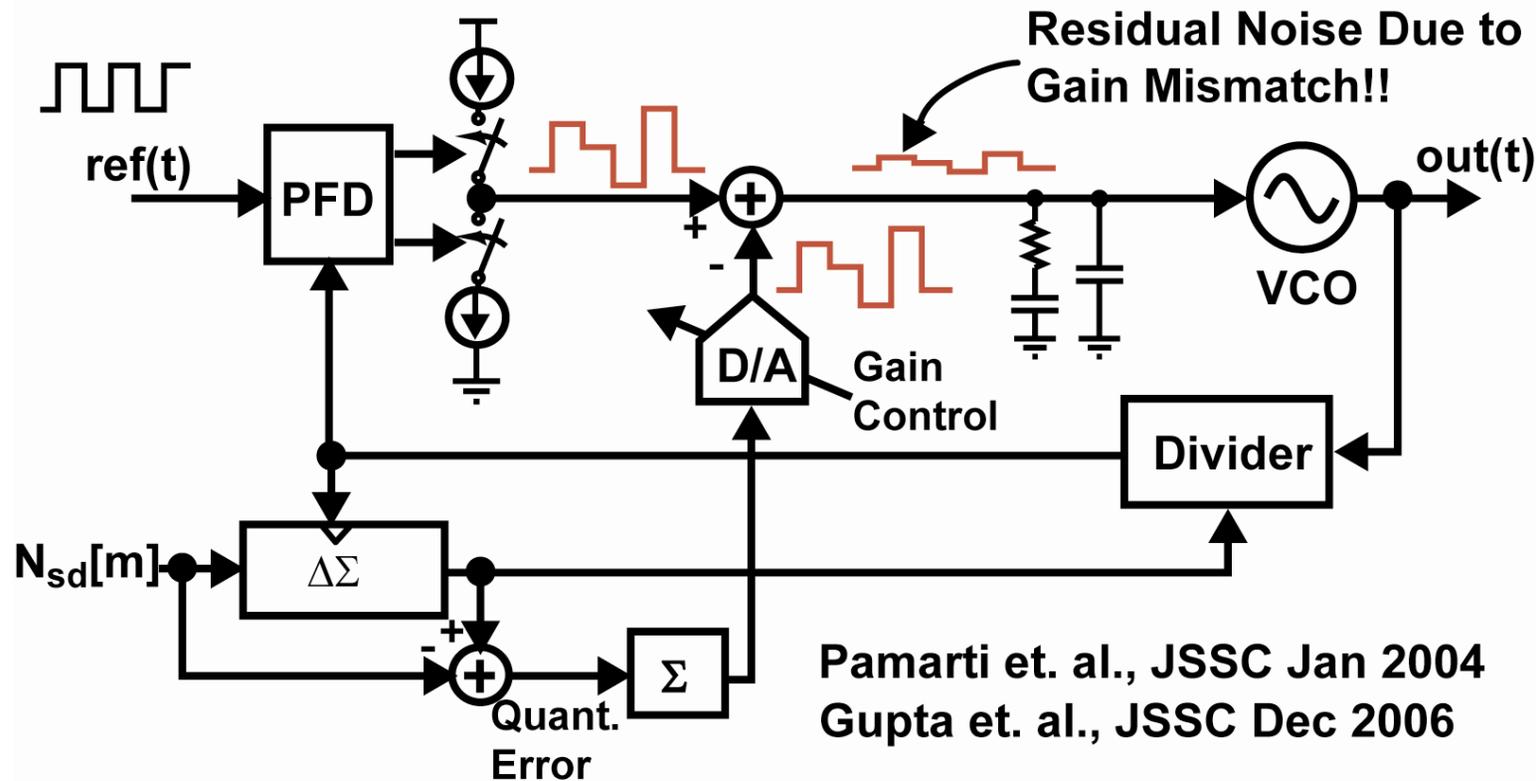
***The Issue of Quantization Noise Due to
Divider Dithering***

The Nature of the Quantization Noise Problem



- Increasing PLL bandwidth increases impact of $\Delta\Sigma$ fractional-N noise
 - Cancellation offers a way out!

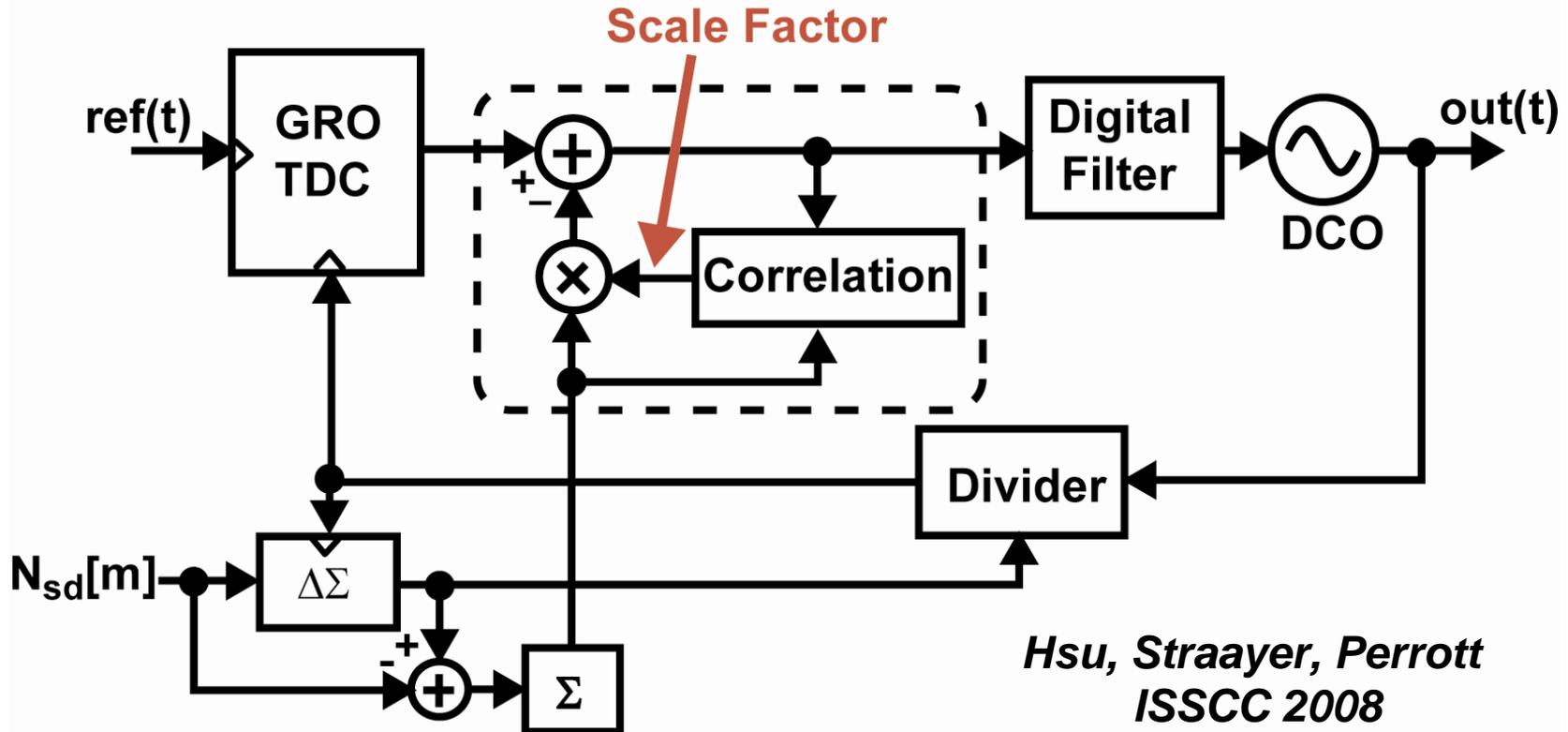
Previous Analog Quantization Noise Cancellation



- Phase error due to $\Delta\Sigma$ is predicted by accumulating $\Delta\Sigma$ quantization error
- Gain matching between PFD and D/A must be precise

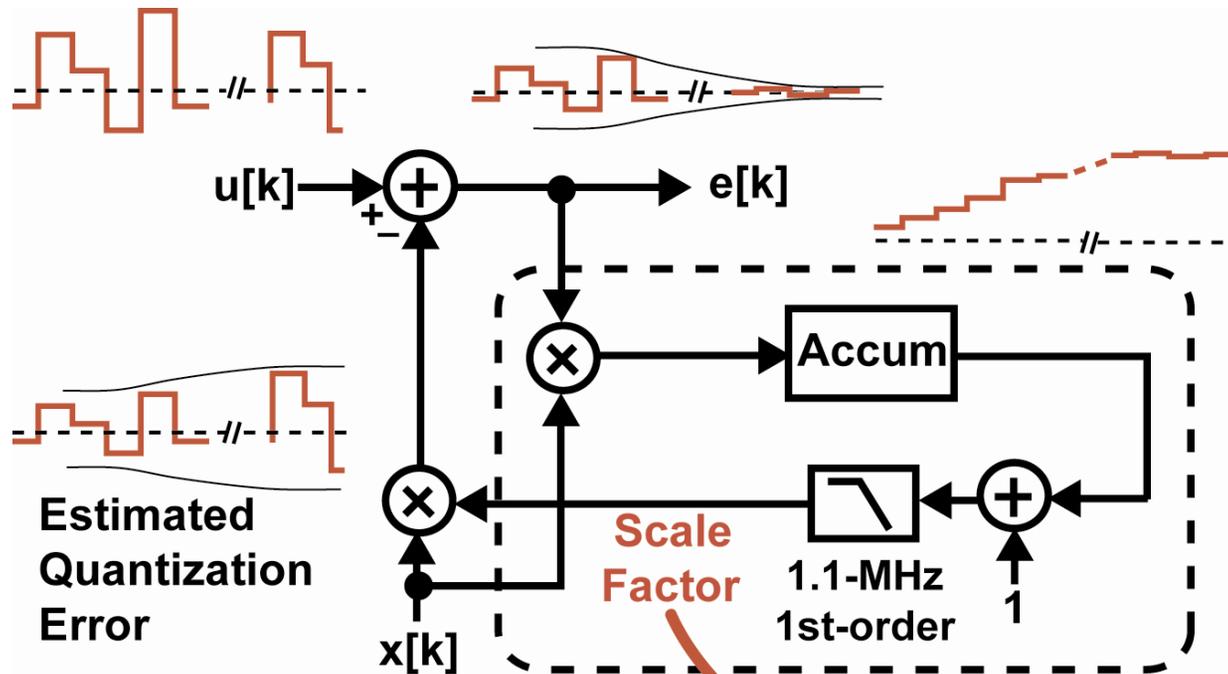
Matching in *analog* domain limits performance

Proposed All-digital Quantization Noise Cancellation

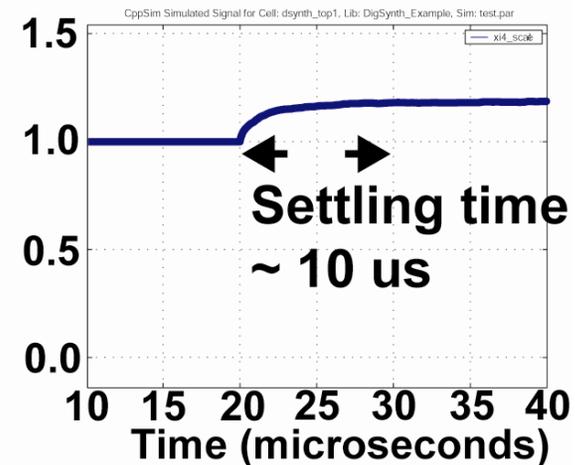


- Scale factor determined by simple digital correlation
- Analog non-idealities such as DC offset are completely eliminated

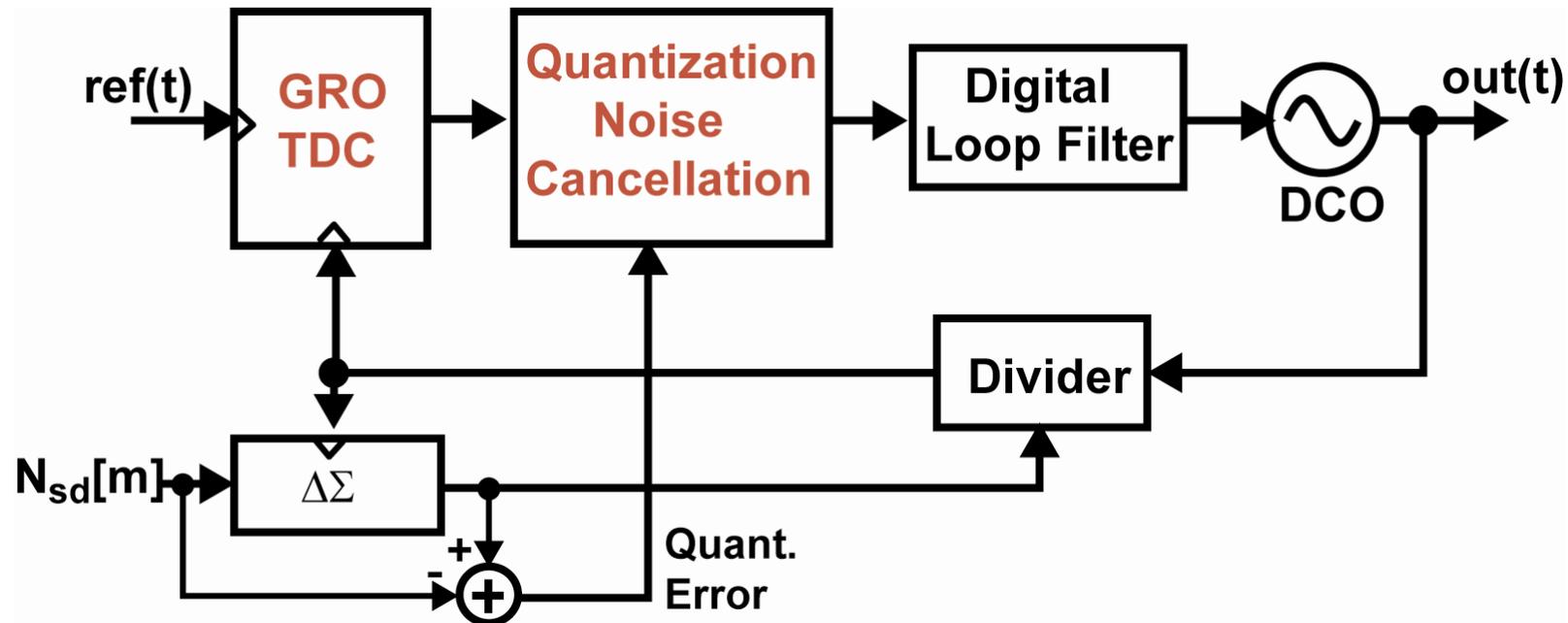
Details of Proposed Quantization Noise Cancellation



- Correlator out is accumulated and filtered to achieve scale factor
 - Settling time chosen to be around 10 us
- See *analog* version of this technique in *Swaminathan et.al., ISSCC 2007*

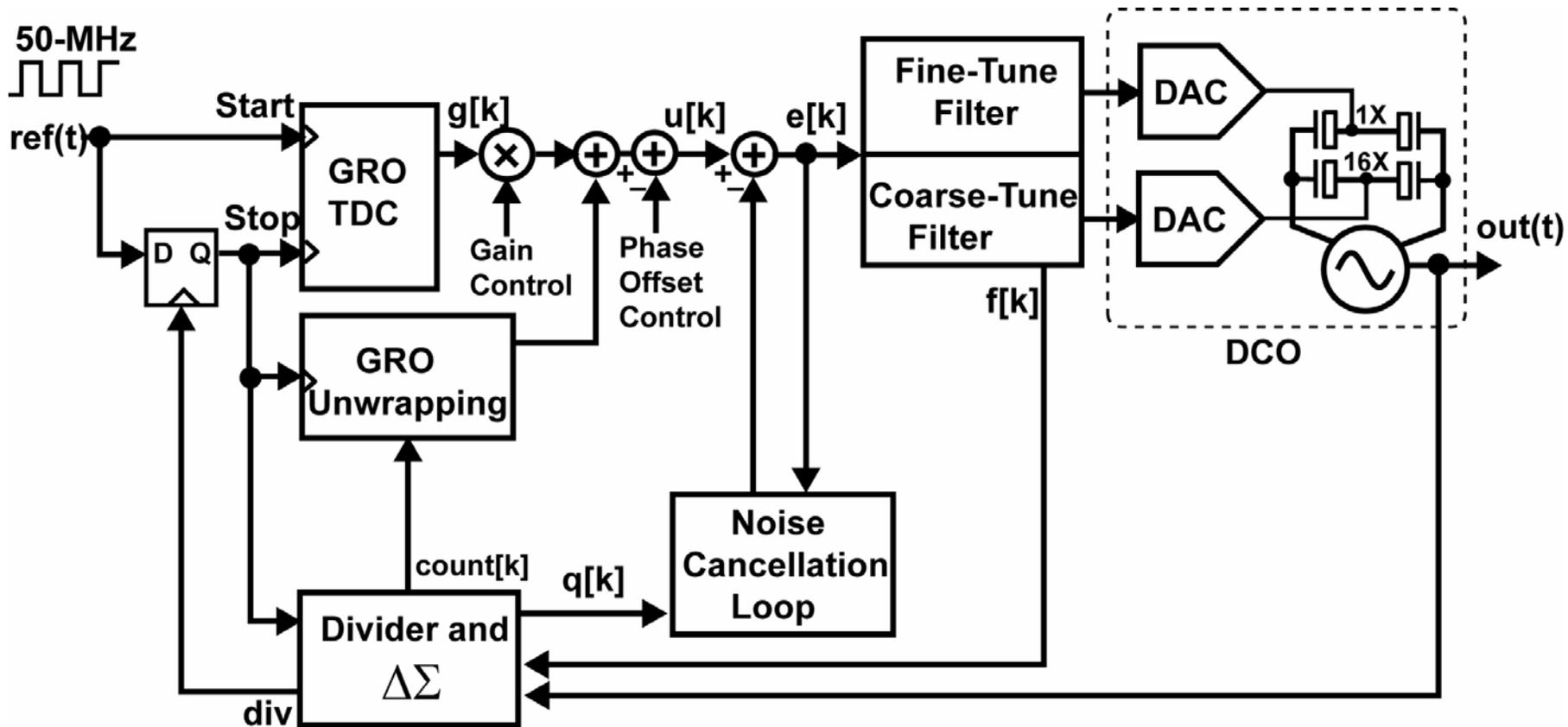


Proposed Digital Wide BW Synthesizer



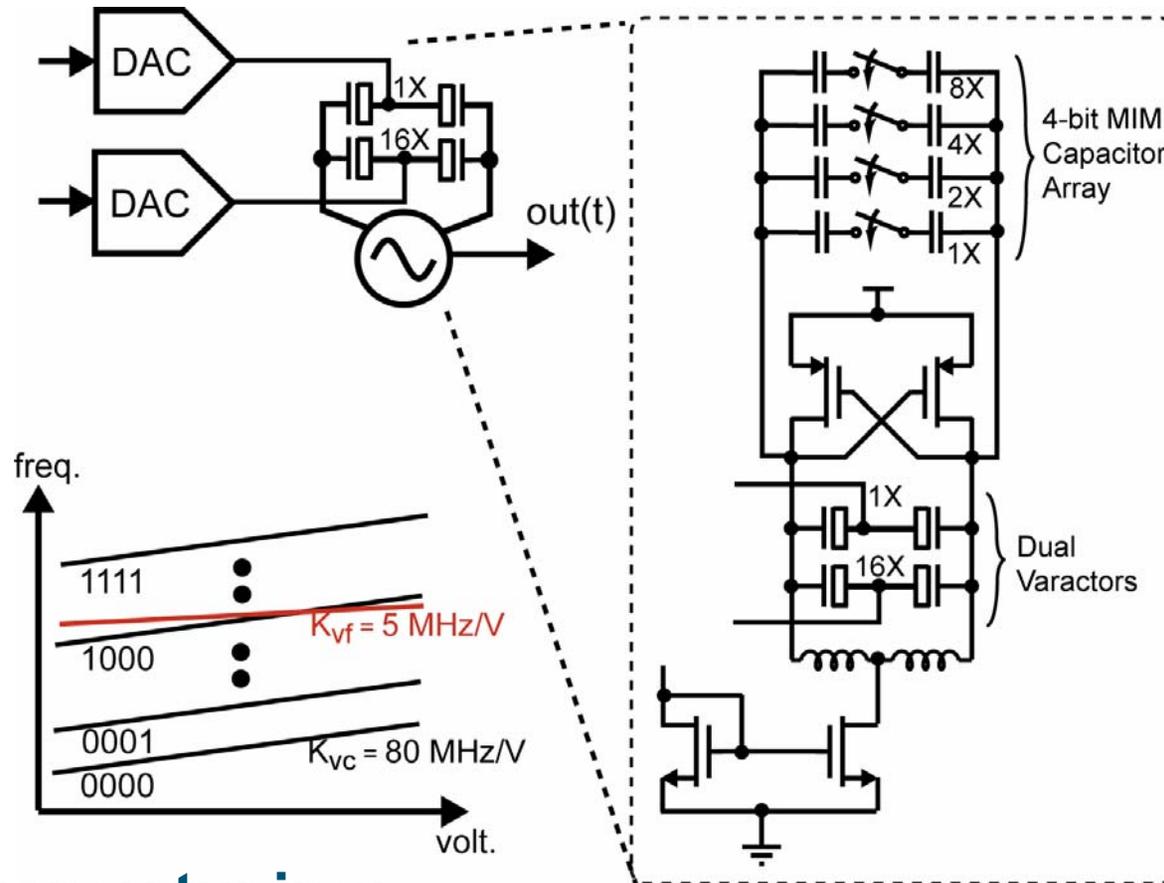
- **Gated-ring-oscillator (GRO) TDC** achieves low in-band noise
- **All-digital quantization noise cancellation** achieves low out-of-band noise
- **Design goals:**
 - 3.6-GHz carrier, 500-kHz bandwidth
 - $<-100\text{dBc/Hz}$ in-band, $<-150\text{ dBc/Hz}$ at 20 MHz offset

Overall Synthesizer Architecture



Note: Detailed behavioral simulation model available at <http://www.cppsim.com>

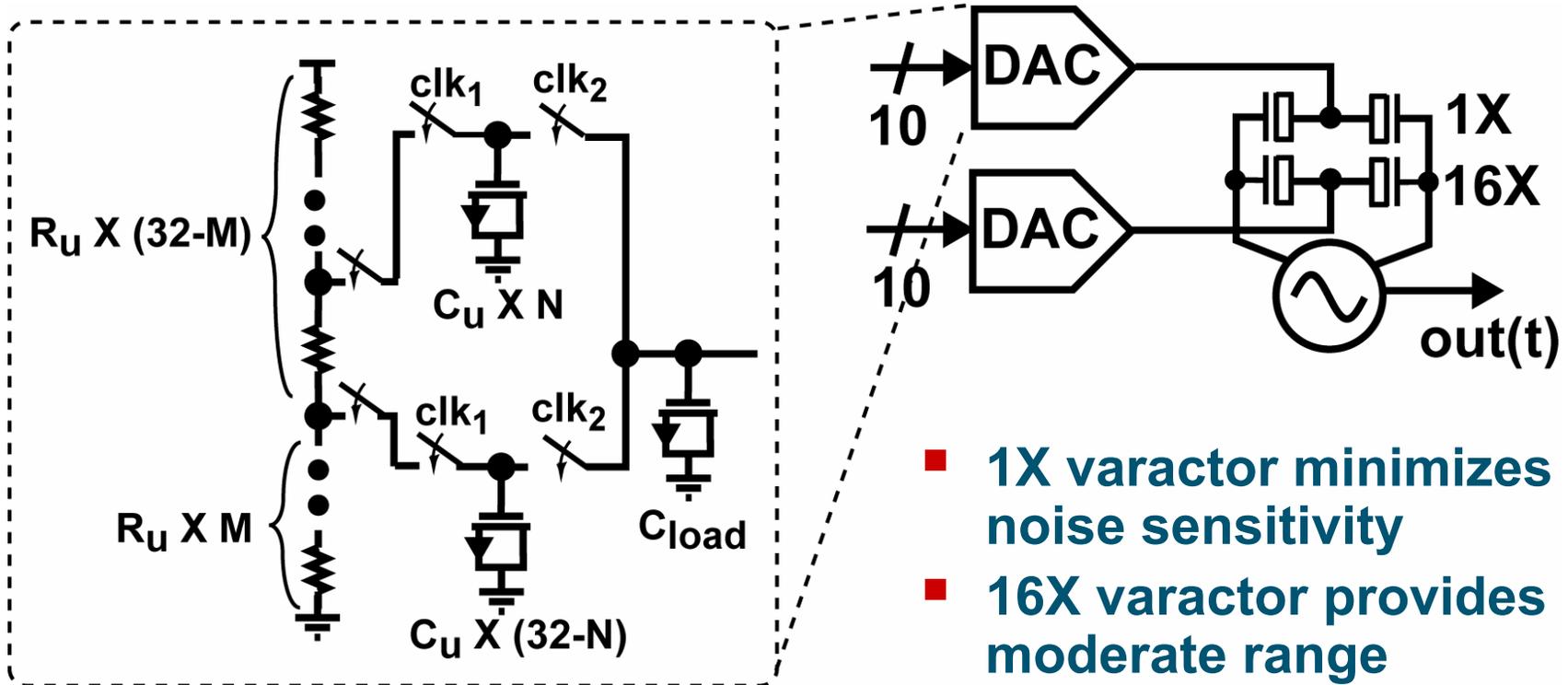
Dual-Port LC VCO



■ Frequency tuning:

- Use a small 1X varactor to minimize noise sensitivity
- Use another 16X varactor to provide moderate range
- Use a four-bit capacitor array to achieve 3.3-4.1 GHz range

Digitally-Controlled Oscillator with Passive DAC

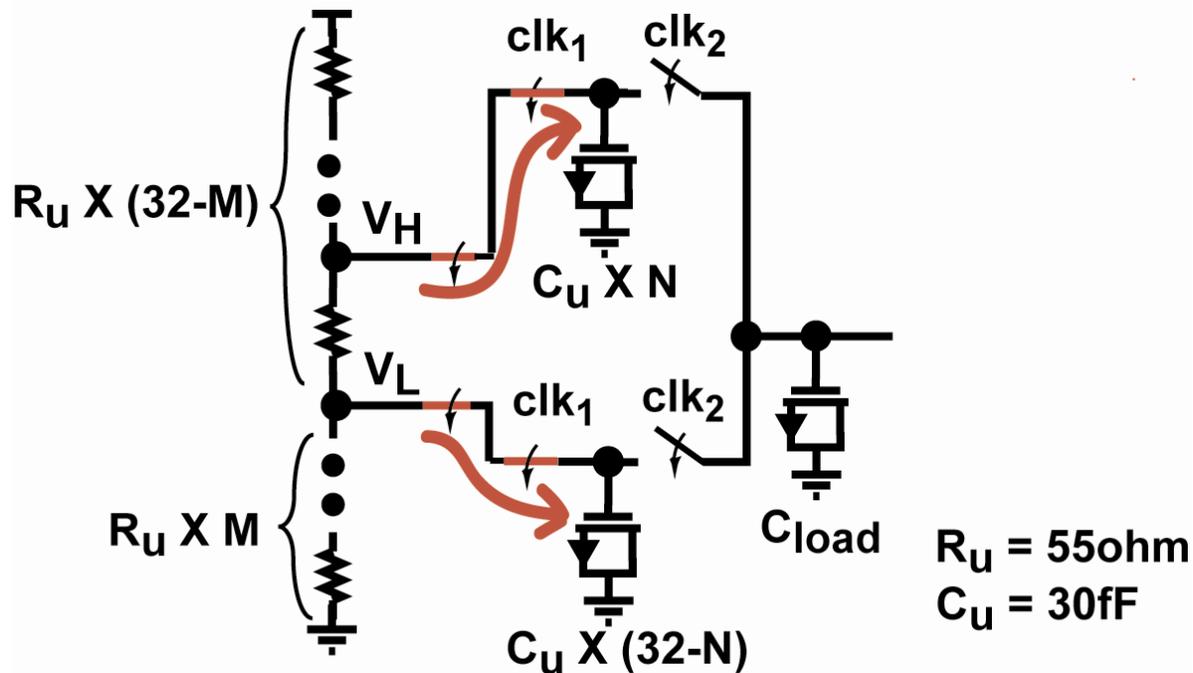


- **Goals of 10-bit DAC**

- Monotonic
- Minimal active circuitry and no transistor bias currents
- Full-supply output range

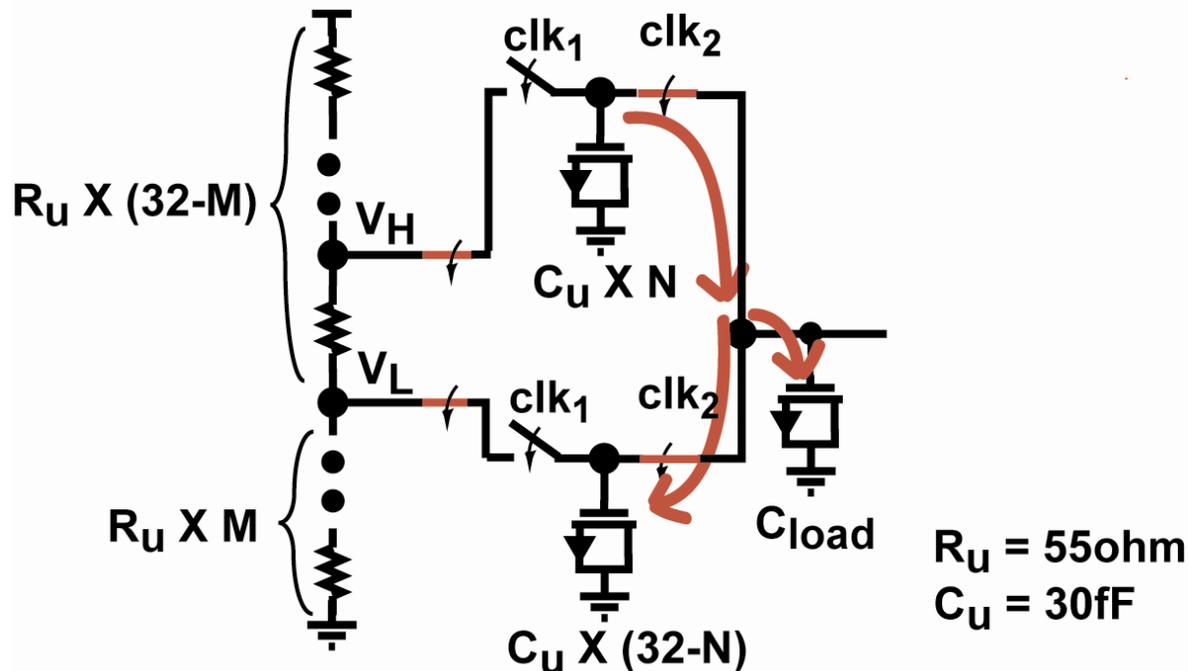
- **1X varactor minimizes noise sensitivity**
- **16X varactor provides moderate range**
- **A four-bit capacitor array covers 3.3-4.1GHz**

Operation of 10-bit Passive DAC (Step 1)



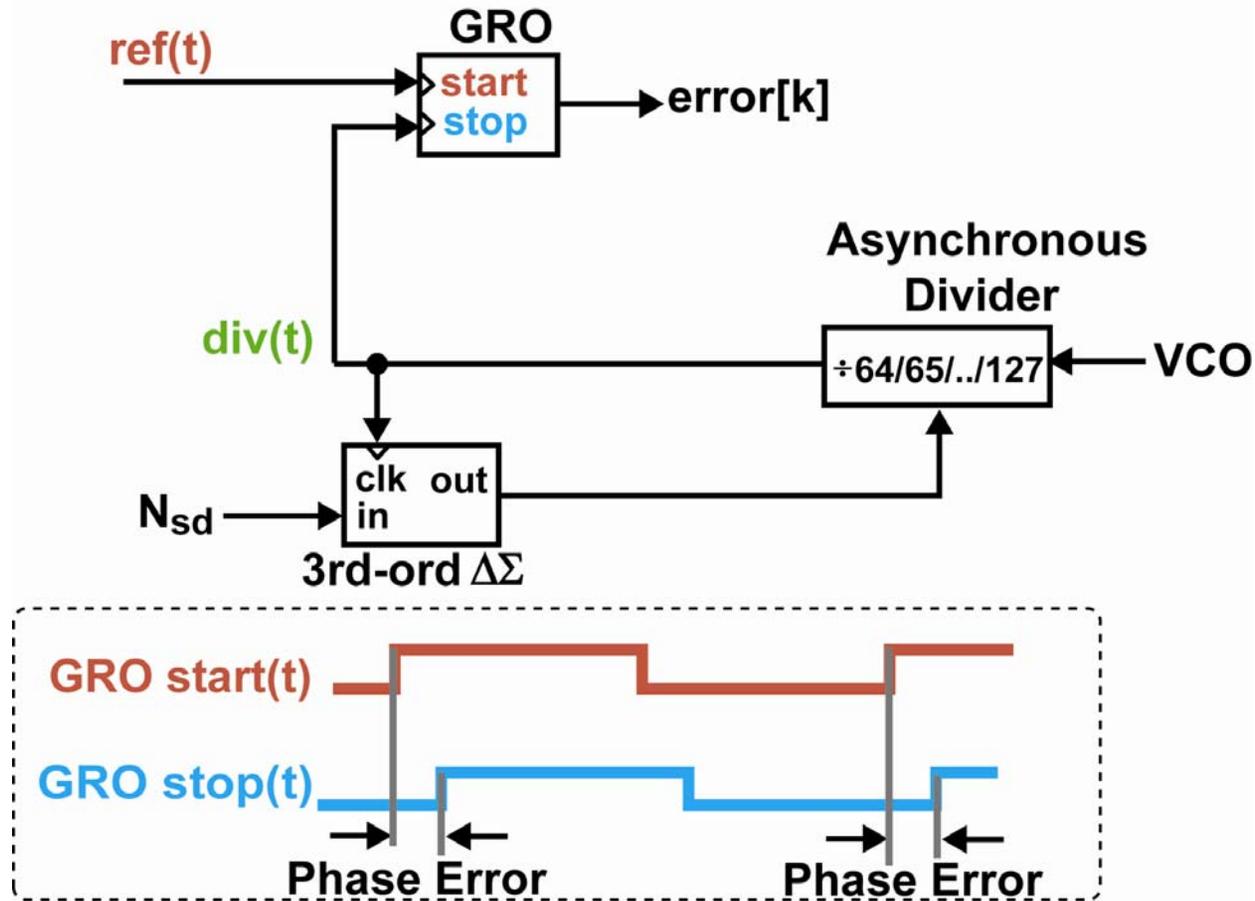
- 5-bit resistor ladder; 5-bit switch-capacitor array
- Step 1: *Capacitors Charged*
 - Resistor ladder forms $V_L = M/32 \cdot V_{DD}$ and $V_H = (M+1)/32 \cdot V_{DD}$, where M ranges from 0 to 31
 - N unit capacitors charged to V_H , and $(32-N)$ unit capacitors charged to V_L

Operation of 10-bit Passive DAC (Step 2)



- **Step 2: Disconnect Capacitors from Resistors, Then Connect Together**
 - Achieves DAC output with first-order filtering
 - Bandwidth = $32 \cdot C_u / (2\pi \cdot C_{load}) \cdot 50\text{MHz}$
 - Determined by capacitor ratio
 - Easily changed by using different C_{load}

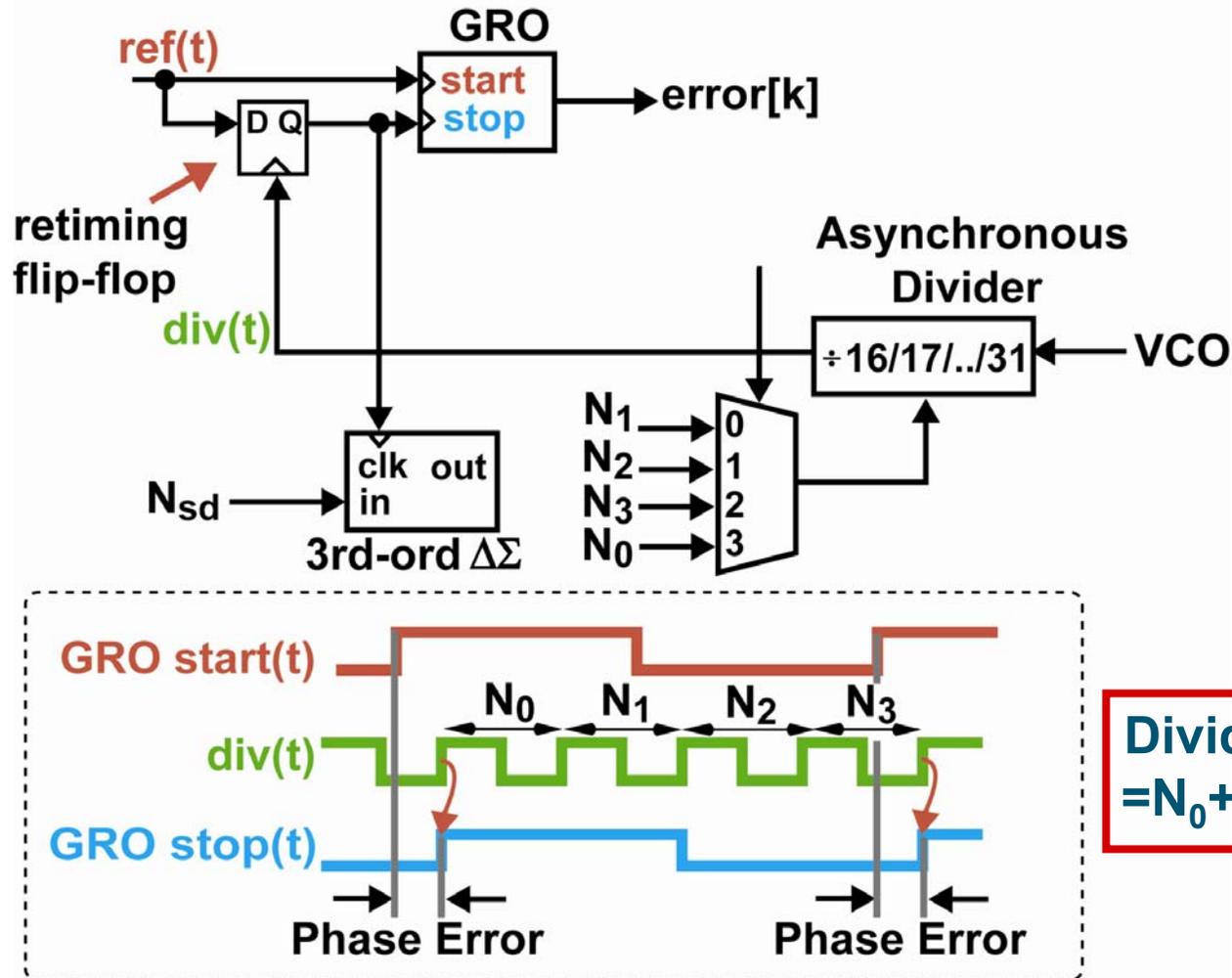
Now Let's Examine Divider ...



■ Issues:

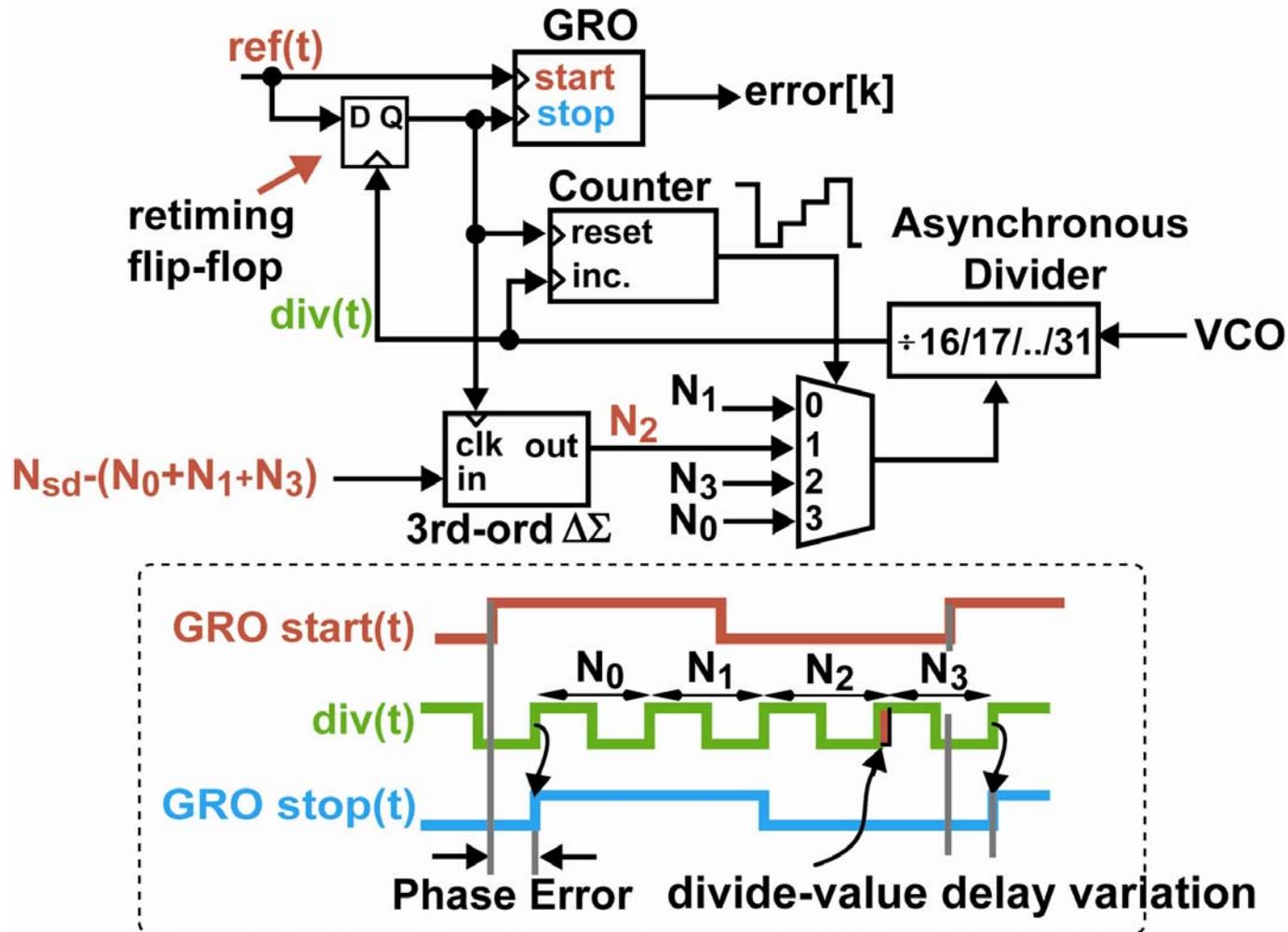
- GRO range must span entire reference period during initial lock-in

Proposed Divider Structure



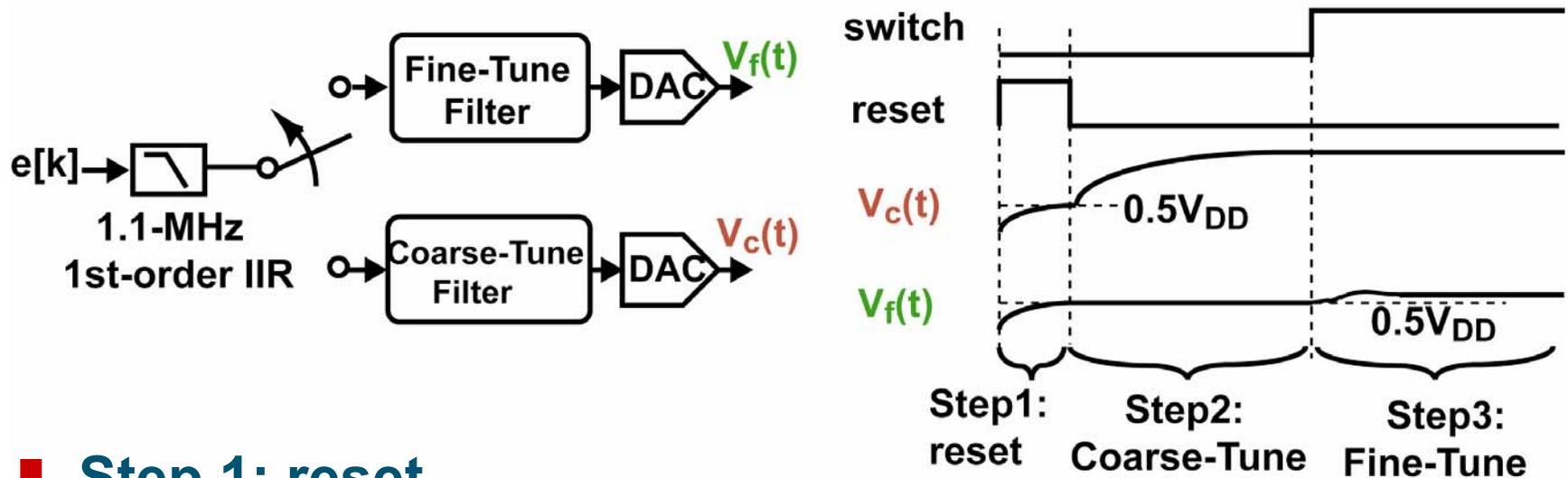
- Resample reference with 4x division frequency
- Lowers GRO range to one fourth of the reference period

Proposed Divider Structure (cont'd)



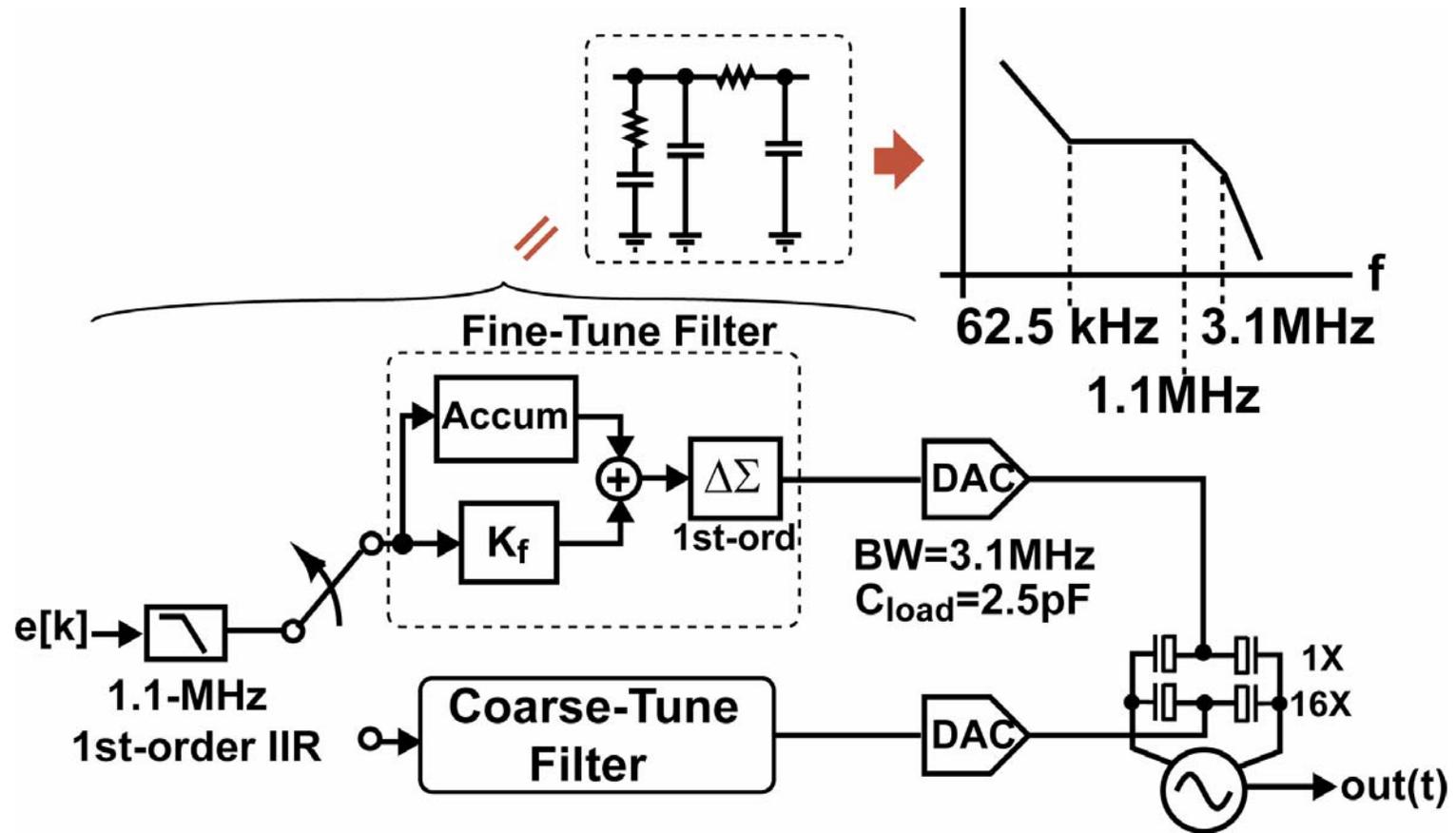
- Place $\Delta\Sigma$ dithered edge away from GRO edge
 - Prevents extra jitter due to divide-value dependent delay

Dual-Path Loop Filter



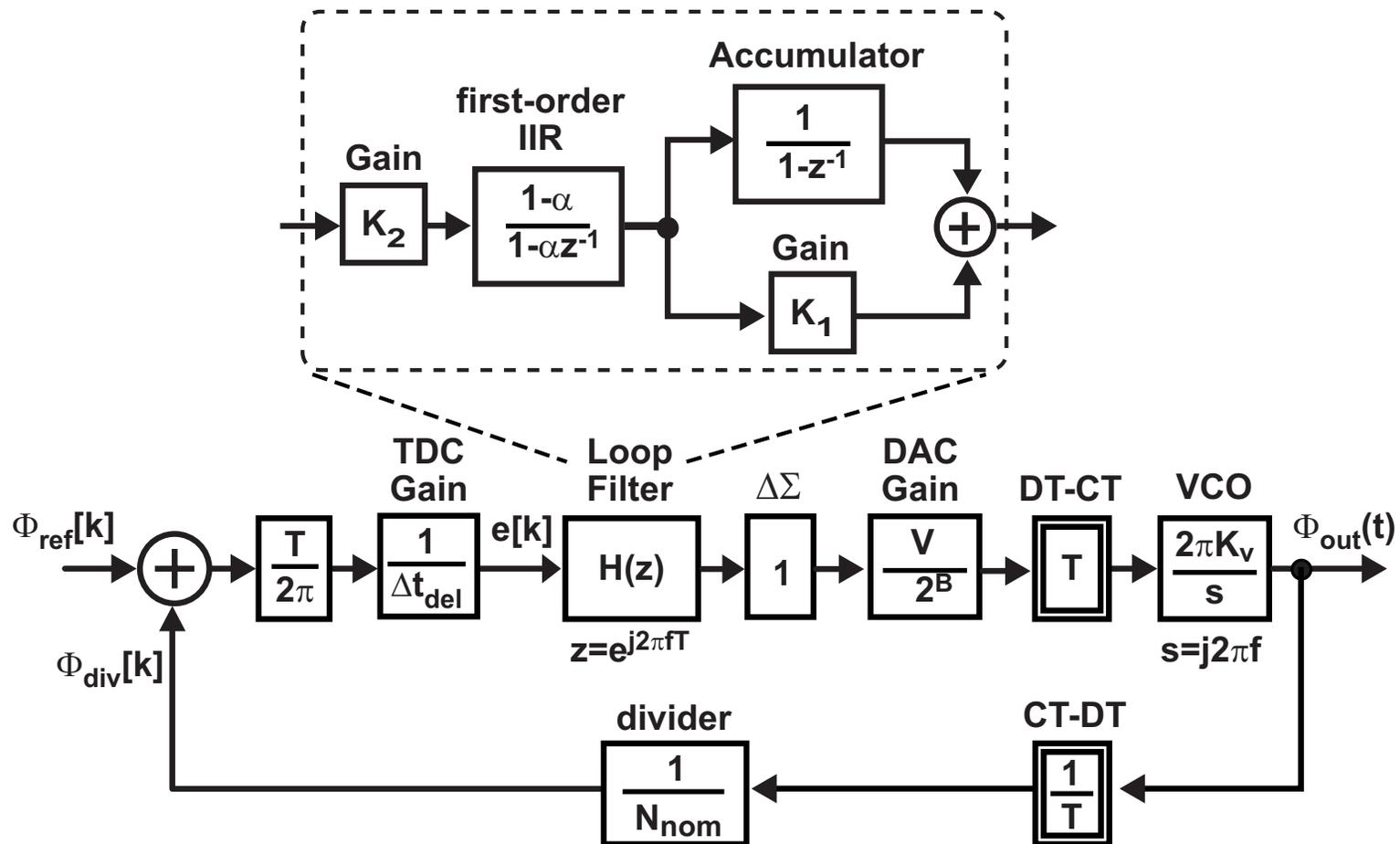
- **Step 1: reset**
- **Step 2: frequency acquisition**
 - $V_c(t)$ varies
 - $V_f(t)$ is held at midpoint
- **Step 3: steady-state lock conditions**
 - $V_c(t)$ is frozen to take quantization noise away
 - $\Delta\Sigma$ quantization noise cancellation is enabled

Fine-Path Loop Filter



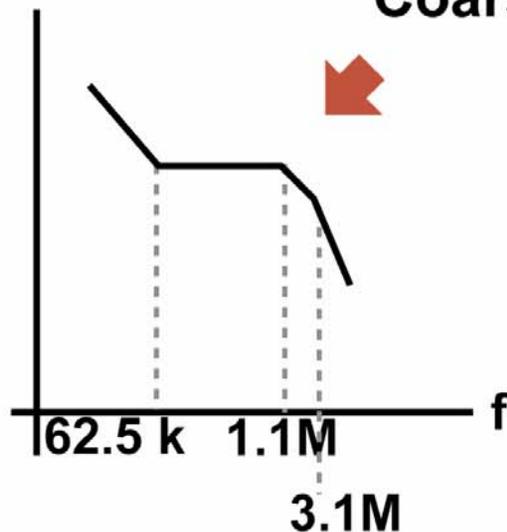
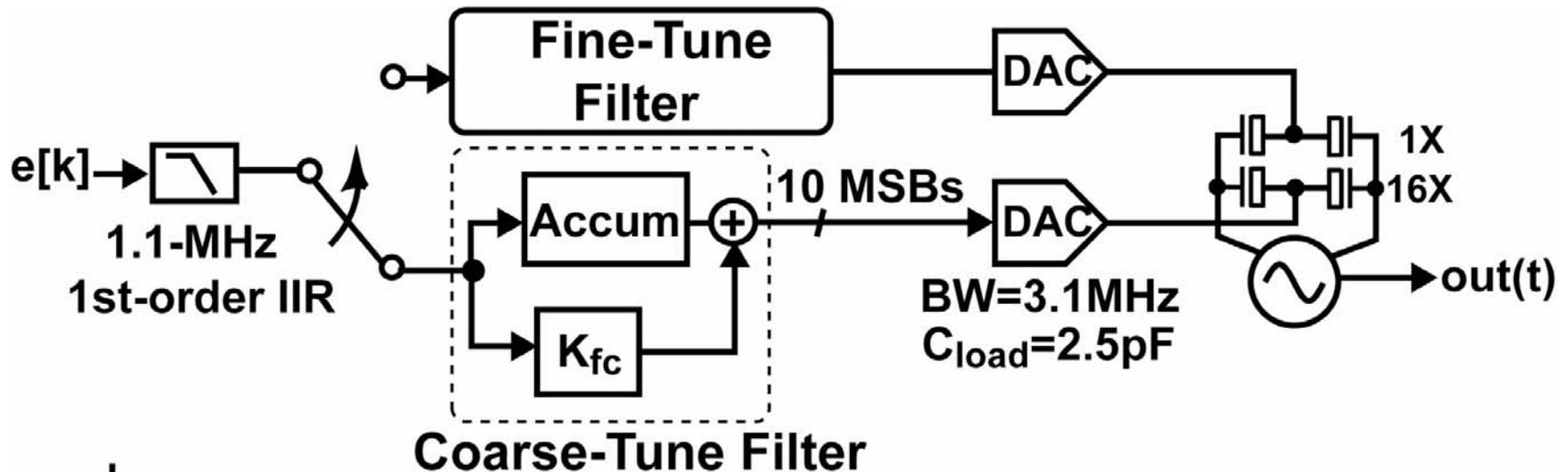
- Equivalent to an analog lead-lag filter
 - Set zero (62.5kHz) and first pole (1.1MHz) digitally
 - Set second pole (3.1MHz) by capacitor ratio
- First-order $\Delta\Sigma$ reduces in-band quantization noise

Linearized Model of PLL Under Fine-Tune Operation



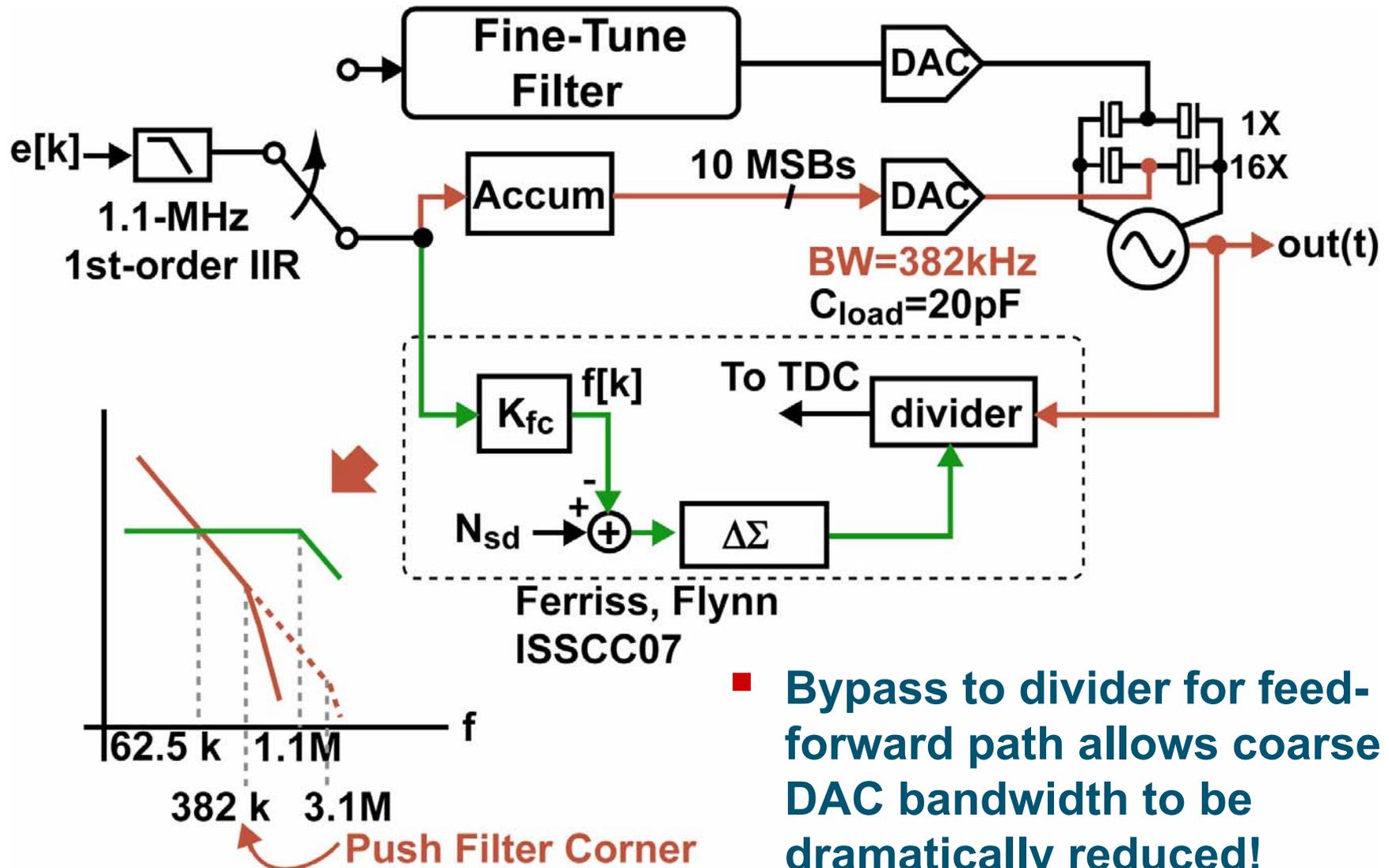
- Standard lead-lag filter topology but implemented in digital domain
 - Consists of accumulator plus feedforward path

Same Technique Poses Problems for Coarse-Tune



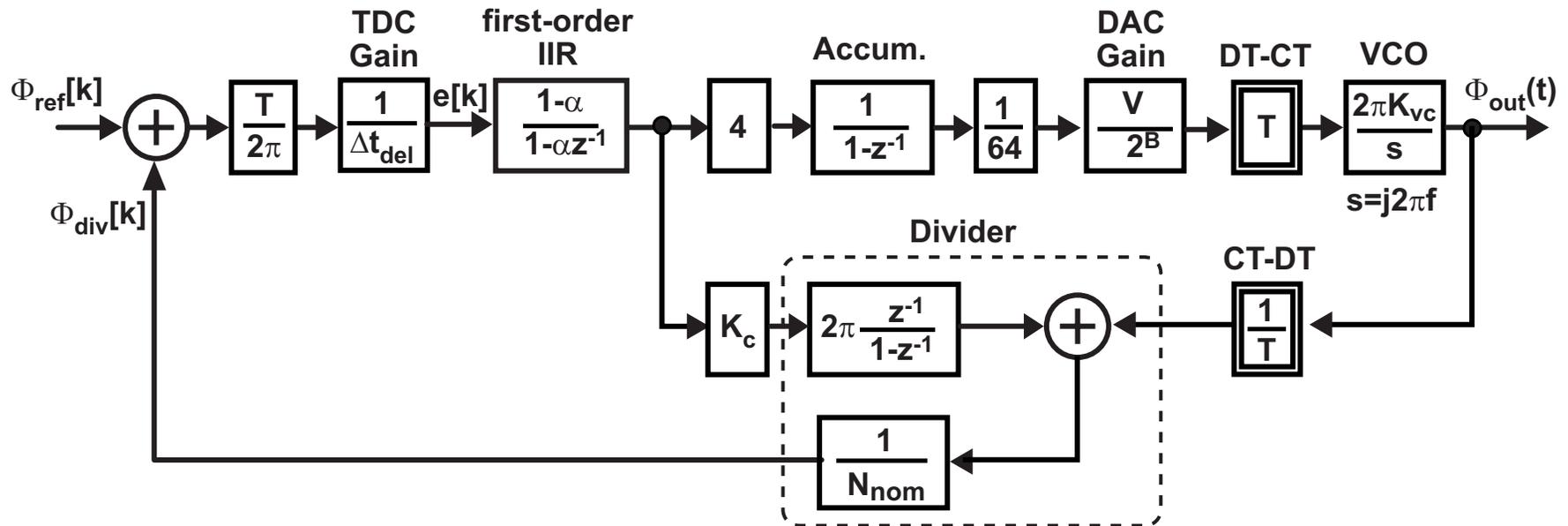
- DAC thermal noise impacts performance due to the higher coarse VCO gain
 - Can we somehow lower the DAC bandwidth?

Fix: Leverage the Divider as a Signal Path



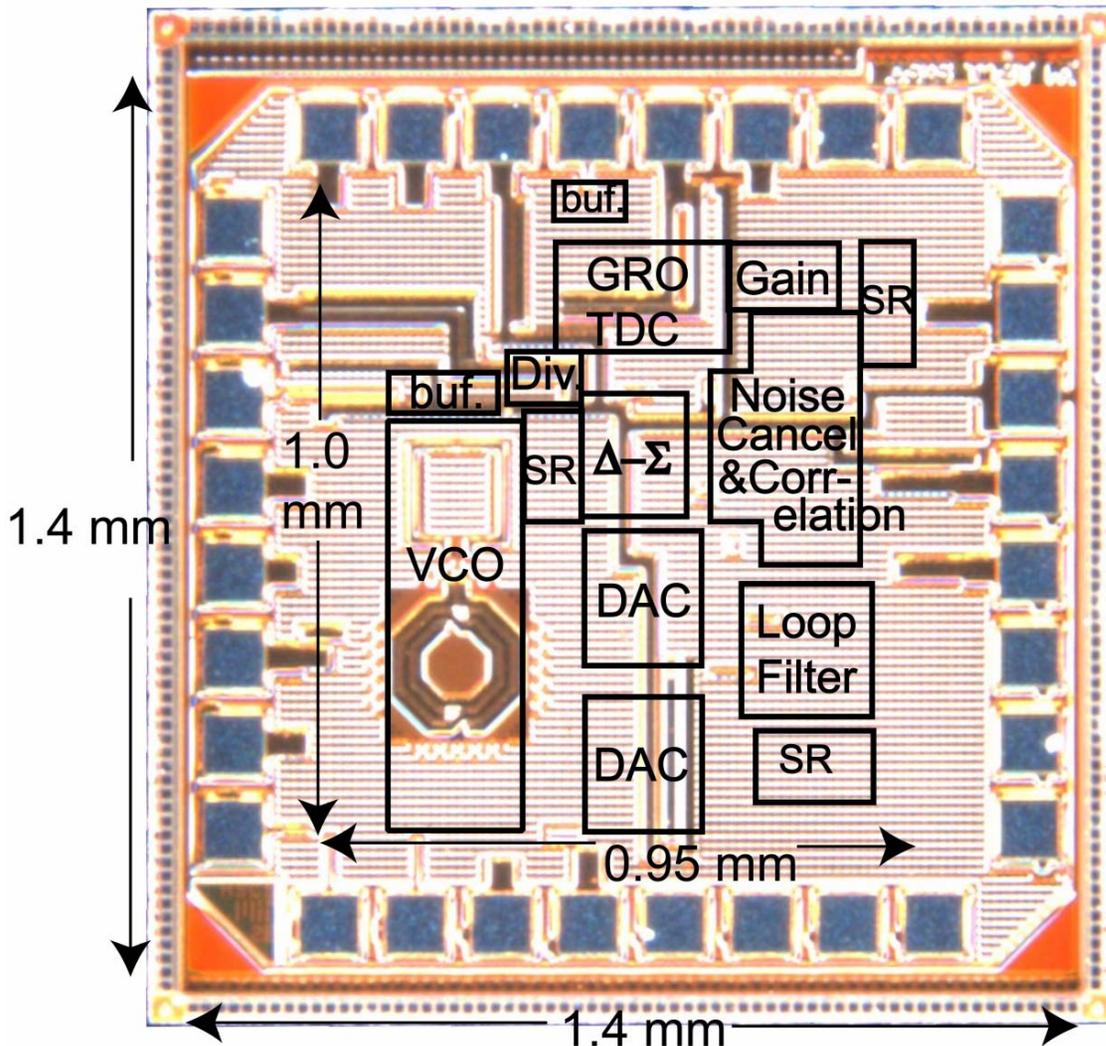
- Bypass to divider for feed-forward path allows coarse DAC bandwidth to be dramatically reduced!

Linearized Model of PLL Under Coarse-Tune Operation



- **Routing of signal path into Sigma-Delta controlling the divider yields a feedforward path**
 - Adds to accumulator path as both signals pass back through the divider
 - Allows reduction of coarse DAC bandwidth
 - Noise impact of coarse DAC on VCO is substantially lowered

Die Photo of Prototype

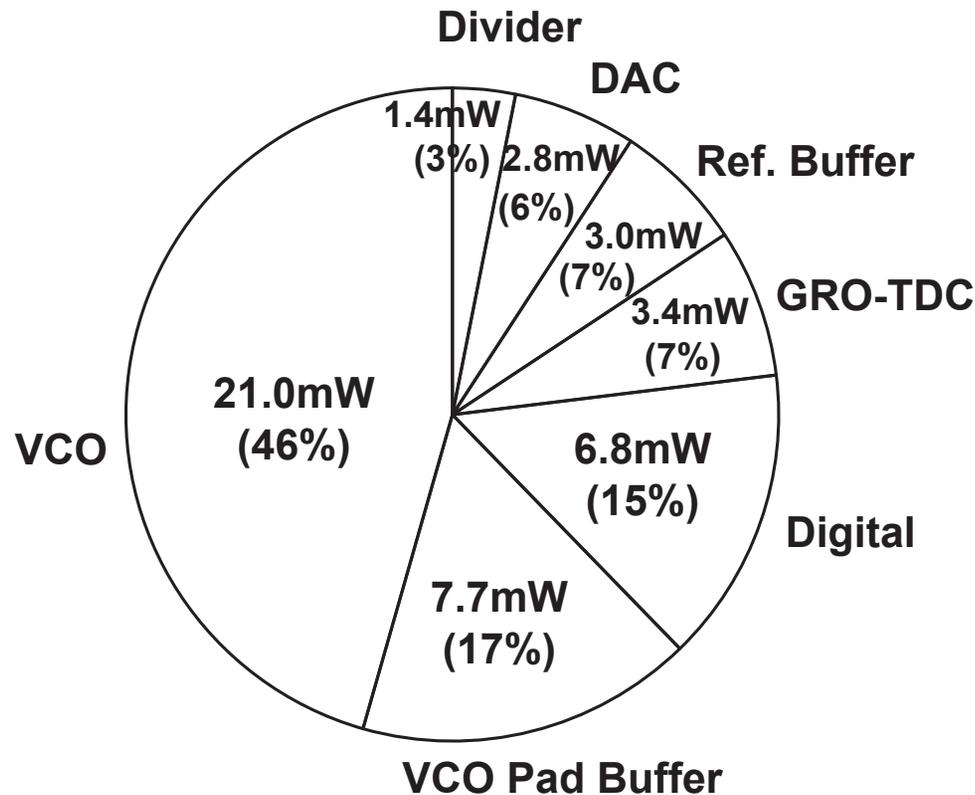


- 0.13- μm CMOS
- Active area: 0.95 mm²
- Chip area: 1.96 mm²
- V_{DD} : 1.5V
- Current:
 - 26mA (Core)
 - 7mA (VCO output buffer at 1.1V)

GRO-TDC:

- 2.3mA
- 157X252 μm^2

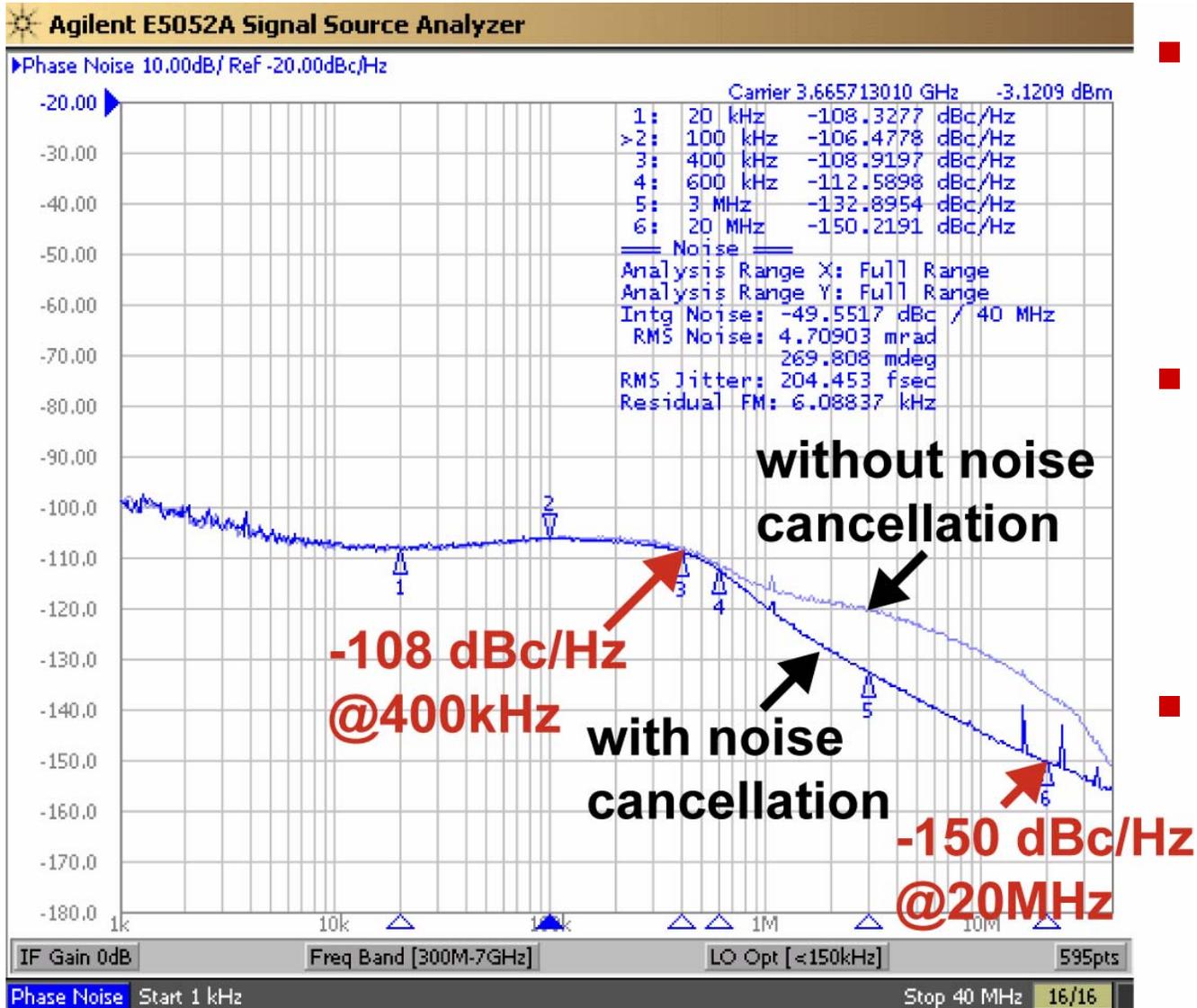
Power Distribution of Prototype IC



Total Power: 46.1mW

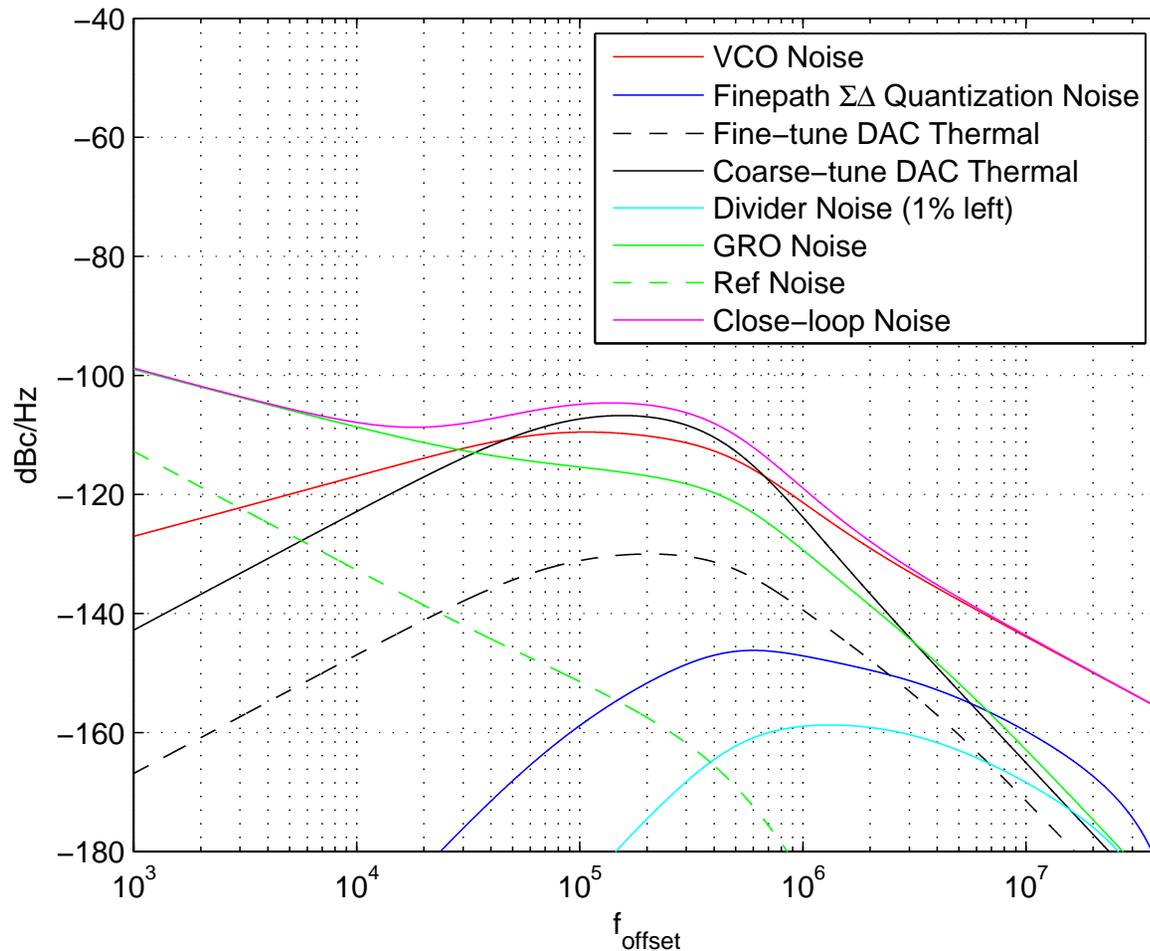
- Notice GRO and digital quantization noise cancellation have only minor impact on power (and area)

Measured Phase Noise at 3.67GHz



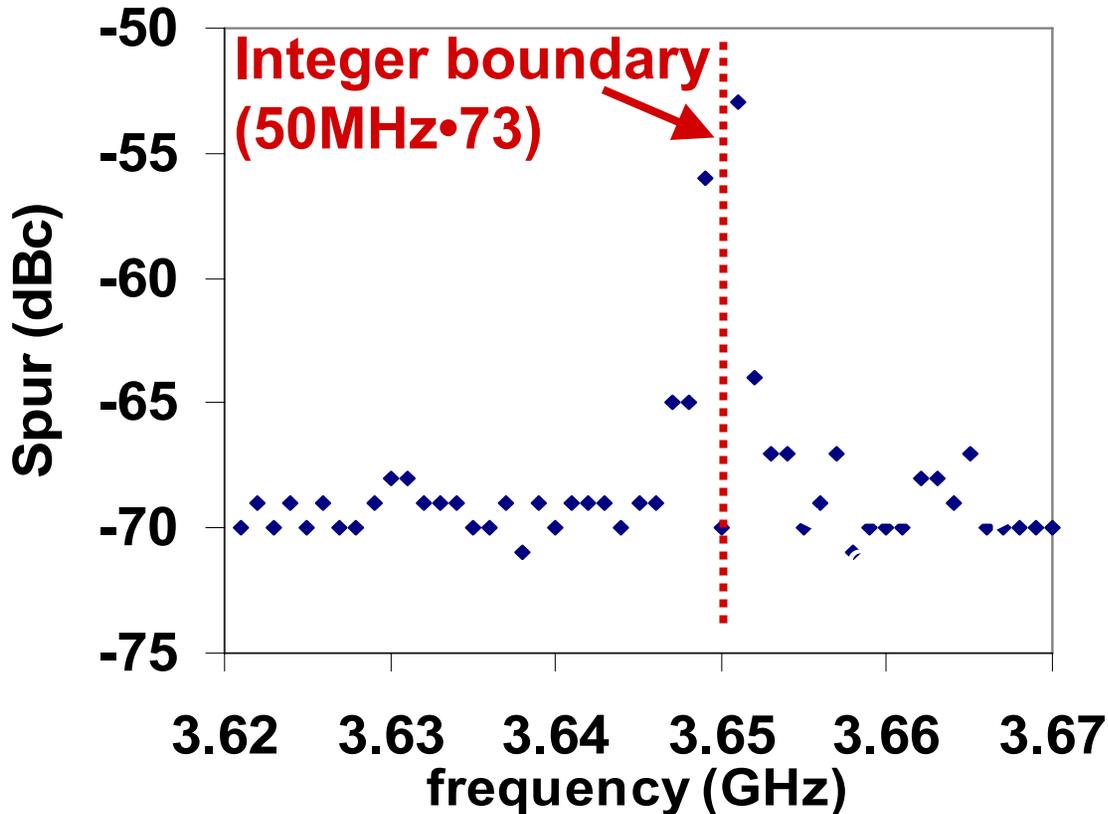
- Suppresses quantization noise by more than 15 dB
- Achieves 204 fs (0.27 degree) integrated noise (jitter)
- Reference spur: -65dBc

Calculation of Phase Noise Components



- See wideband digital synthesizer tutorial available at <http://www.cppsim.com>

Measured Worst Spurs over Fifty Channels



- Tested from 3.620 GHz to 3.670 GHz at intervals of 1 MHz
 - Worst spurs observed close to integer-N boundary (multiples of 50 MHz)
- -42dBc worst spur observed at 400kHz offset from boundary

Conclusions

- **Digital Phase-Locked Loops look extremely promising for future applications**
 - Very amenable to future CMOS processes
 - Excellent performance can be achieved
- **Analysis of digital PLLs is similar to analog PLLs**
 - PLL bandwidth is often chosen for best noise performance
 - TDC (or Ref) noise dominates at low frequency offsets
 - DCO noise dominates at high frequency offsets
- **Behavioral simulation tools such as CppSim allow architectural investigation and validation of calculations**
- **TDC structures are an exciting research area**
 - Ideas from A-to-D conversion can be applied

Innovation of future digital PLLs will involve joint circuit/algorithm development