

A Low Area, Switched-Resistor Loop Filter Technique for Fractional-N Synthesizers Applied to a MEMS-based Programmable Oscillator

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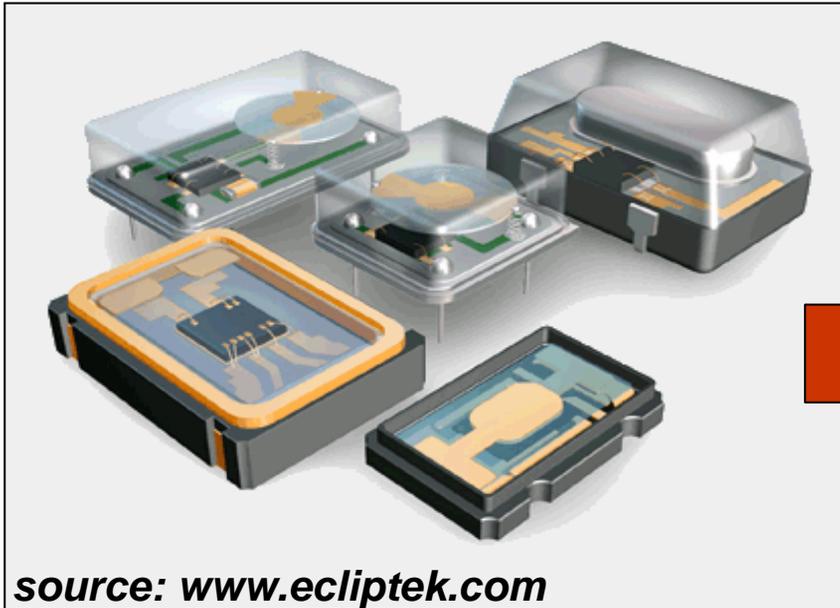
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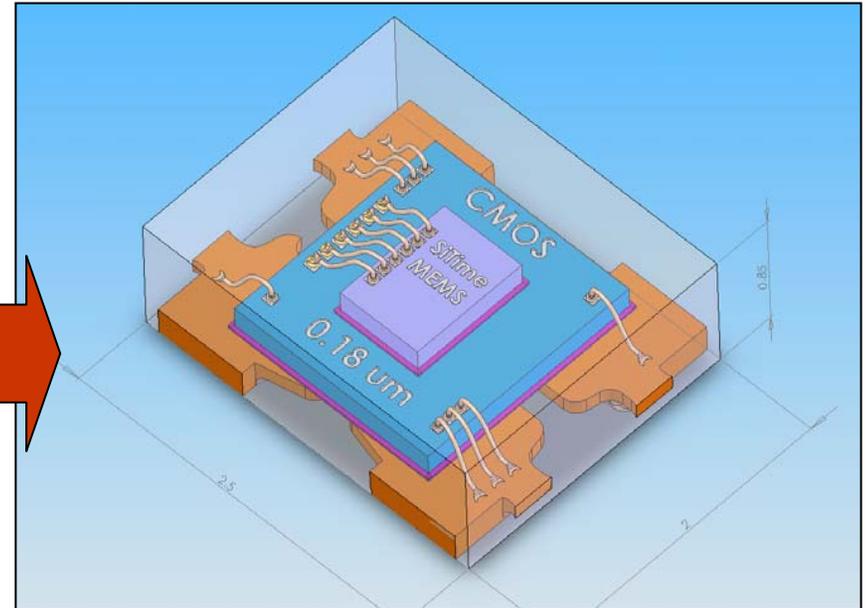


Why Switch to MEMS-based Programmable Oscillators?

Quartz Oscillators



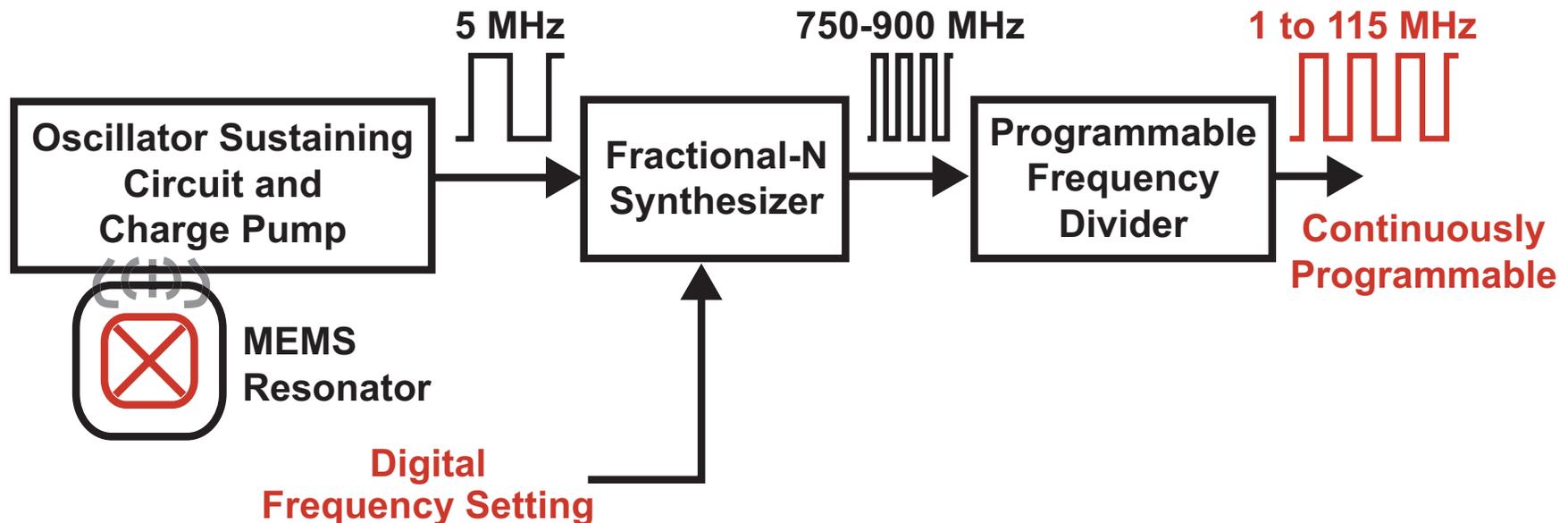
MEMS-based Oscillator



- A part for each frequency and non-plastic packaging
 - Non-typical frequencies require long lead times
- Same part for all frequencies and plastic packaging
 - Pick any frequency you want without extra lead time

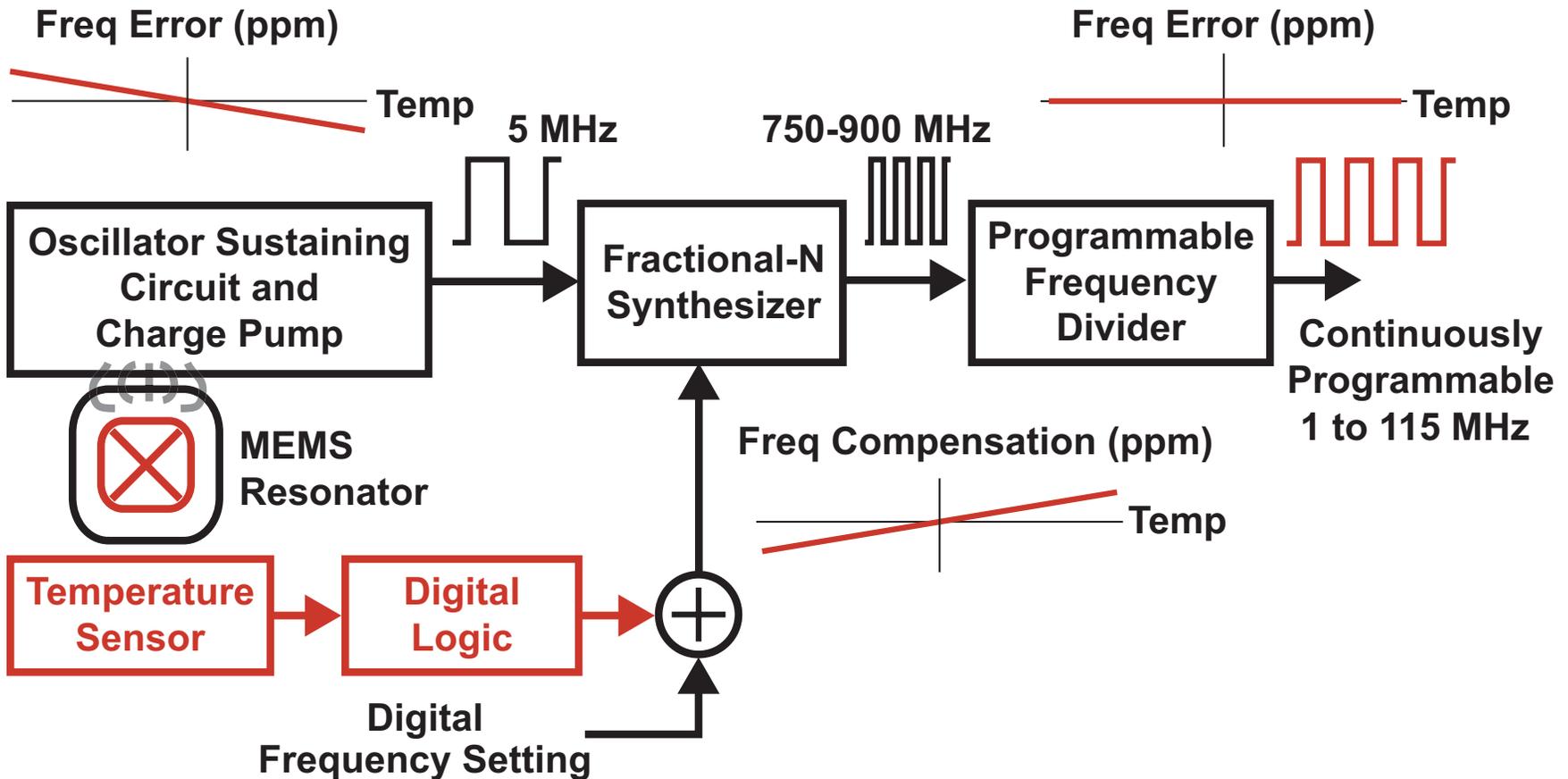
We can achieve high volumes at low cost using IC fabrication

Architecture of MEMS-Based Programmable Oscillator



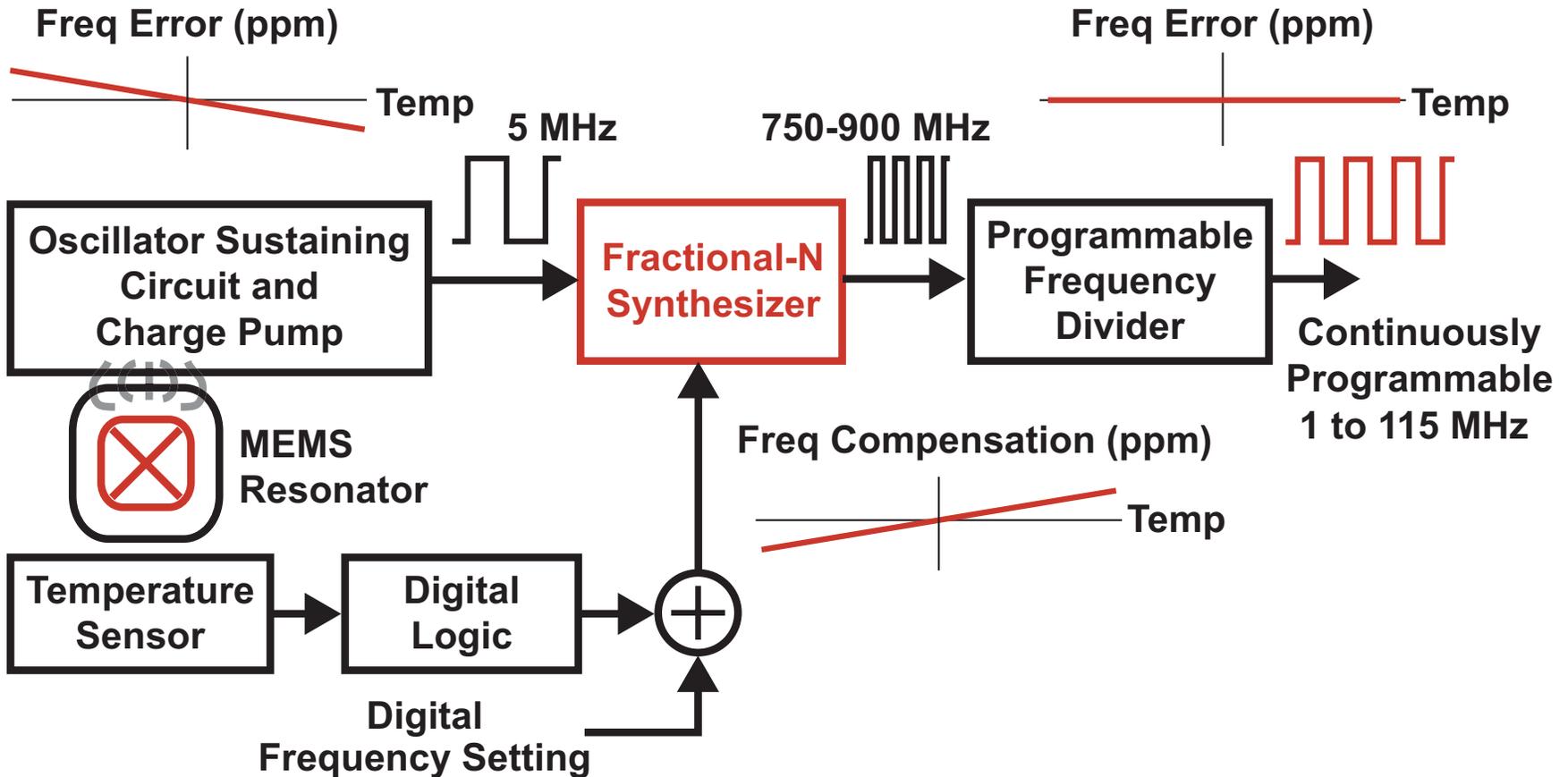
- **MEMS device provides high Q resonance at 5 MHz**
 - CMOS circuits provide DC bias and sustaining amplifier
- **Fractional-N synthesizer multiplies 5 MHz MEMS reference to a programmable range of 750 to 900 MHz**
- **Programmable frequency divider enables 1 to 115 MHz output**

Compensation of Temperature Variation



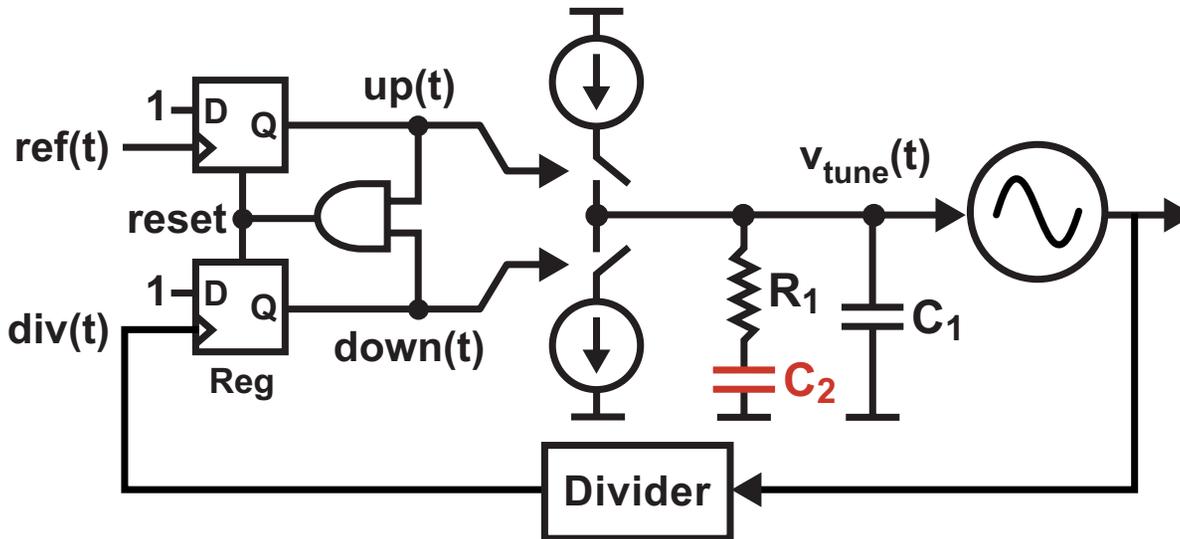
- High resolution control of fractional-N synthesizer allows simple method of compensating for MEMS frequency variation with temperature
 - Simply add temperature sensor and digital compensation logic

The Focus of This Talk



How do we achieve a fractional-N synthesizer with low area, low power, and low design complexity?

Analog Versus Digital Fractional-N Synthesizer?

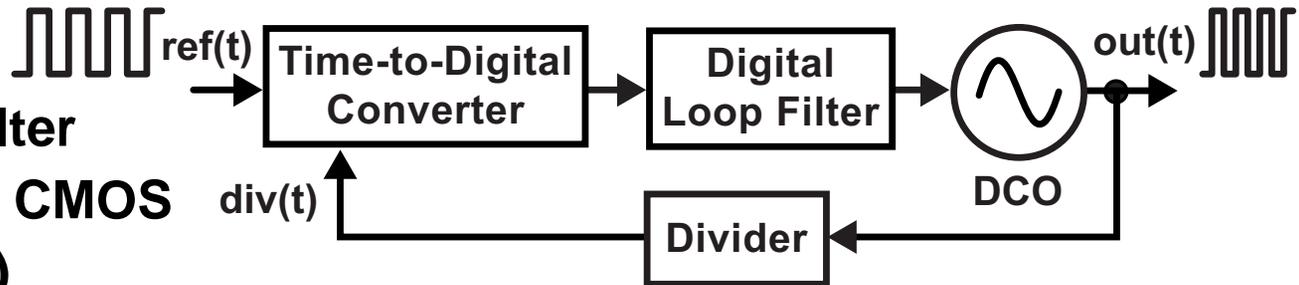


Analog PLL

- + Low power
- Large loop filter (Dominated by C_2)

Digital PLL

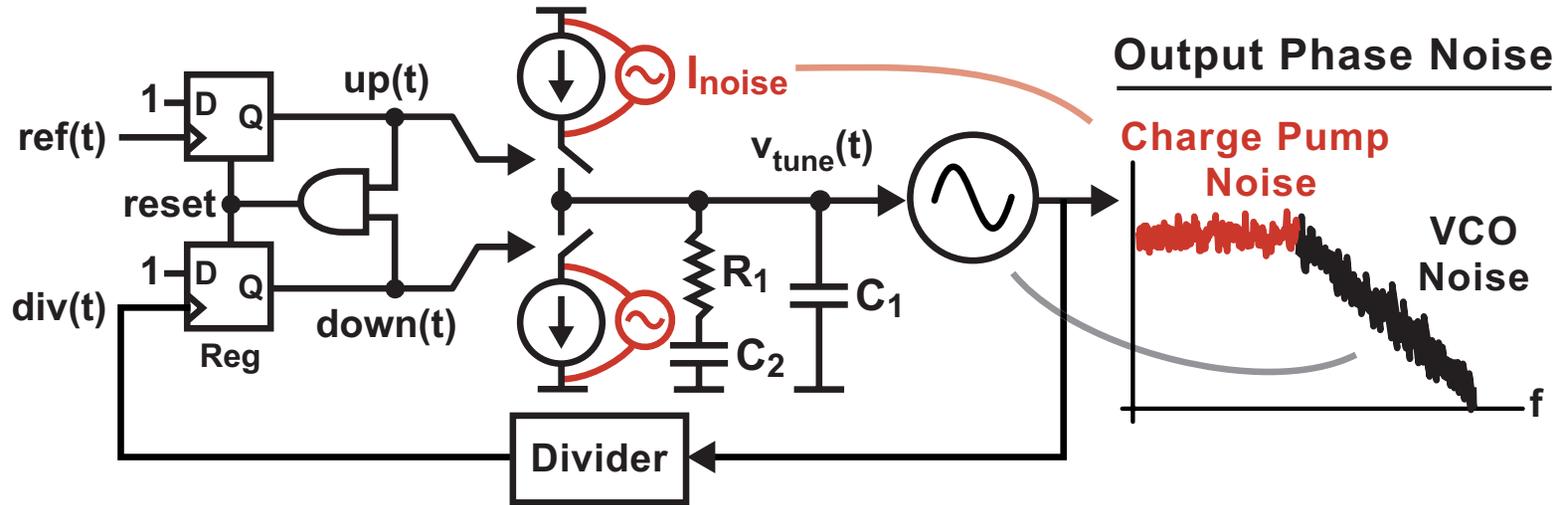
- + Smaller loop filter
- Difficult in 0.18 CMOS (Higher power)



- Analog PLL wins in 0.18u CMOS for low power

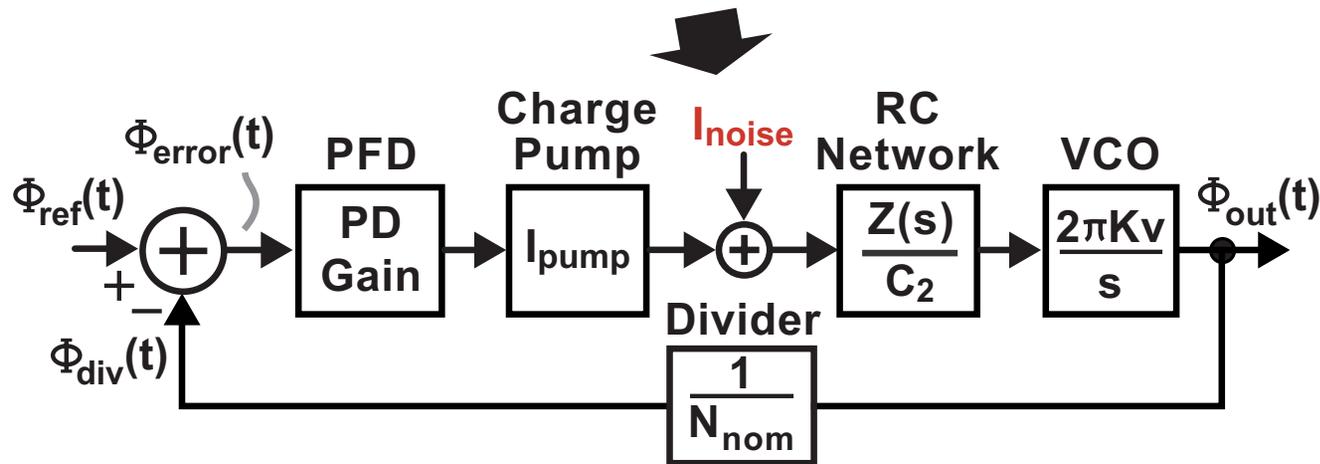
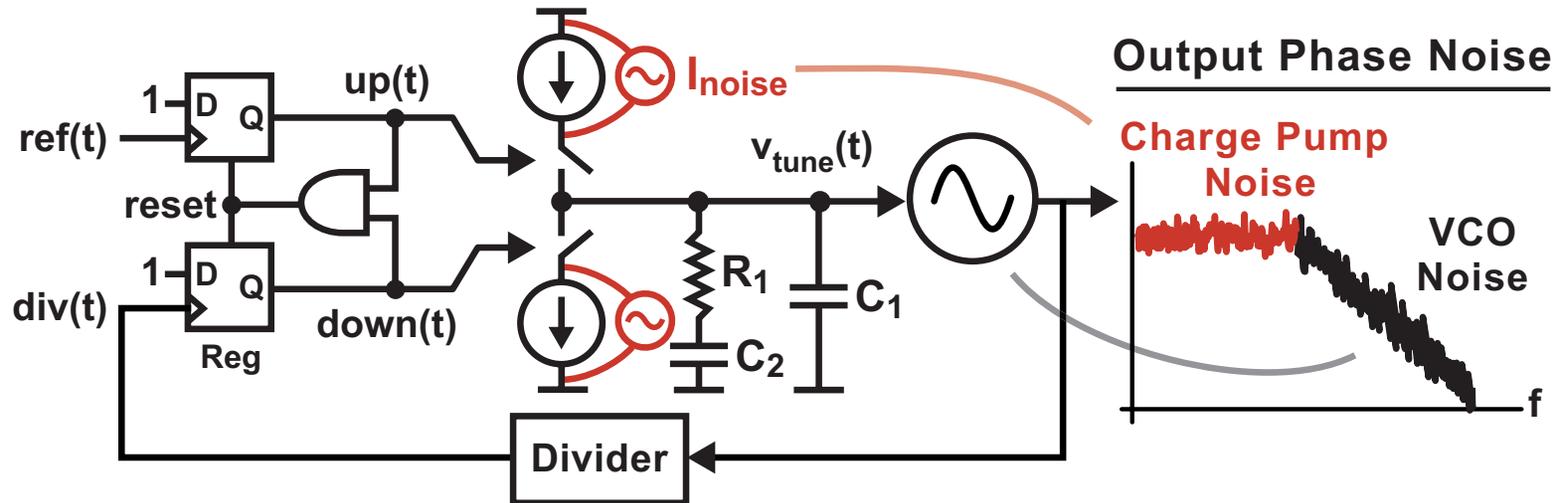
Can we achieve a low area (and low power) analog PLL with reduced design effort?

The Issue of Area: What Causes a Large Loop Filter?



- Loop filter noise (primarily from charge pump) often dominates PLL phase noise at low offset frequencies
- We will show that
 - The common approach of *reducing* loop filter noise leads to increased loop filter area (i.e., C_2 for charge pump PLL)
 - We can instead increase PD gain to lower the *impact* of loop filter noise
 - Loop filter area can be smaller

First Step: Model PLL with Charge Pump Noise

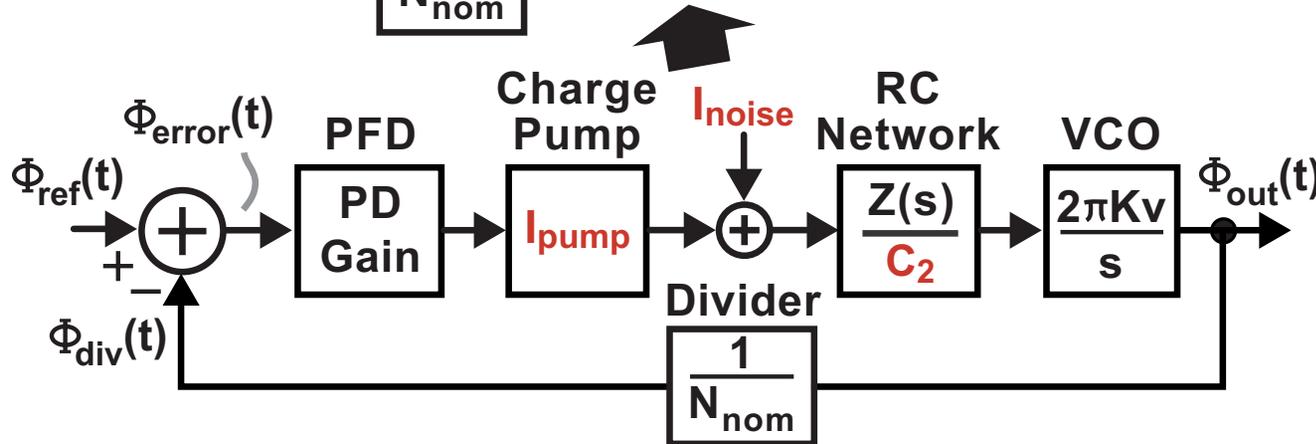
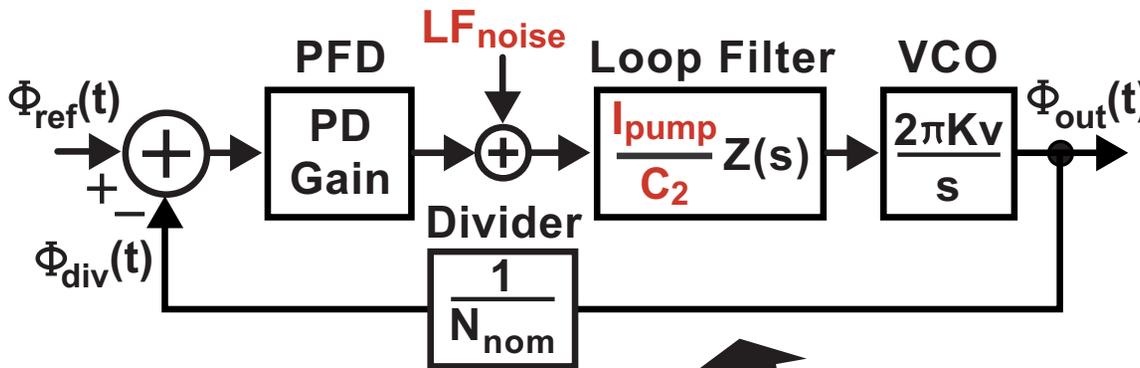
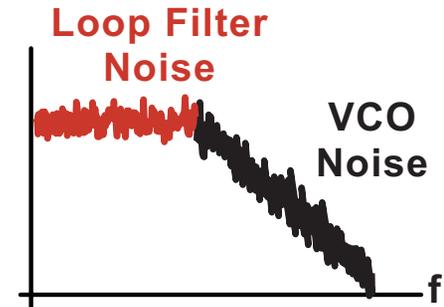


Increasing I_{pump} Reduces Input-Referred Loop Filter Noise

$$\overline{LF_{noise}}^2 \rightarrow \left| \frac{1}{I_{pump}} \right|^2 \overline{I_{noise}}^2 \rightarrow \propto \frac{1}{I_{pump}}$$

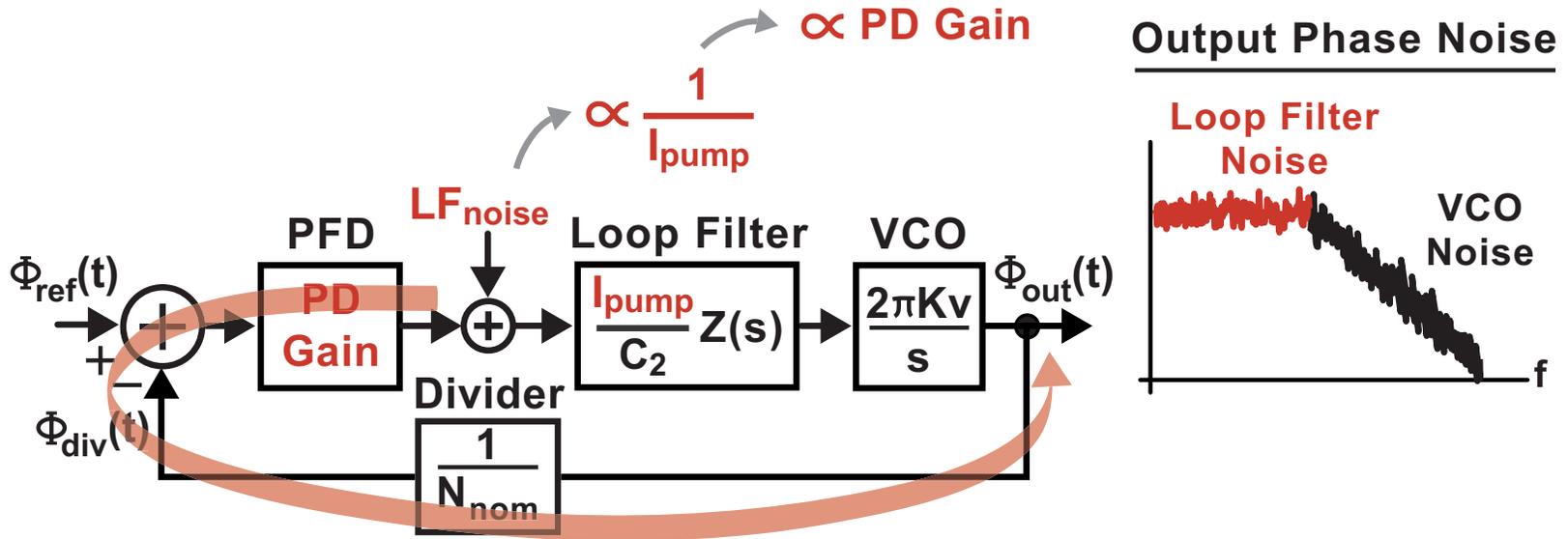
$\overline{I_{noise}}^2 \propto I_{pump}$

Output Phase Noise



Area gets larger since C_2 is typically increased as well to maintain desired open loop gain

Increasing PD Gain Reduces Impact of Loop Filter Noise



Impact of Loop Filter Noise on Output

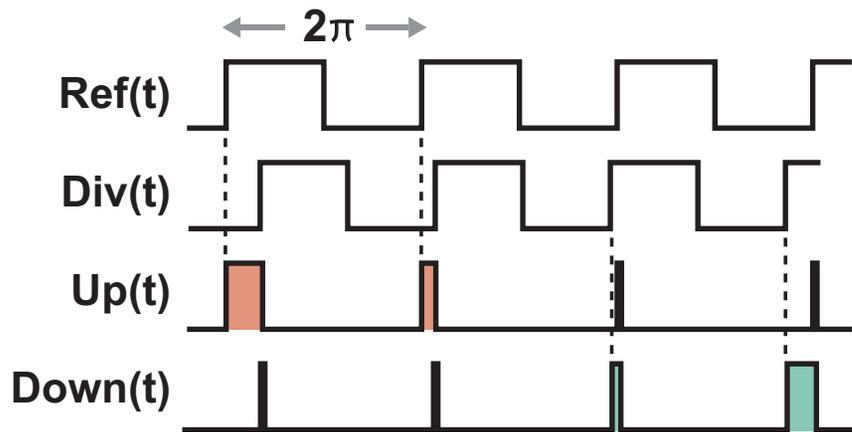
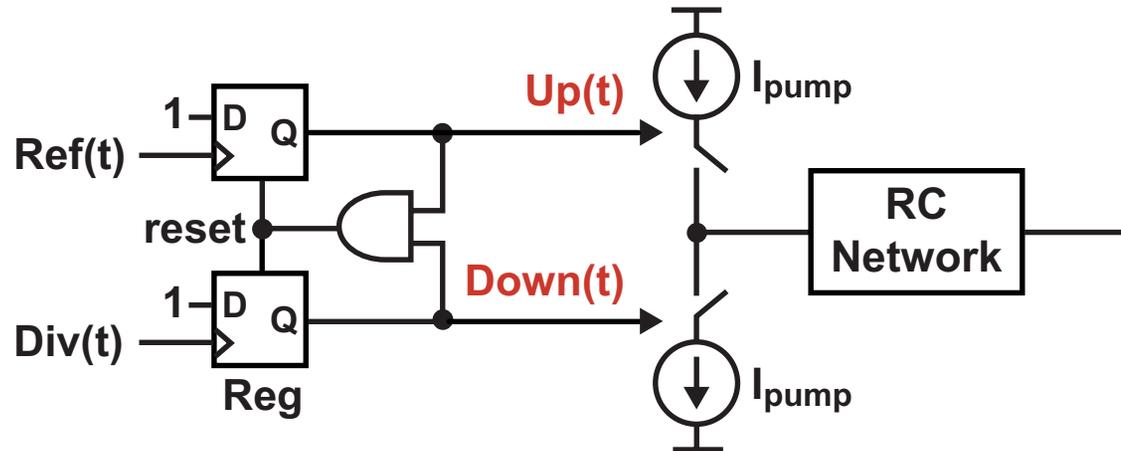
$PD\ Gain \bullet I_{pump}$
 ↑ ↓
 Keep Open Loop Gain Constant

$$\frac{LF_{noise}^2}{\left| \frac{N_{nom}}{PD\ Gain} \right|^2} \rightarrow \propto \frac{1}{PD\ Gain}$$

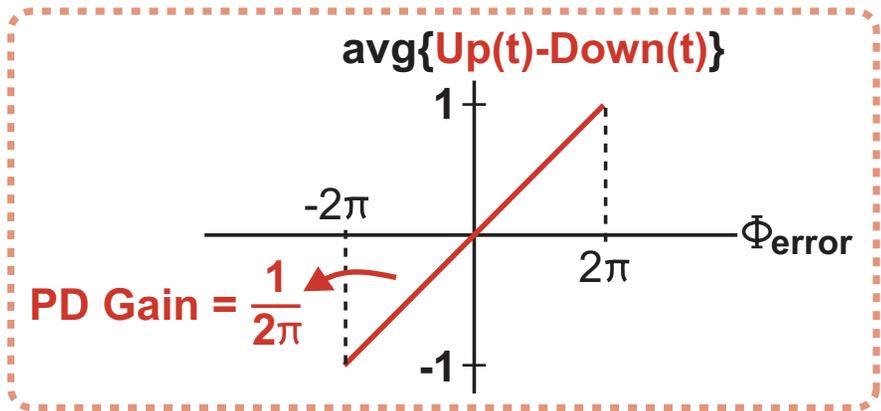
- Loop filter area does not need to become larger

But how do we increase the PD gain?

PD Gain of Classical Tristate PFD

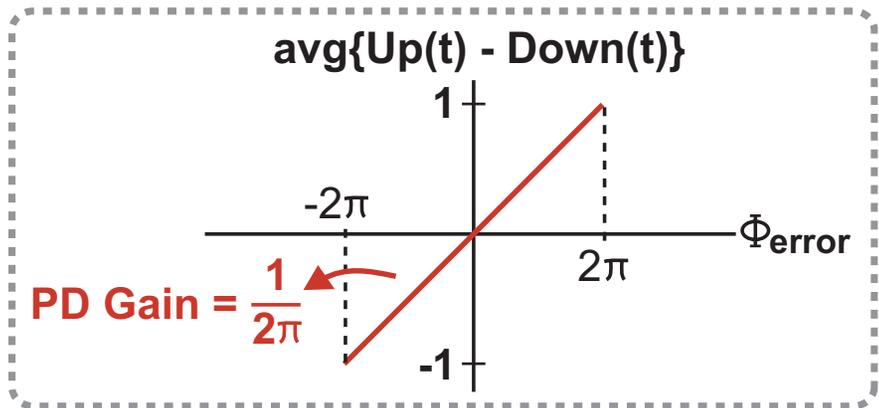
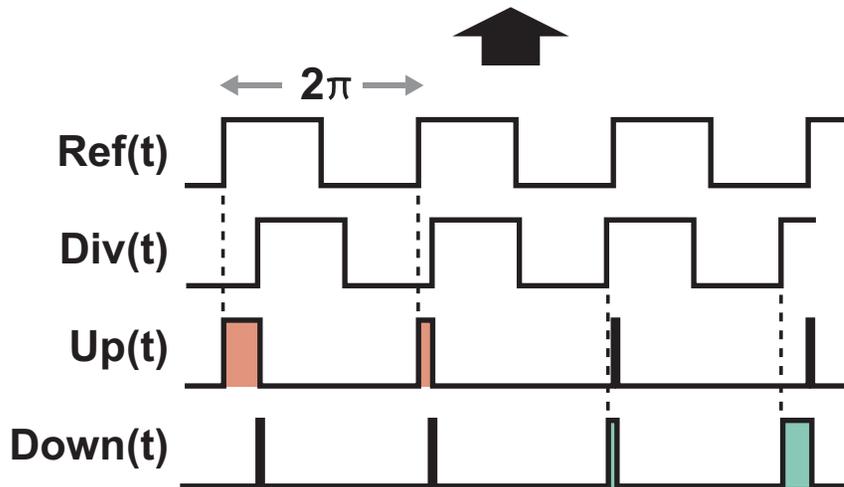
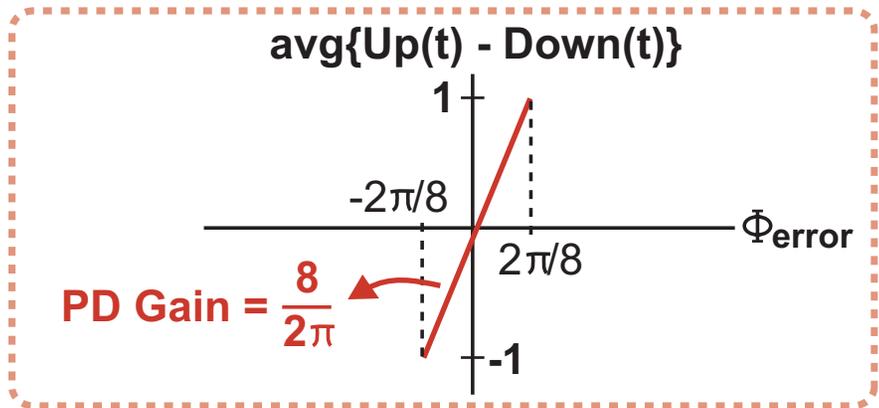
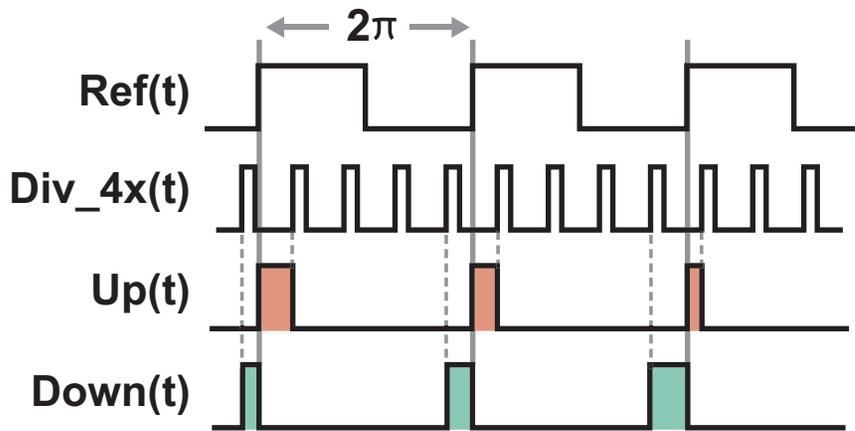


Phase Detector Characteristic



- Compute gain by averaging Up/Down pulses vs. phase error
 - Note that tristate PFD has a phase error range of 2 Ref periods

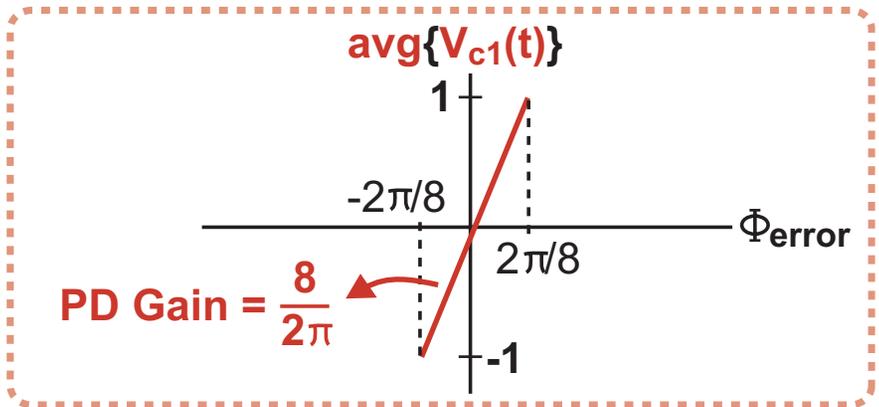
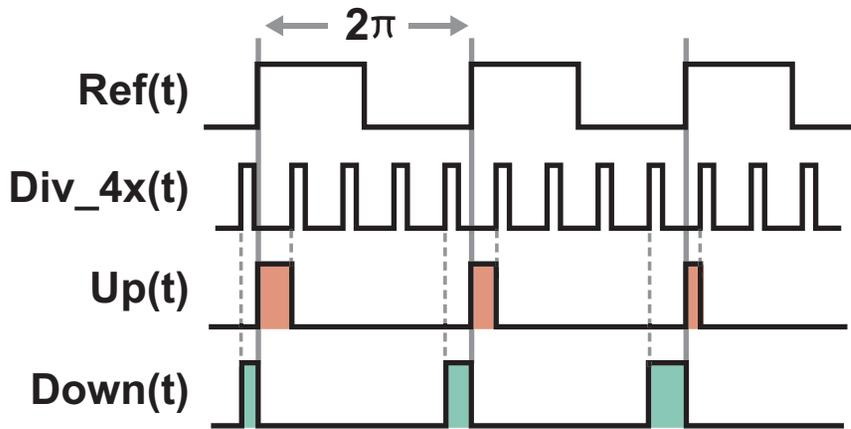
Proposed Method of Increasing Phase Detector Gain



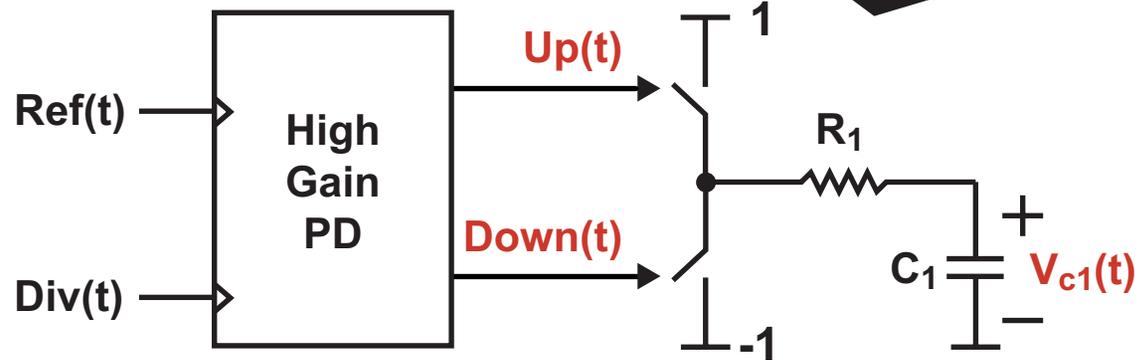
- Reduce phase detection range to 1/4 of the Ref period
 - Achieves 8X increase in phase detector gain

How do we capitalize on this reduced range in the filter?

Simple RC Network Can Be Utilized



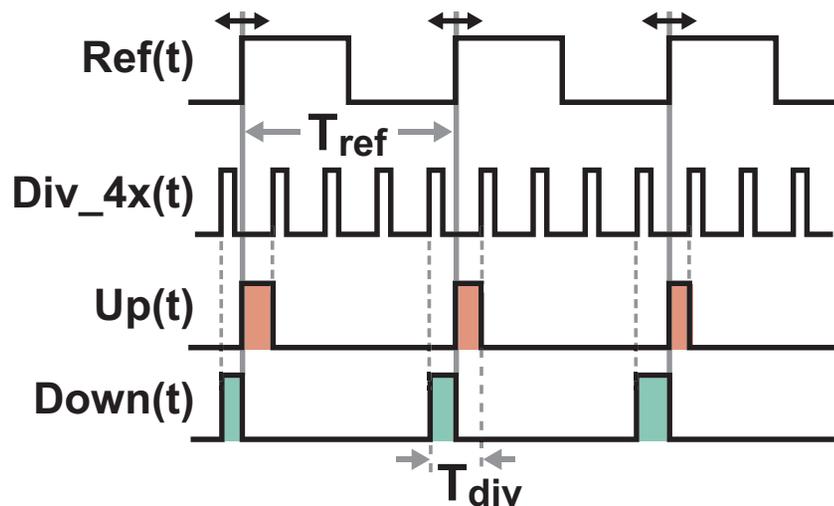
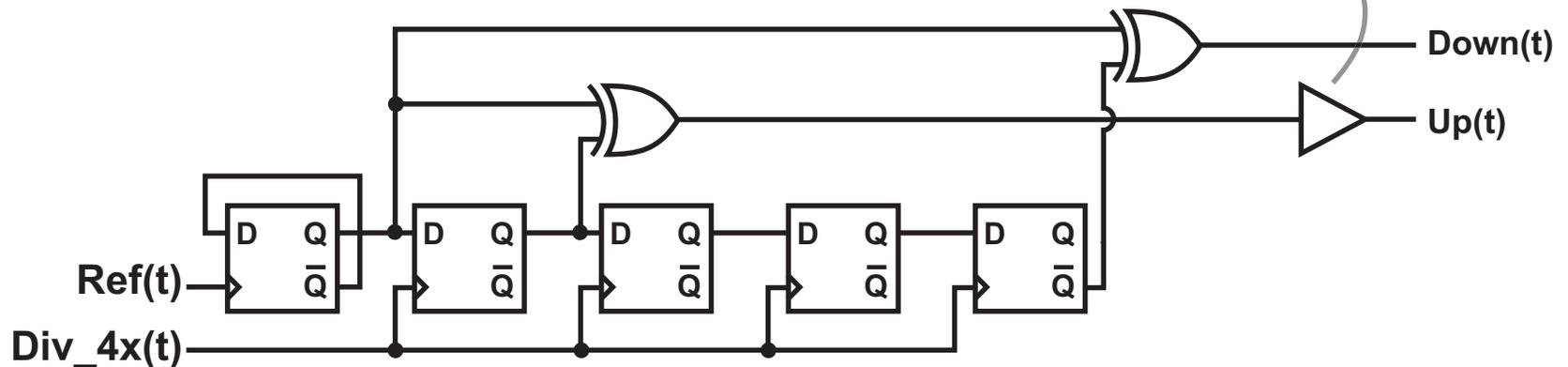
See also:
Hedayati, Bakkaloglu
RFIC 2009



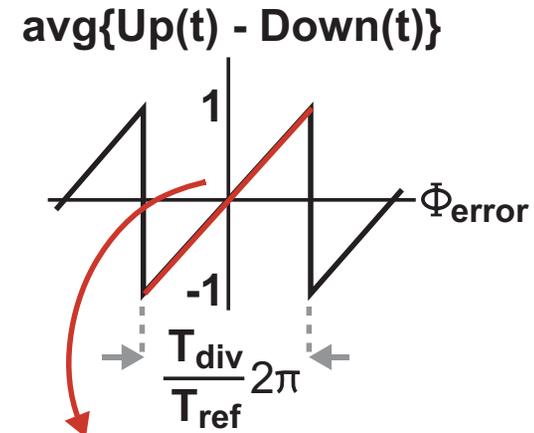
- Achieves full voltage range at V_{c1} as phase error is swept across the reduced phase detector range
- Note: instead of being influenced by charge pump gain after the PD, we are influenced by (regulated) supply voltage

Implementation of High Gain Phase Detector

Delay Buffer For Non-Overlapping Up/Down Pulses



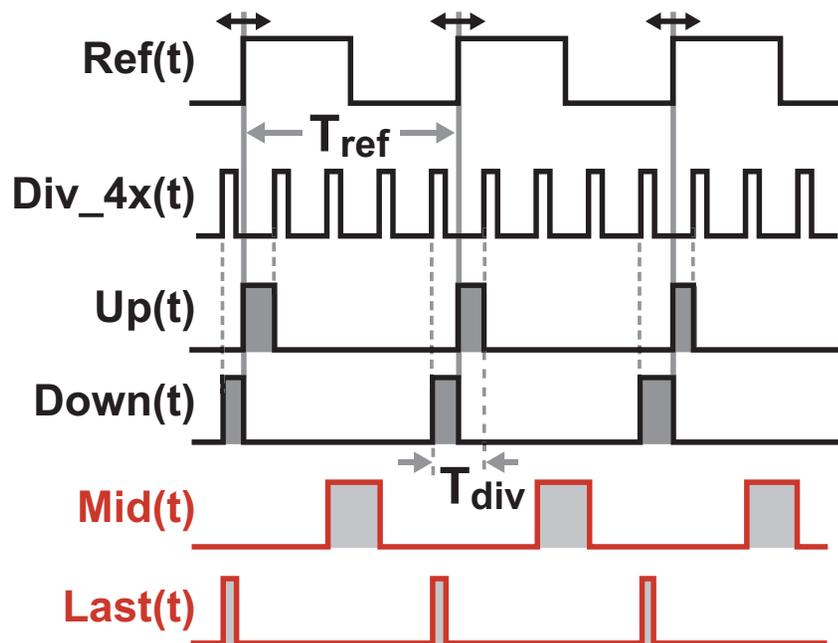
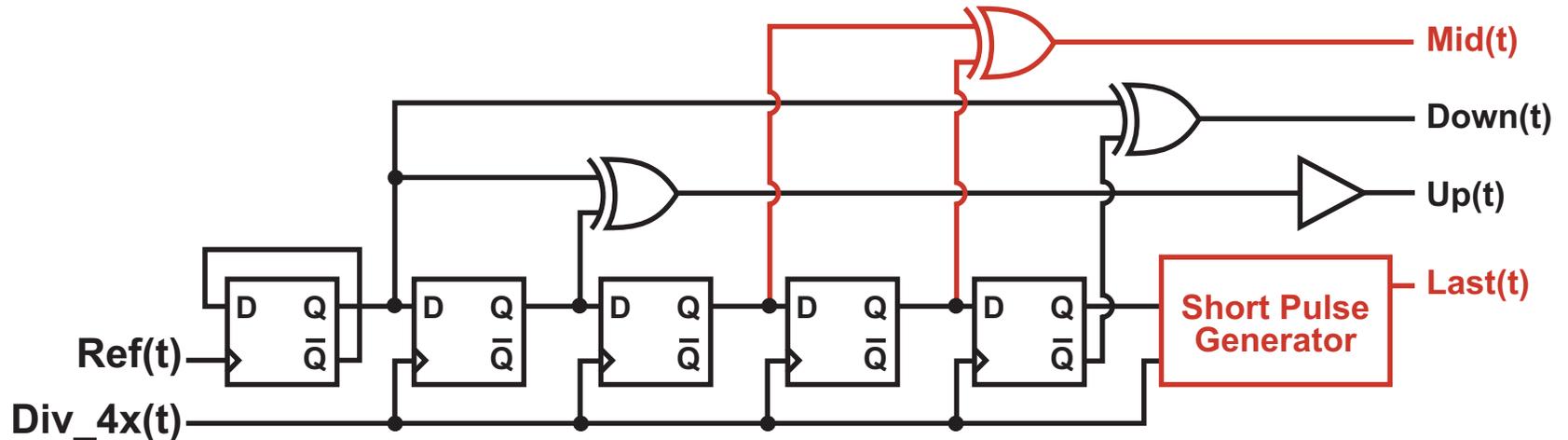
Phase Detector Characteristic



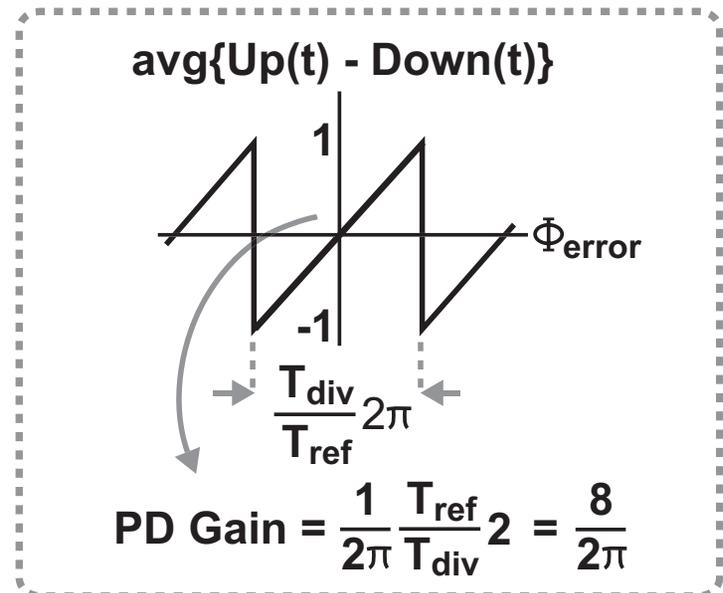
$$\text{PD Gain} = \frac{1}{2\pi} \frac{T_{\text{ref}}}{T_{\text{div}}} 2 = \frac{8}{2\pi}$$

- Use 4X higher divider frequency
 - Simple digital implementation

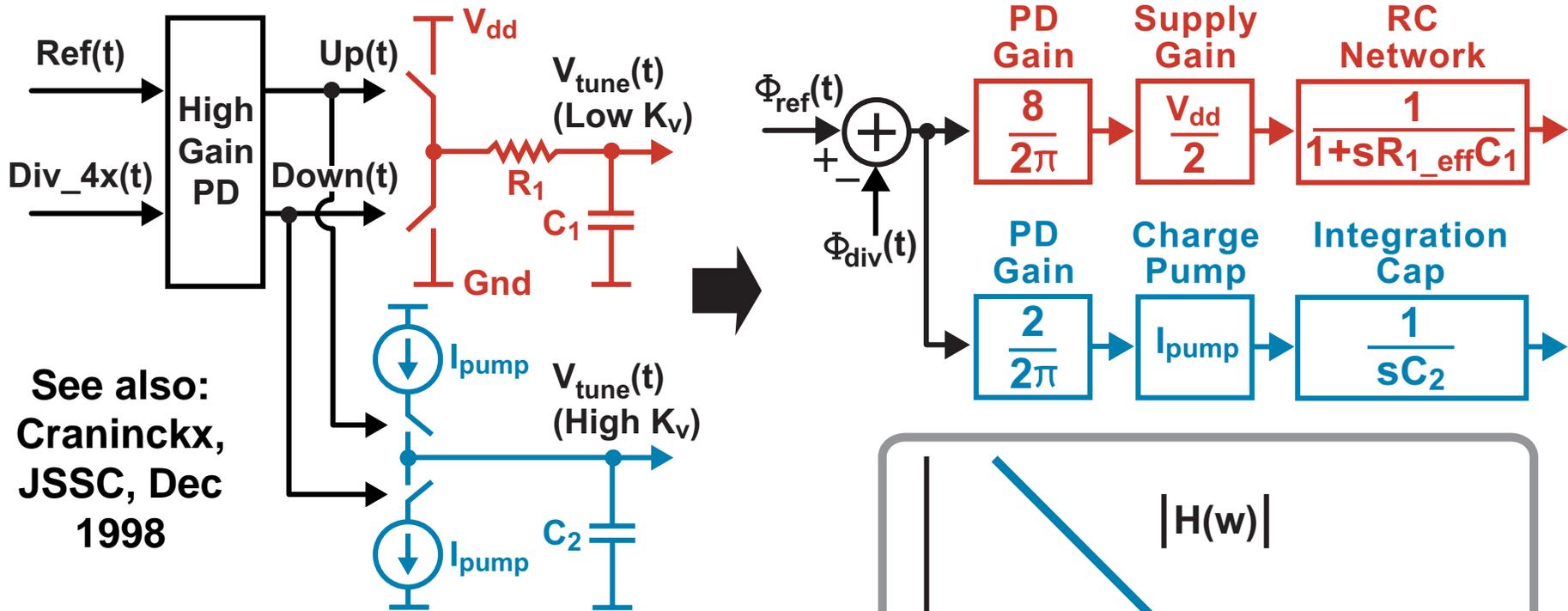
Multi-Phase Pulse Generation (We'll Use it Later...)



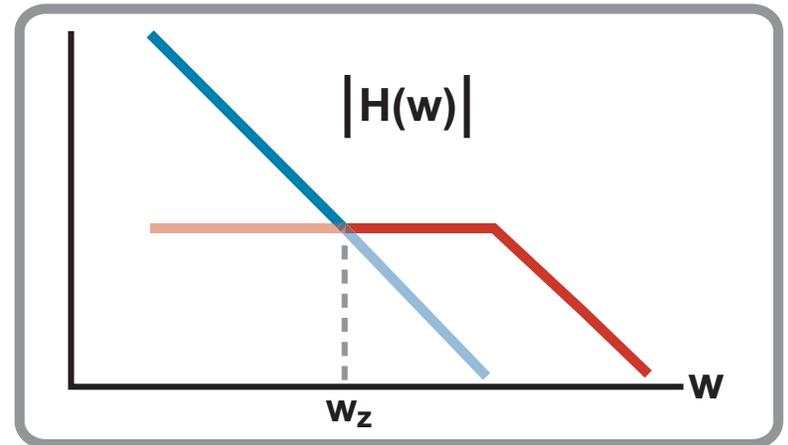
Phase Detector Characteristic



Overall Loop Filter – Consider Using Charge Pump

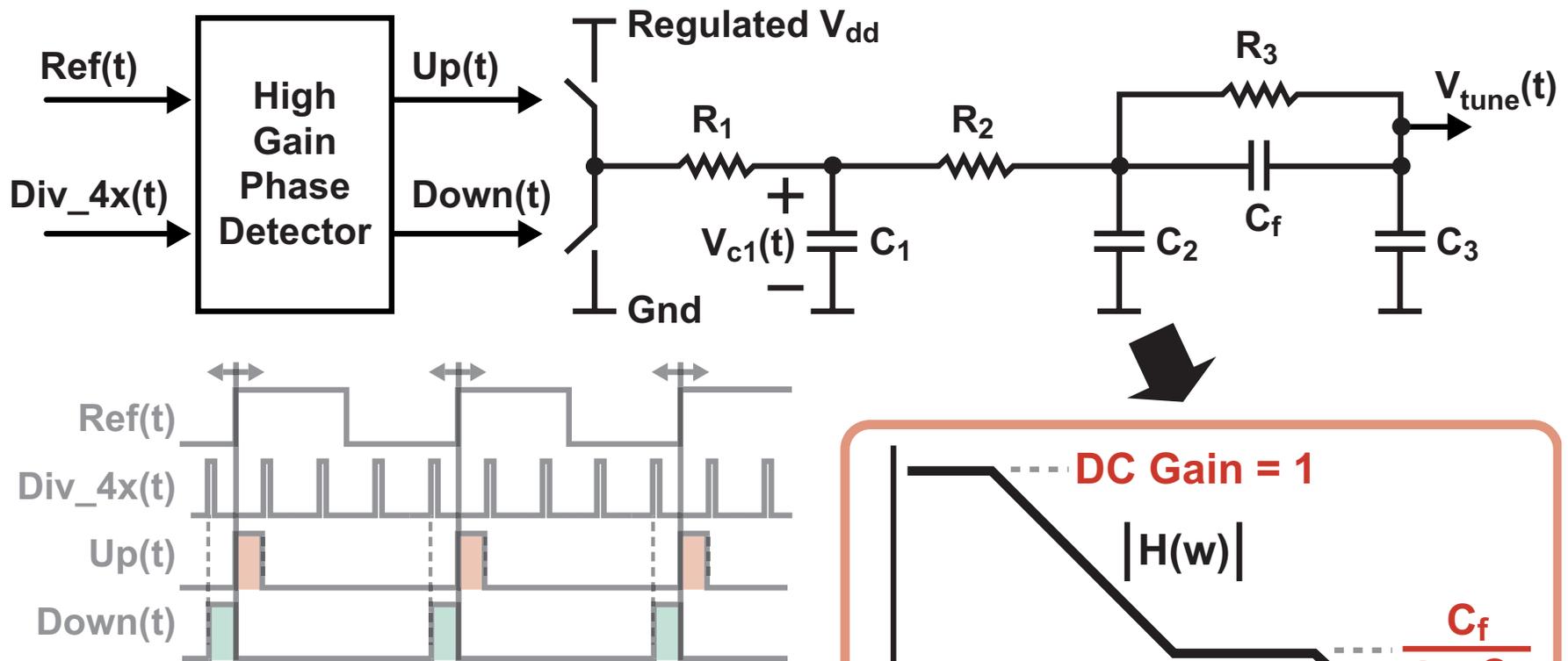


- We can use the high gain PD in a dual-path loop filter topology
 - But we want a simple design!

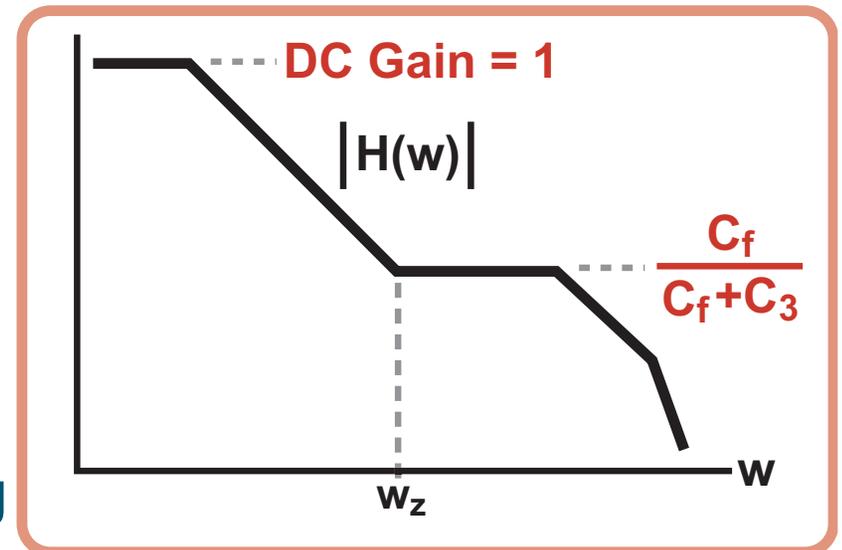


Can we remove the charge pump to reduce the analog design effort?

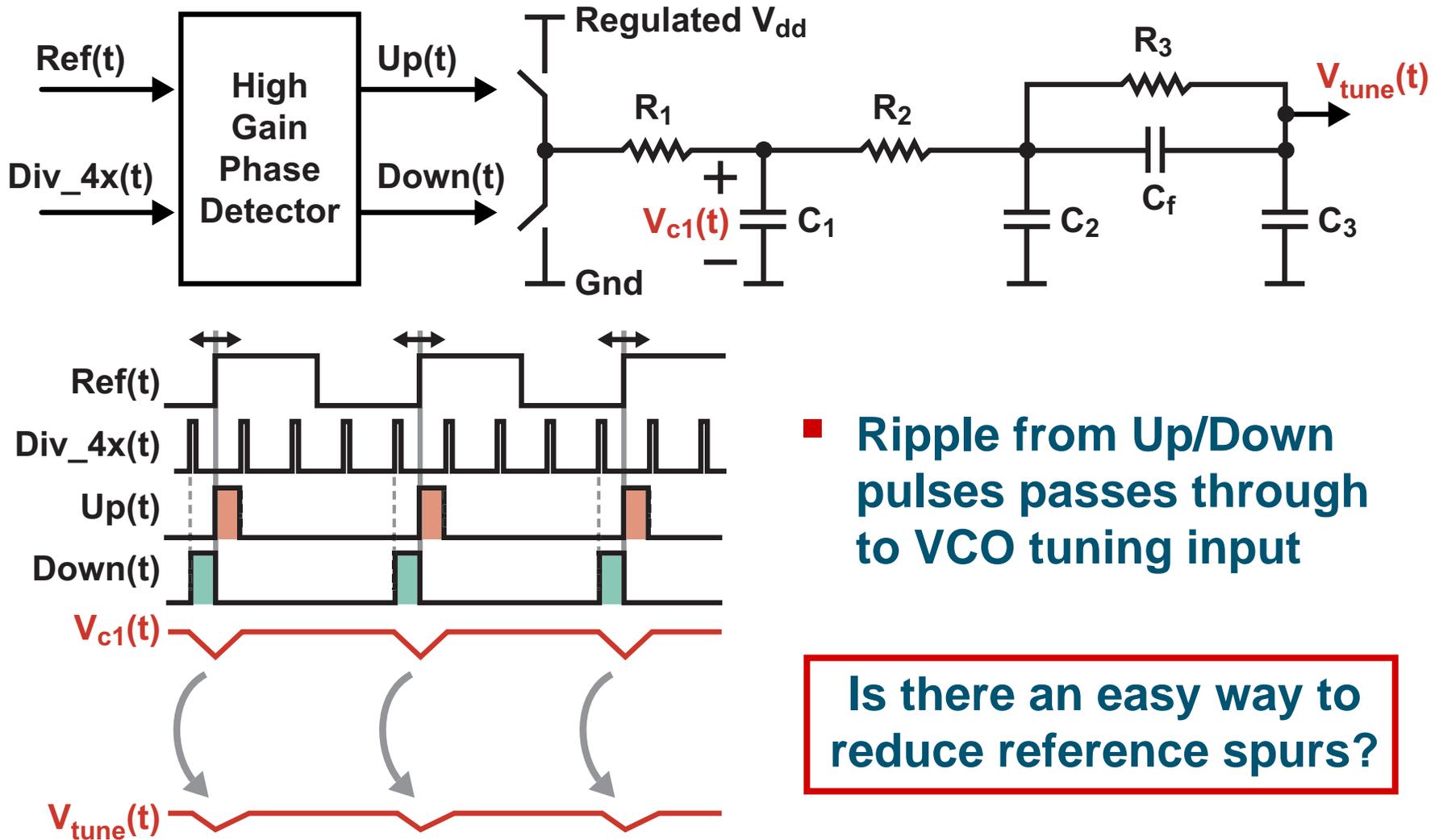
Passive RC Network Offers a Simpler Implementation



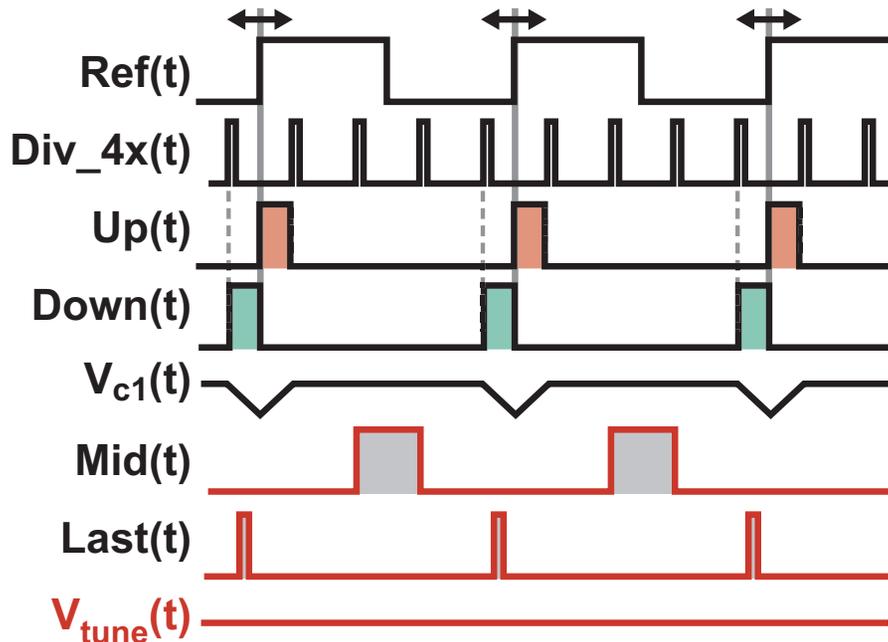
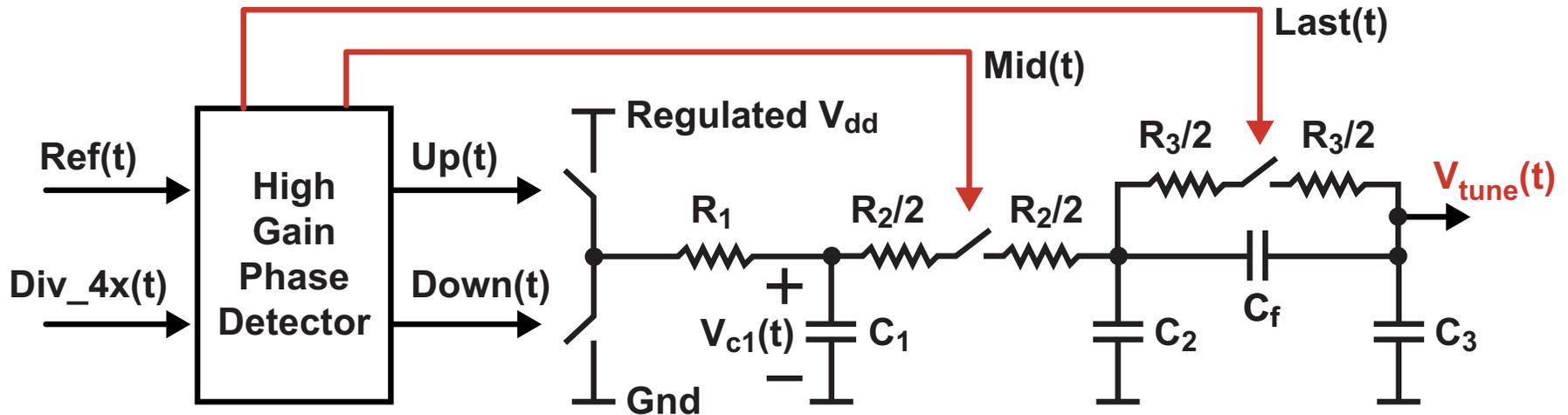
- **Capacitive feedforward path provides stabilizing zero**
- **Design effort is simply choosing switch sizes and RC values**



The Issue of Reference Spurs



Leverage Multi-Phase Pulsing

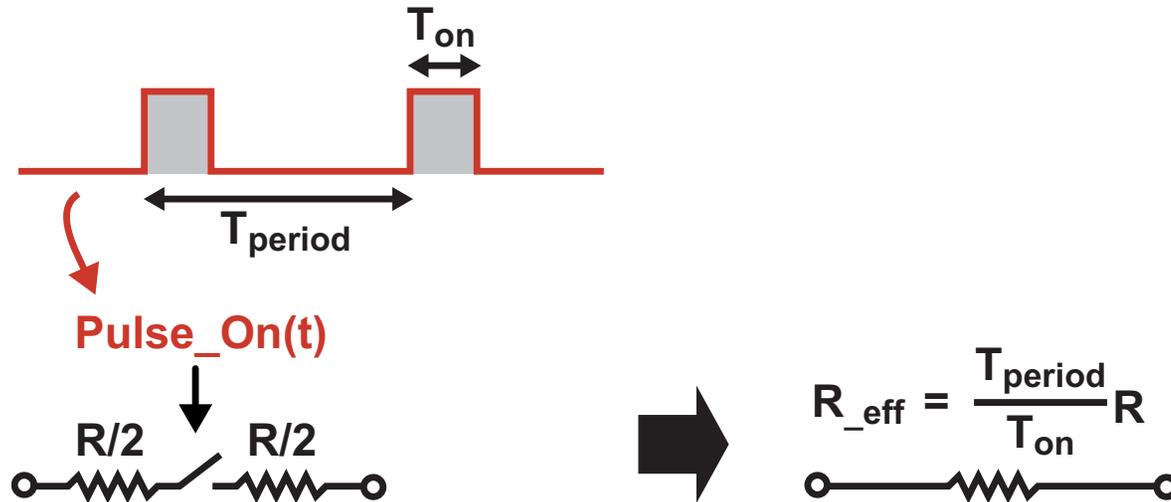


■ **Ripple from Up/Down pulses blocked before reaching VCO**

- Reference spurs reduced!
- Similar to sample-and-hold technique (such as Zhang et. al., JSSC, 2003)

There is a nice side benefit to pulsing resistors...

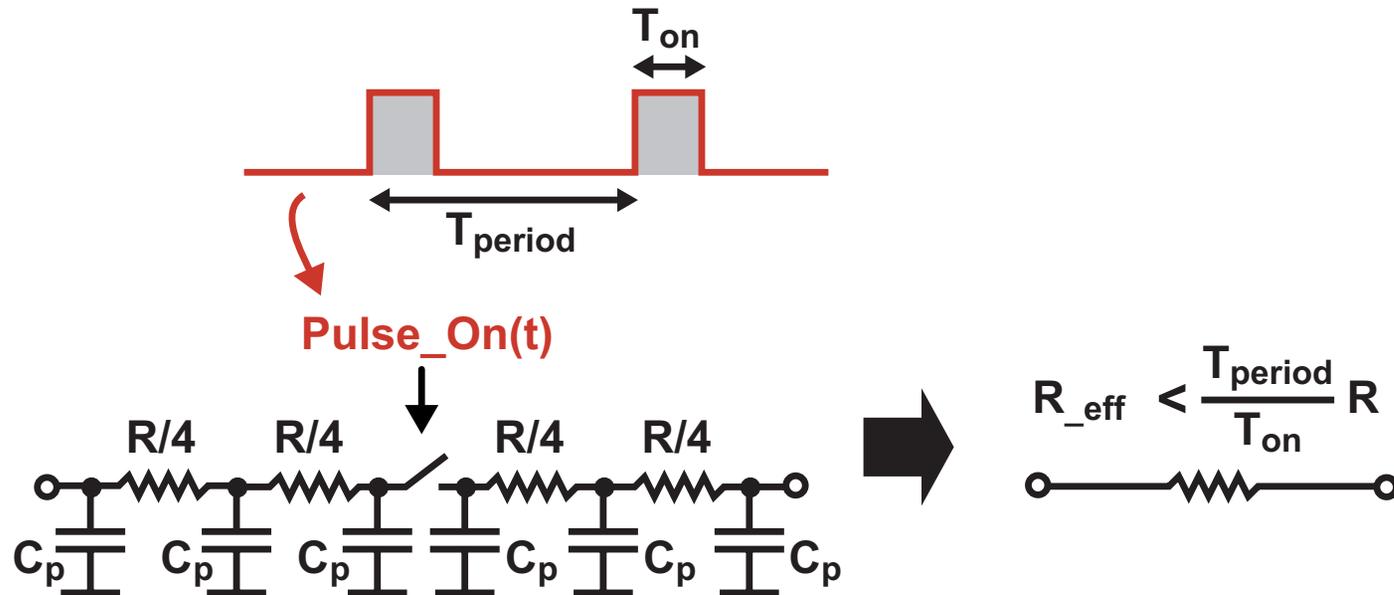
Pulsing Resistor Multiplies Resistance!



- Resistor only passes current when pulsed on
 - Average current through resistance is reduced according to ratio of On time, T_{on} , versus pulsing Period, T_{period}
 - *Effective* resistance is actual resistance *multiplied* by ratio $T_{\text{period}}/T_{\text{on}}$

Resistor multiplication allows a large RC time constant to be implemented with smaller area

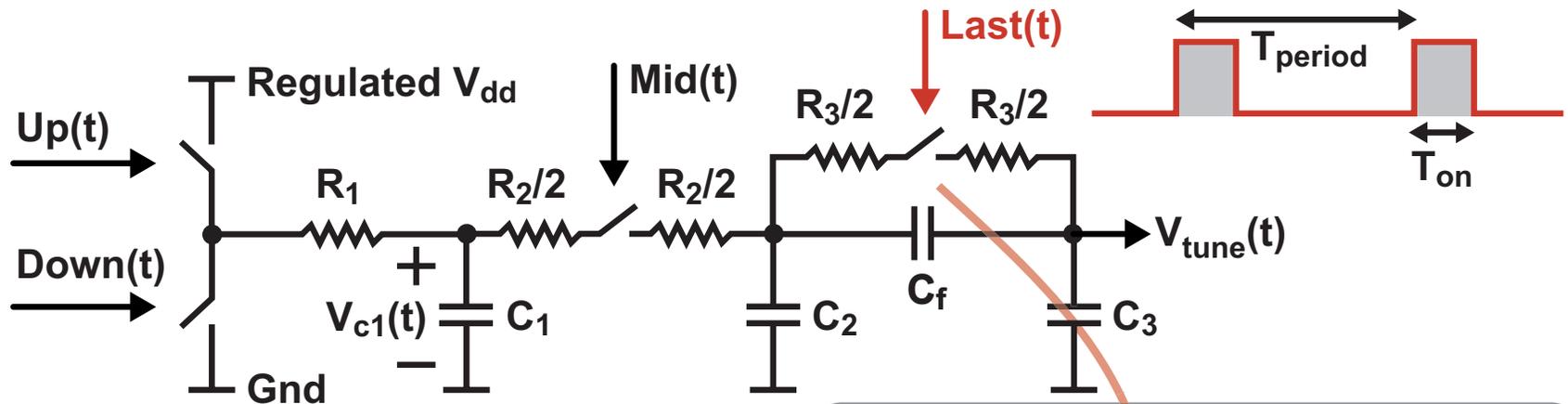
Parasitic Capacitance Reduces Effective Resistance



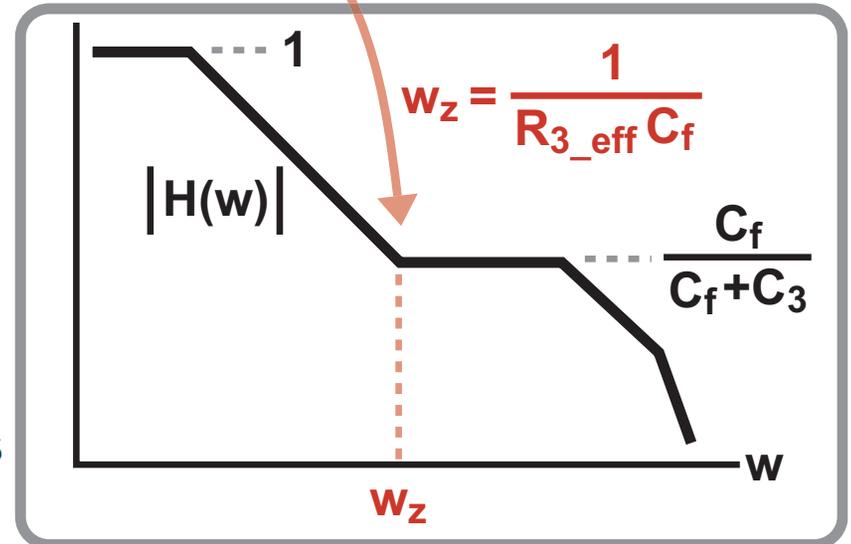
- Parasitic capacitance stores charge during the pulse “On” time
 - Leads to non-zero current through resistor during pulse Off time
 - Effective resistance reduced

Spice simulation and measured results reveal that >10X resistor multiplication can easily be achieved

Switched Resistor Achieves PLL Zero with Low Area

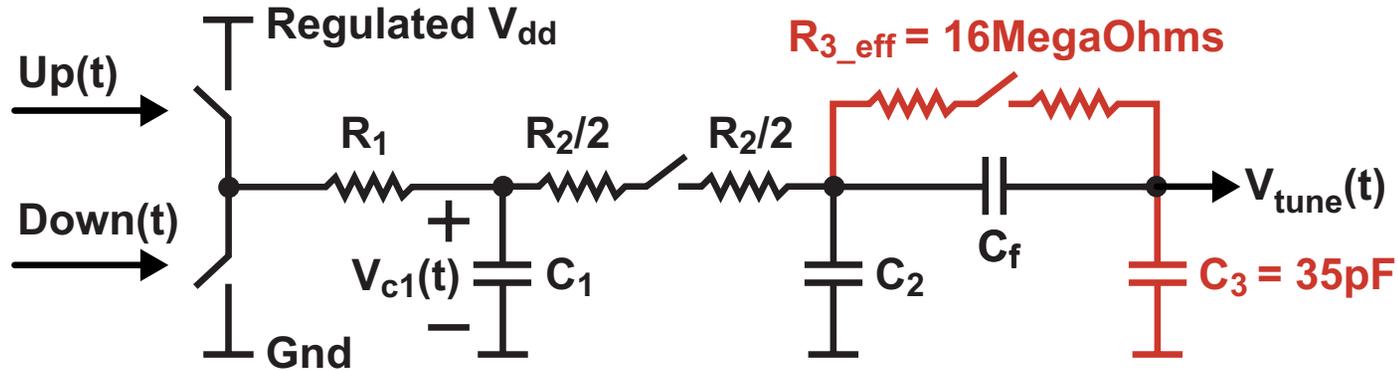


- For robust stability, PLL zero should be set well below PLL bandwidth of 30 kHz
 - Assume desired $w_z = 4$ kHz
 - Set $C_f = 2.5$ pF (for low area)
 - Required $R_{3_eff} = 16$ MegaOhms
 - Large area



Proper choice of T_{on} and T_{period} allows $R_{3_eff} = 16$ MegaOhms to be achieved with $R_3 = 500$ kOhms!

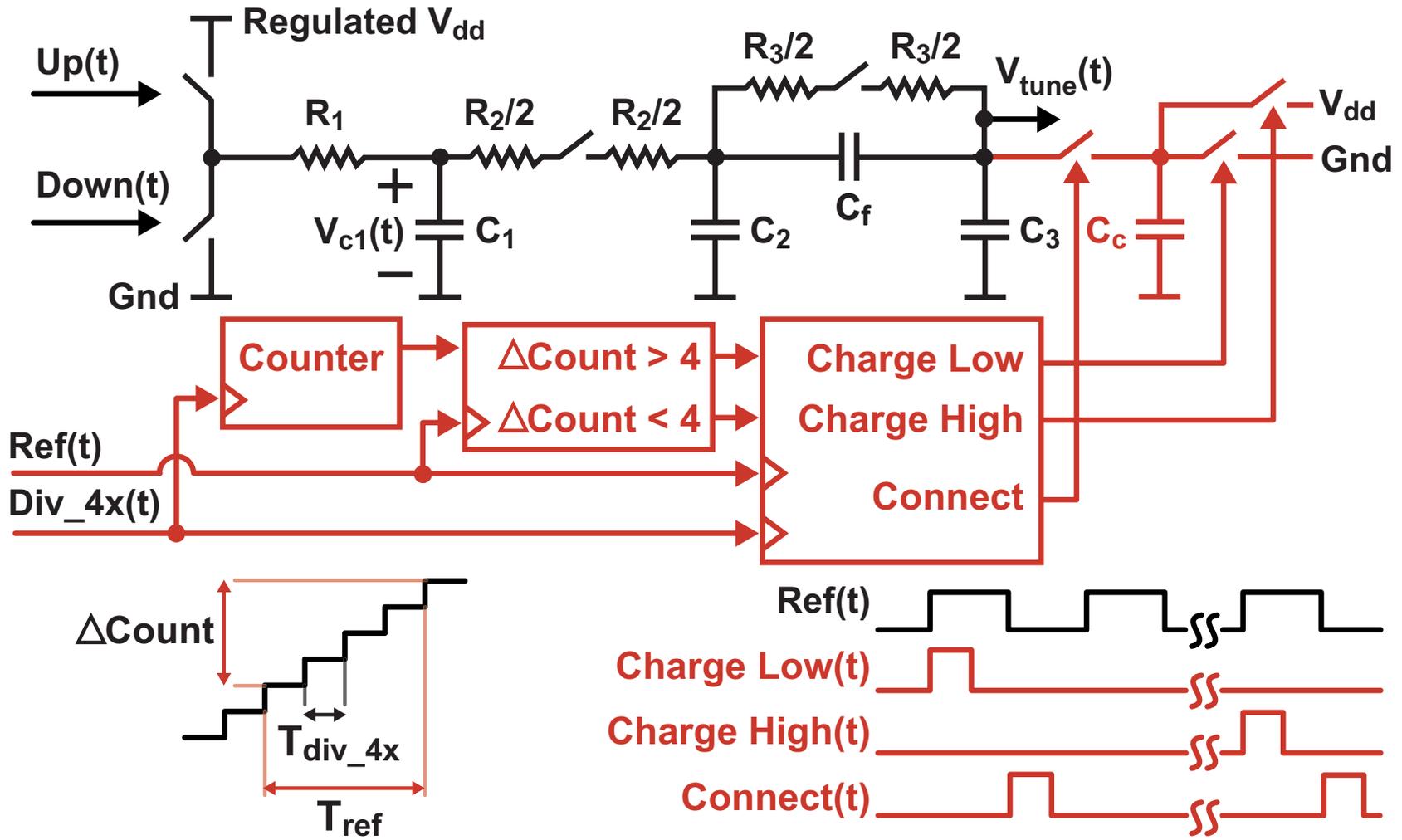
The Issue of Initial Frequency Acquisition



- During initial frequency acquisition, $V_{tune}(t)$ must be charged to proper bias point
 - This takes too long with $R_{3_eff} = 16\text{ MegaOhms}$

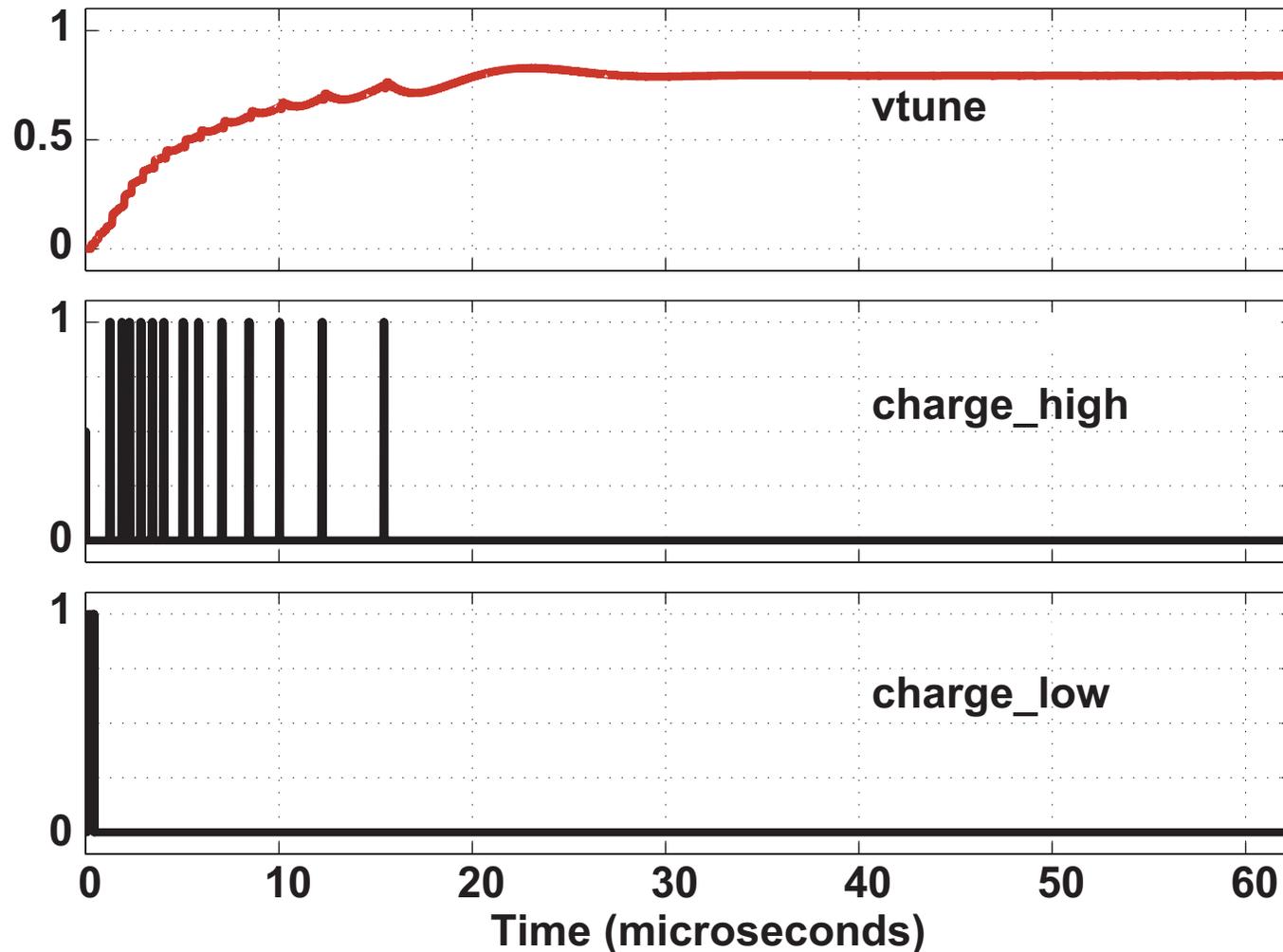
How do we quickly charge capacitor C_3 during initial frequency acquisition?

Utilize Switched Capacitor Charging Technique



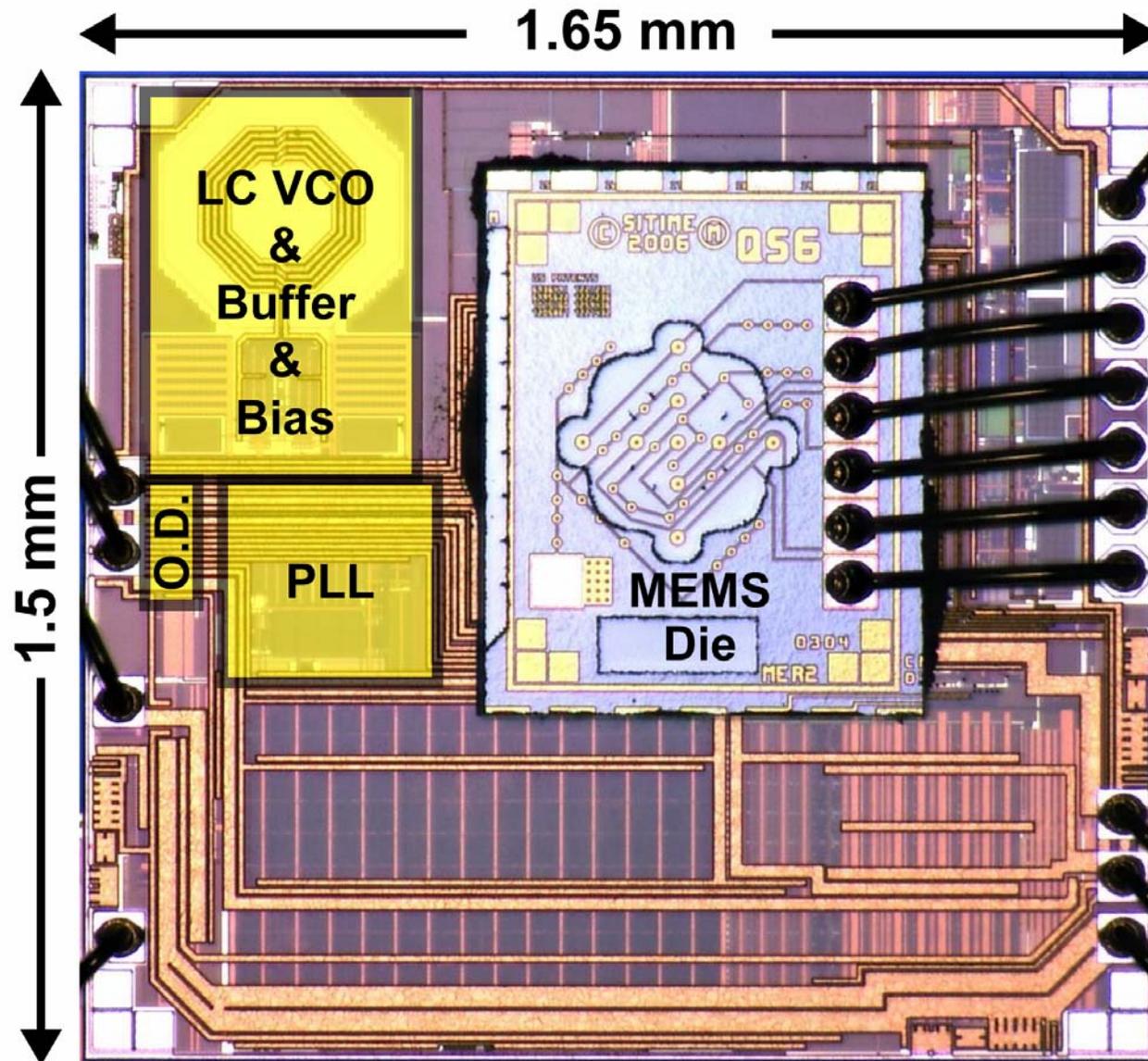
- Charge C_3 high or low only when frequency error is detected
 - No steady-state noise penalty, minimal power consumption

CppSim Behavioral Simulation of Frequency Locking



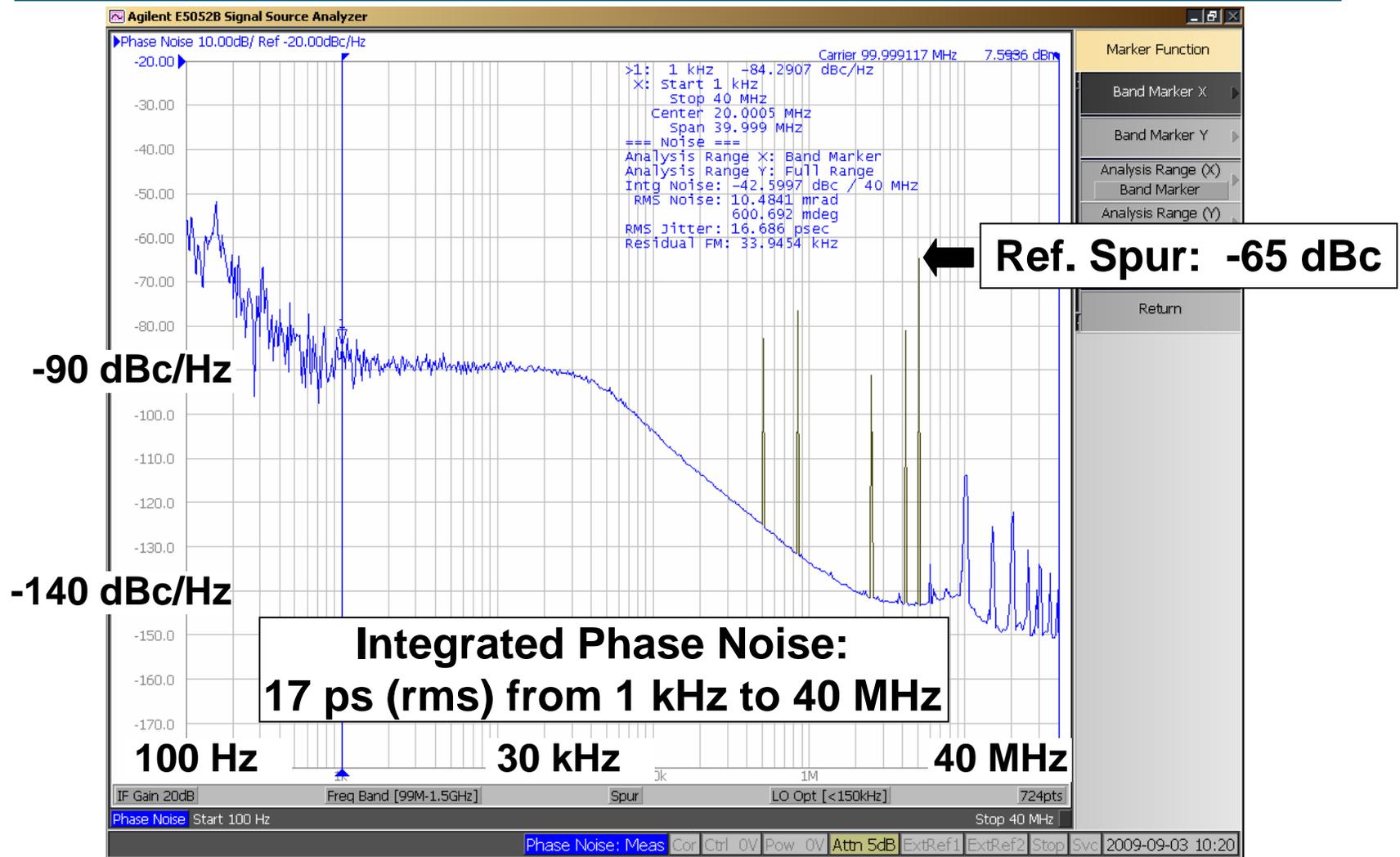
Switched capacitor technique allows relatively fast frequency locking

CMOS and MEMS Die Photos Show Low Area of PLL



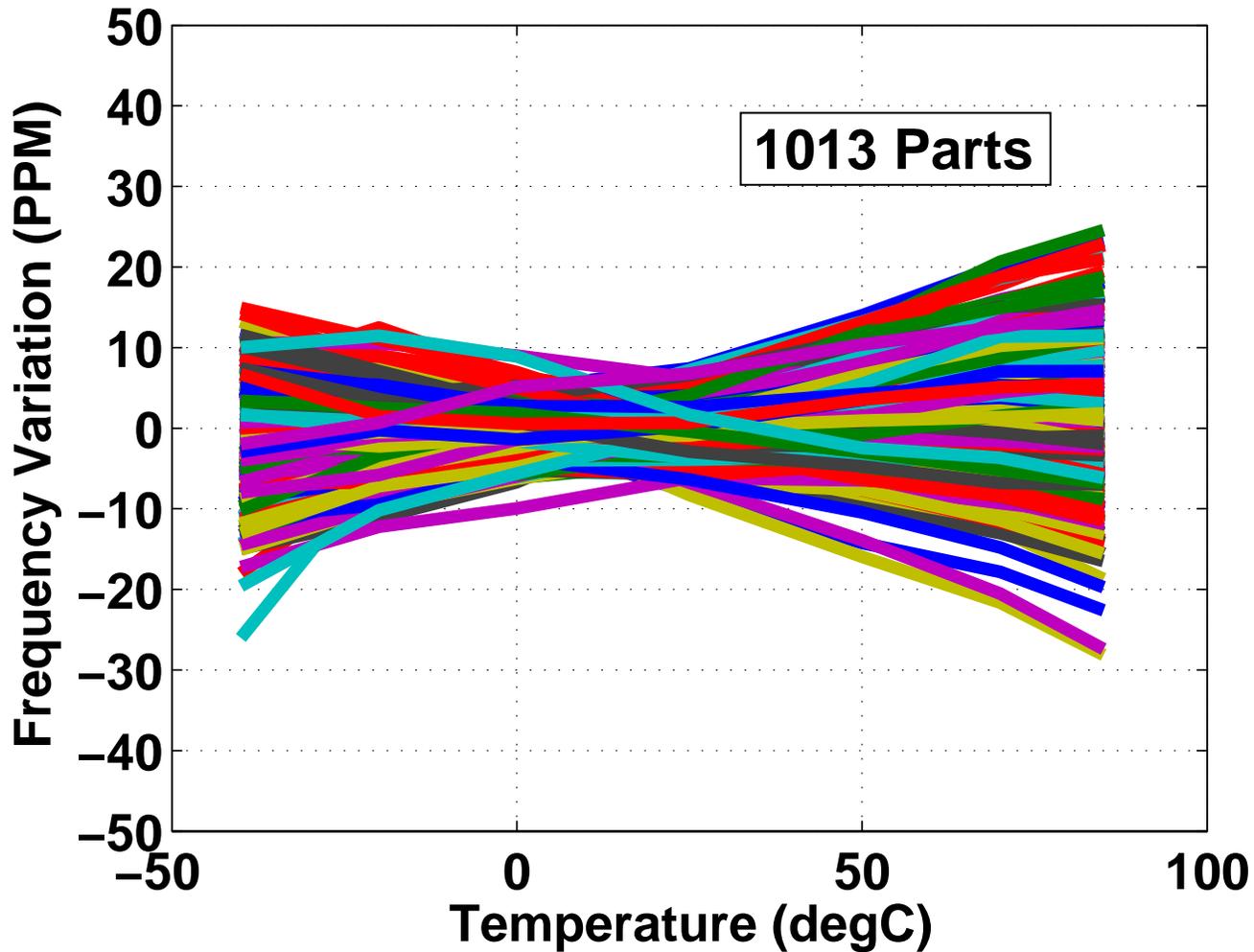
- **Active area:**
 - VCO & buffer & bias: 0.25mm²
 - PLL (PFD, Loop Filter, divider): 0.09 mm²
 - Output divider: 0.02 mm²
- **External supply**
 - 1.8/3.3V
- **Current (20 MHz output, no load)**
 - ALL: 3.2/3.7mA
 - VCO: 1.3mA
 - PLL & Output Divider: 0.7mA

Measured Phase Noise (100 MHz output)



- Suitable for most serial applications, embedded systems and FPGAs, audio, USB 1.1 and 2.0, cameras, TVs, etc.

Frequency Variation After Single-Temperature Calibration



**< 30 ppm across industrial temperature range
with single-temperature calibration**

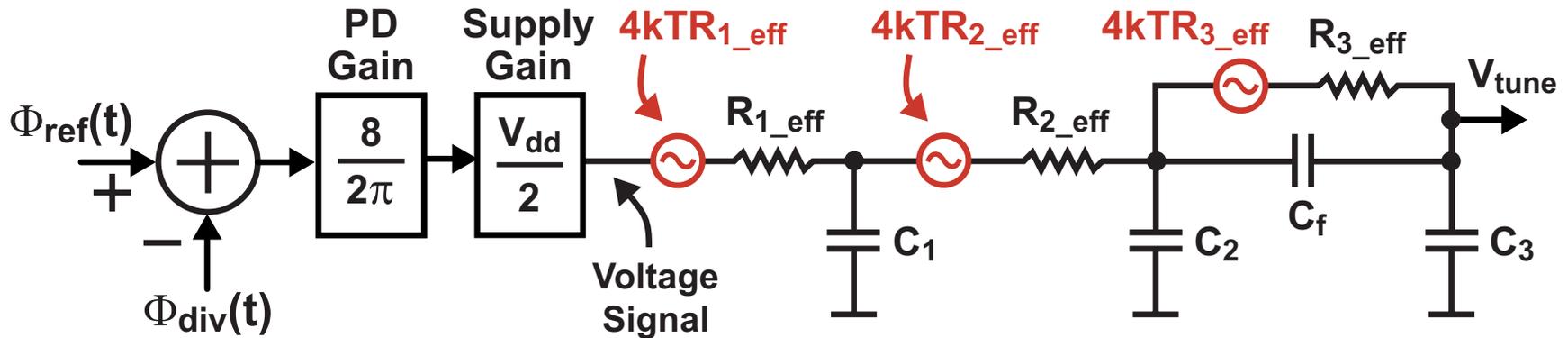
Conclusion

- **A MEMS-based programmable oscillator provides an efficient solution for industrial clocking needs**
 - Programmability of frequency value simplifies supply chain and inventory management
 - Leveraging of semiconductor processing, rather than custom tools for quartz, allows low cost and low lead times
- **Proposed fractional-N synthesizer allows low area, low power, and reduced analog design effort**
 - High gain phase detector lowers impact of loop filter noise
 - Switched resistor technique eliminates the charge pump and reduces area through resistor multiplication
 - Switched capacitor frequency detection enables reasonable frequency acquisition time with no noise penalty

Frequency references have entered the realm of integrated circuit design and manufacturing

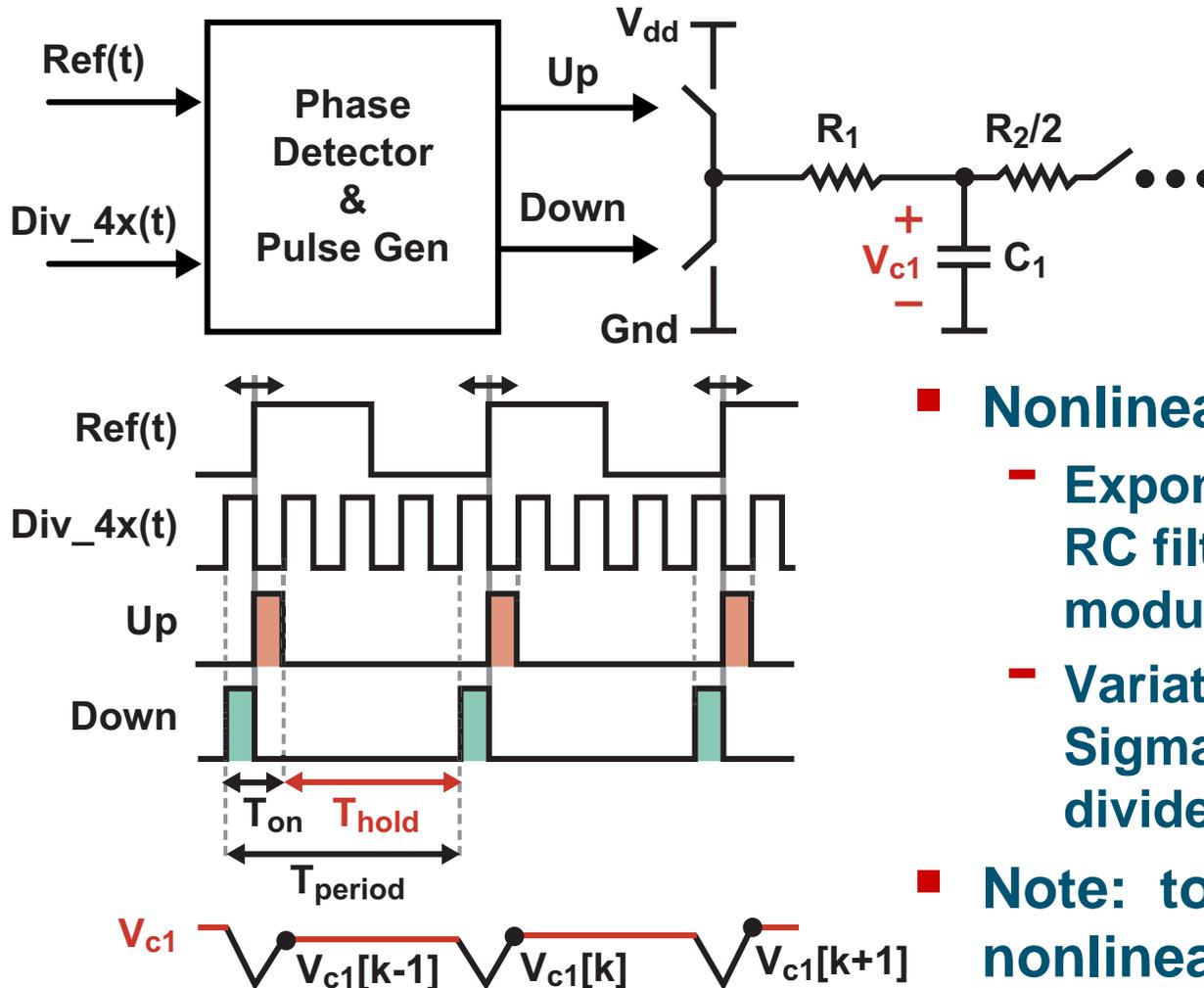
Supplemental Slides

Noise Analysis (Ignore Parasitic Capacitance of Resistors)



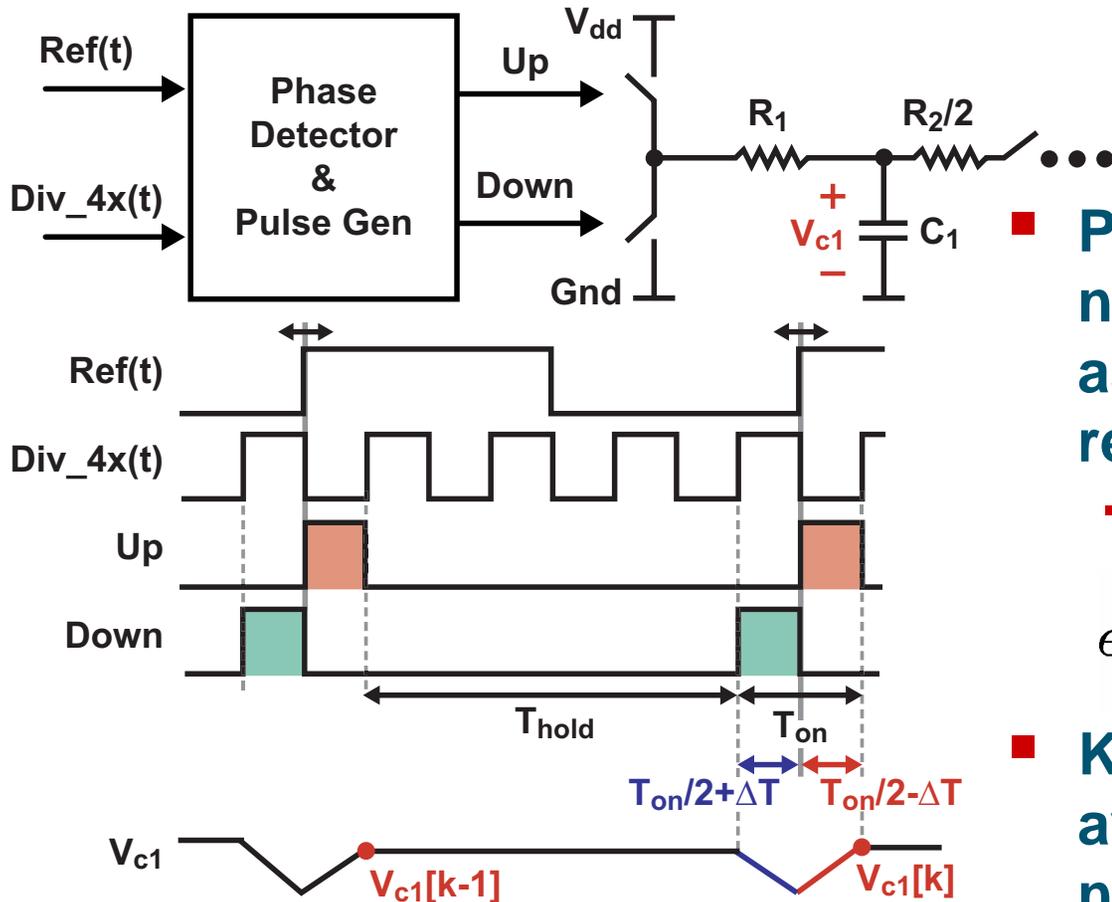
- **Assumption:** switched resistor time constants are much longer than “on time” of switches
 - Single-sided voltage noise contributed by each resistor is simply modeled as $4kTR_{\text{eff}}$ (same as for a resistor of the equivalent value)
- **Note:** if switched resistor time constants are shorter than “on time” of switches
 - Resistors contribute kT/C noise instead of $4kTR_{\text{eff}}$
 - We would not want to operate switched resistor filter in this domain since time constants would not be boosted

Issue: Nonlinearity in Switched Resistor Loop Filter



- **Nonlinearity is caused by**
 - Exponential response of RC filter to pulse width modulation
 - Variation of T_{hold} due to Sigma-Delta dithering of divide value
- **Note: to avoid additional nonlinearity, design divide value control logic to keep T_{on} a constant value**

Nonlinearity Due to Pulse Width Modulation



■ Pulse width modulation nonlinearity is reduced as ratio $\Delta T/(R_1 C_1)$ is reduced

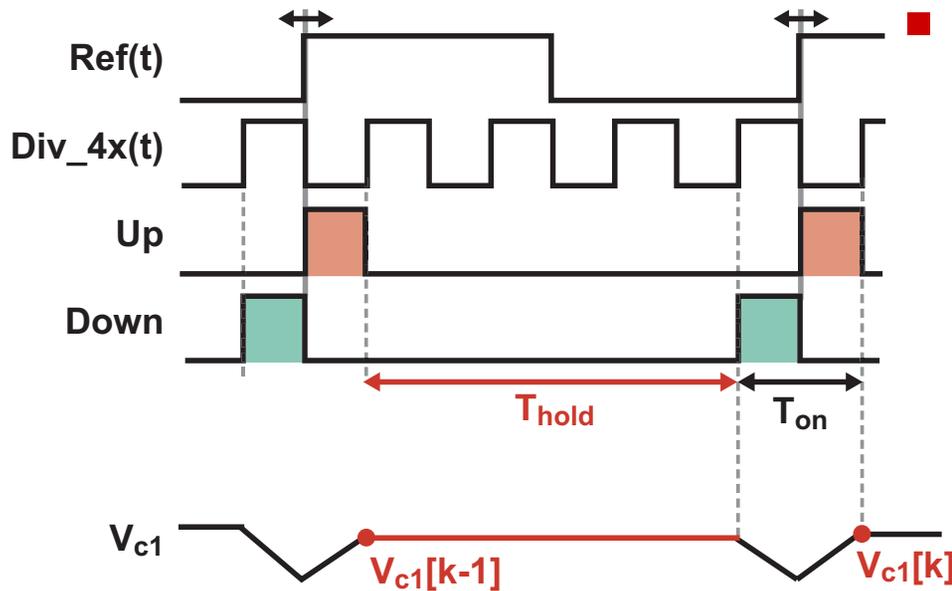
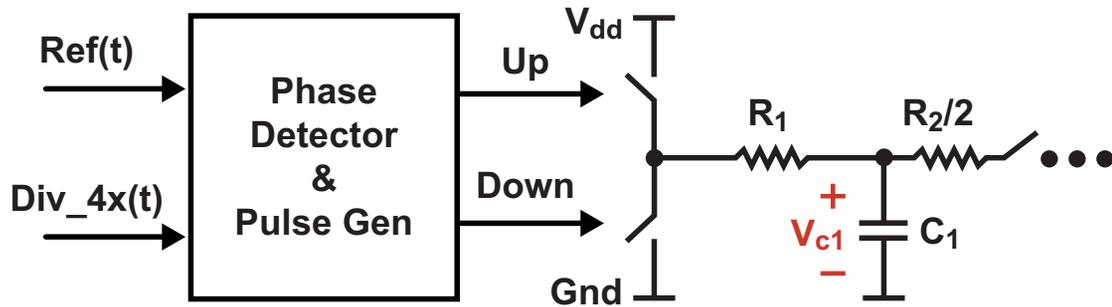
■ If $\Delta T/(R_1 C_1)$ is small:

$$e^{\frac{1}{R_1 C_1} \Delta T} \approx 1 + \frac{\Delta T}{R_1 C_1}$$

■ Keep T_{on} constant to avoid increased nonlinearity!

$$V_{c1}[k] = V_{dd} e^{-\frac{1}{R_1 C_1} \frac{T_{on}}{2}} e^{\frac{1}{R_1 C_1} \Delta T} + e^{-\frac{T_{on}}{R_1 C_1}} (V_{c1}[k-1] - V_{dd})$$

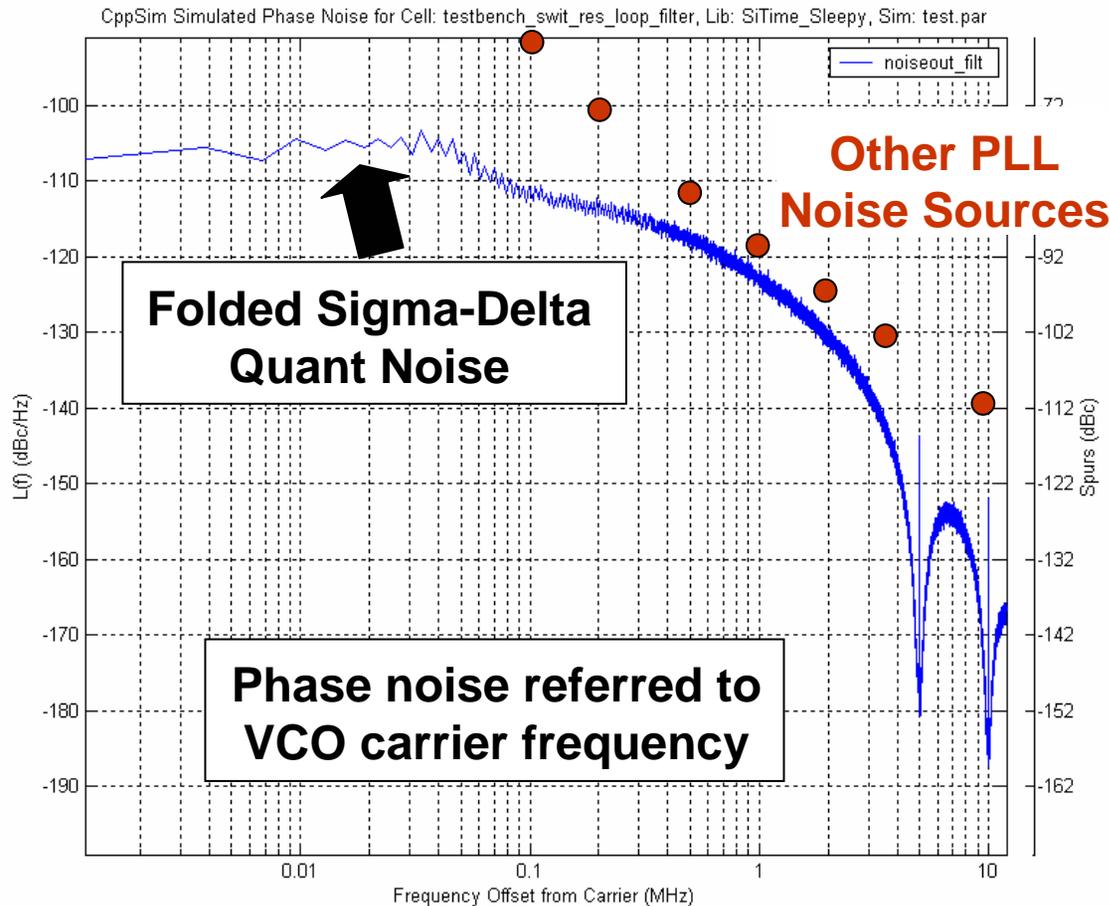
Nonlinearity Due to Hold Time Variation



■ Hold time nonlinearity is reduced as changes in T_{hold} (due to divide value dithering) are reduced

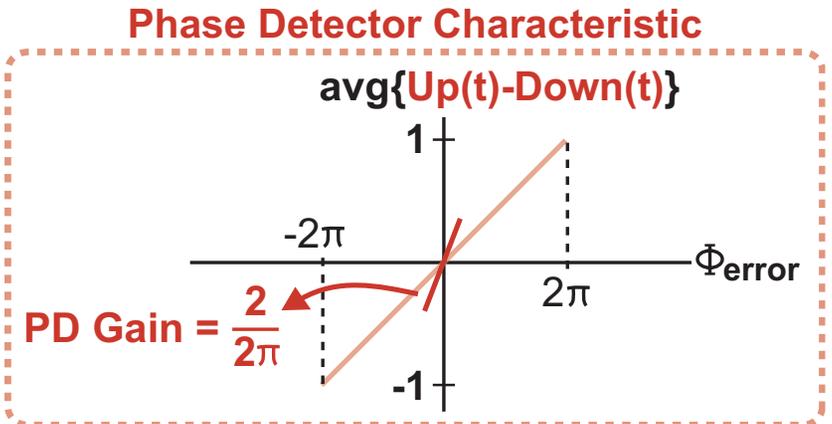
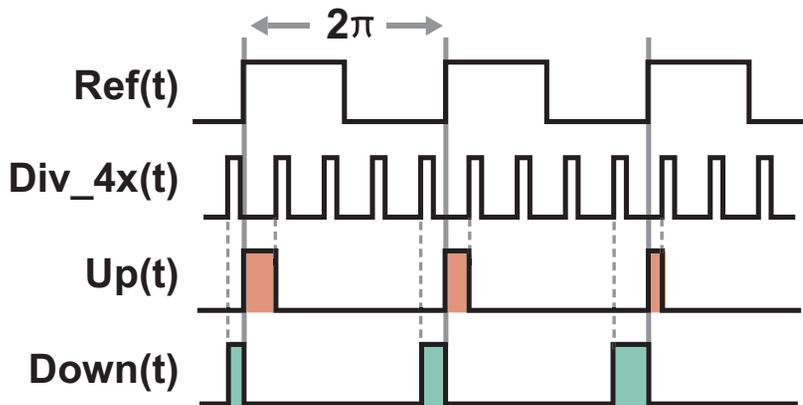
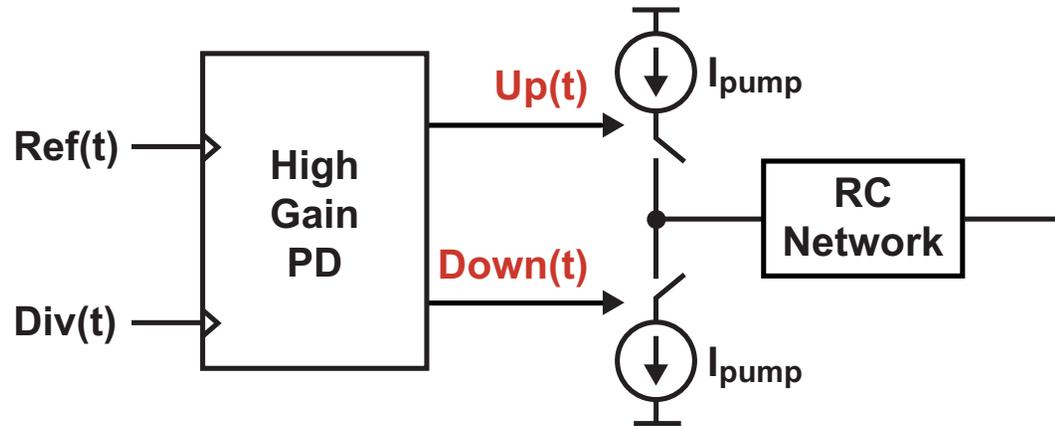
- Reduce order of MASH $\Sigma-\Delta$
 - Benefits are offset by reduced noise shaping of lower order Sigma-Delta
- Reduce step size of MASH $\Sigma-\Delta$
 - Achieved with higher VCO frequency

Nonlinearity Is Not An Issue For This Design



- **Folded quantization noise due to nonlinearity is reasonably below other noise sources for this design**
 - However, could be an issue for a wide bandwidth PLL design
- **Use (CppSim) behavioral simulation to evaluate this issue**

What If We Use A Pure Charge Pump Loop Filter?



- PD Gain increased by 2 compared to tristate PFD
 - Reduced phase error range and max/min current occurs
- High linearity despite charge pump current mismatch
 - Similar to XOR PD, but noise is reduced