Design Techniques for Analog PLLs: Moving Beyond Classical Topologies

CICC 2010

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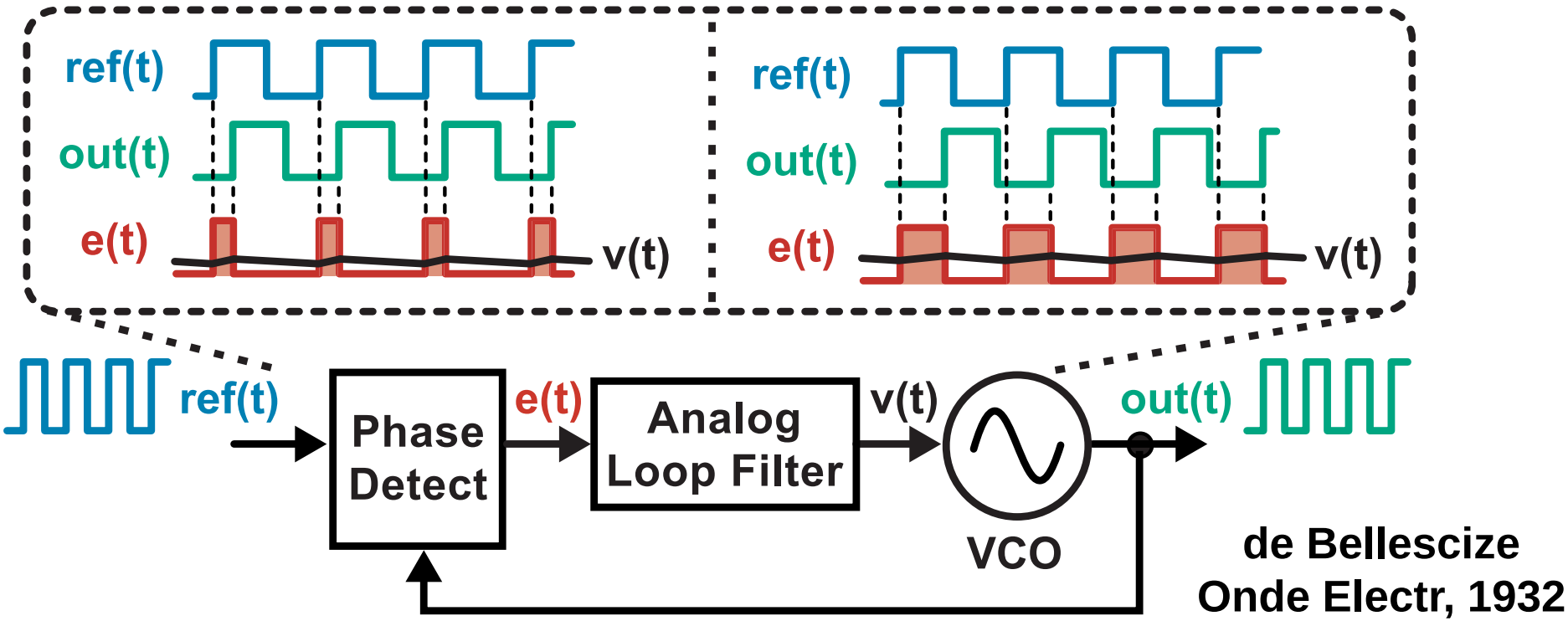
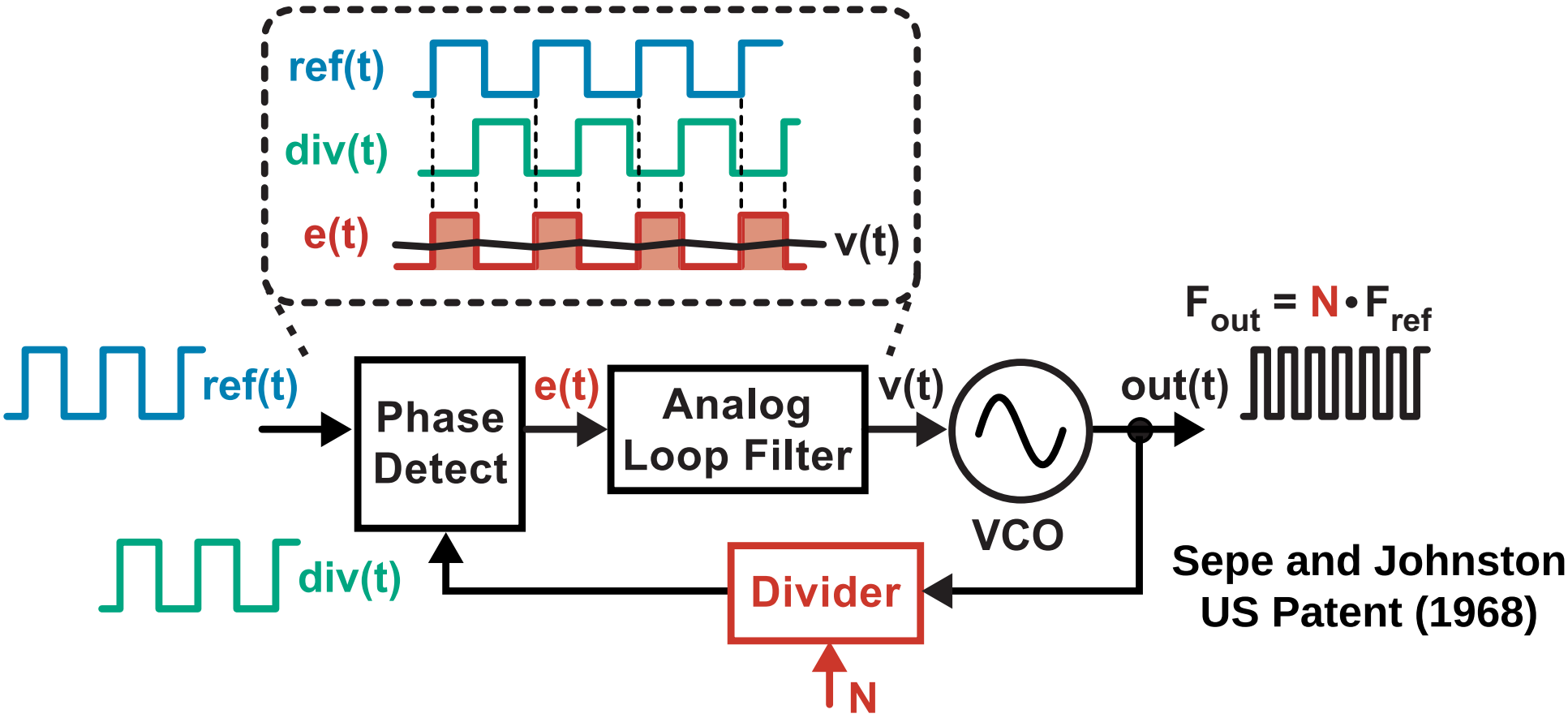
What is a Phase-Locked Loop (PLL)?



- **VCO efficiently provides oscillating waveform with variable frequency**
- **PLL synchronizes VCO frequency to input reference frequency through feedback**
  - **Key block is phase detector**
    - Realized as *digital gates* that create pulsed signals

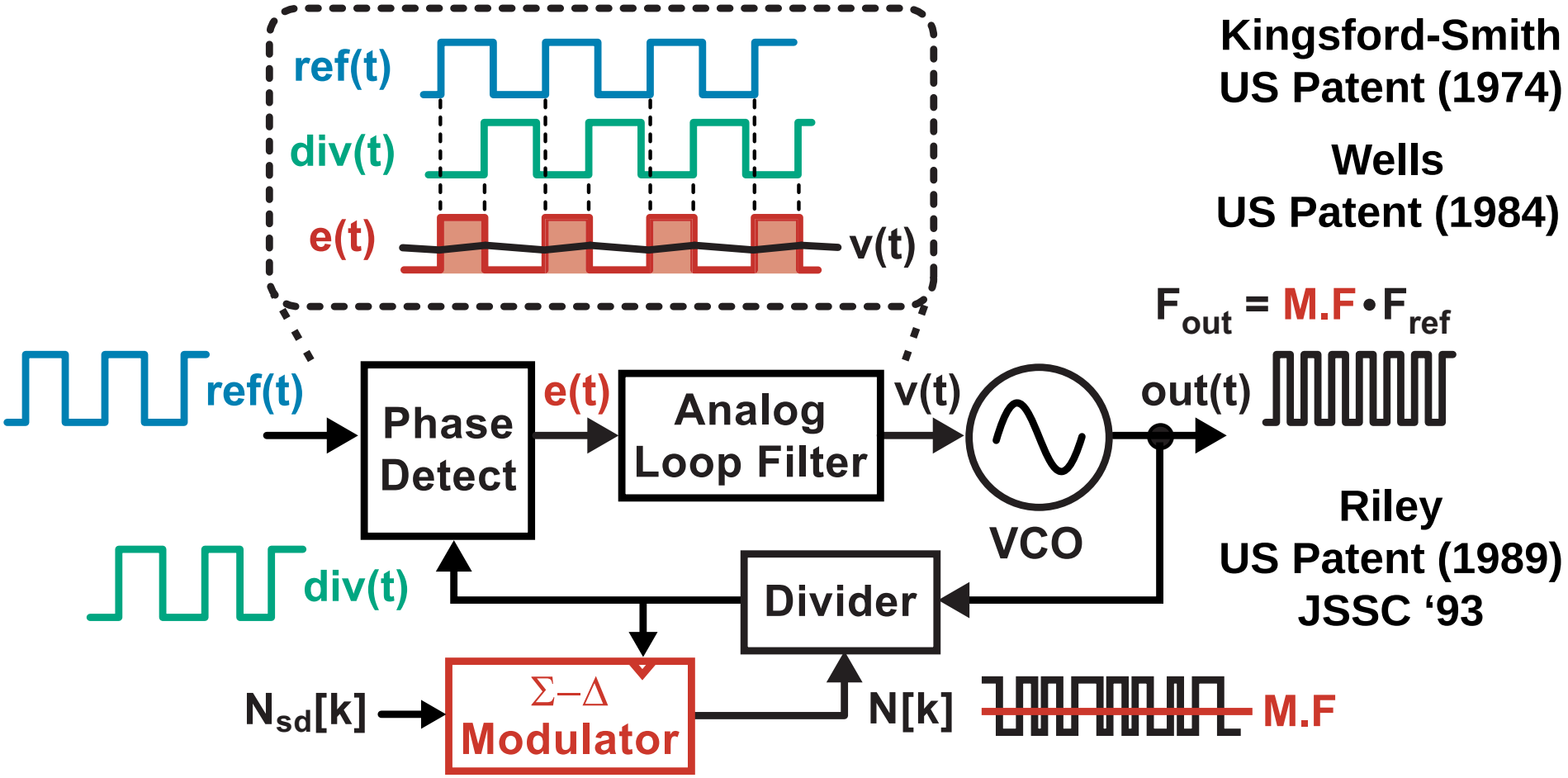
Integer-N Frequency Synthesizers



- Use digital counter structure to divide VCO frequency
  - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

Output frequency is digitally controlled

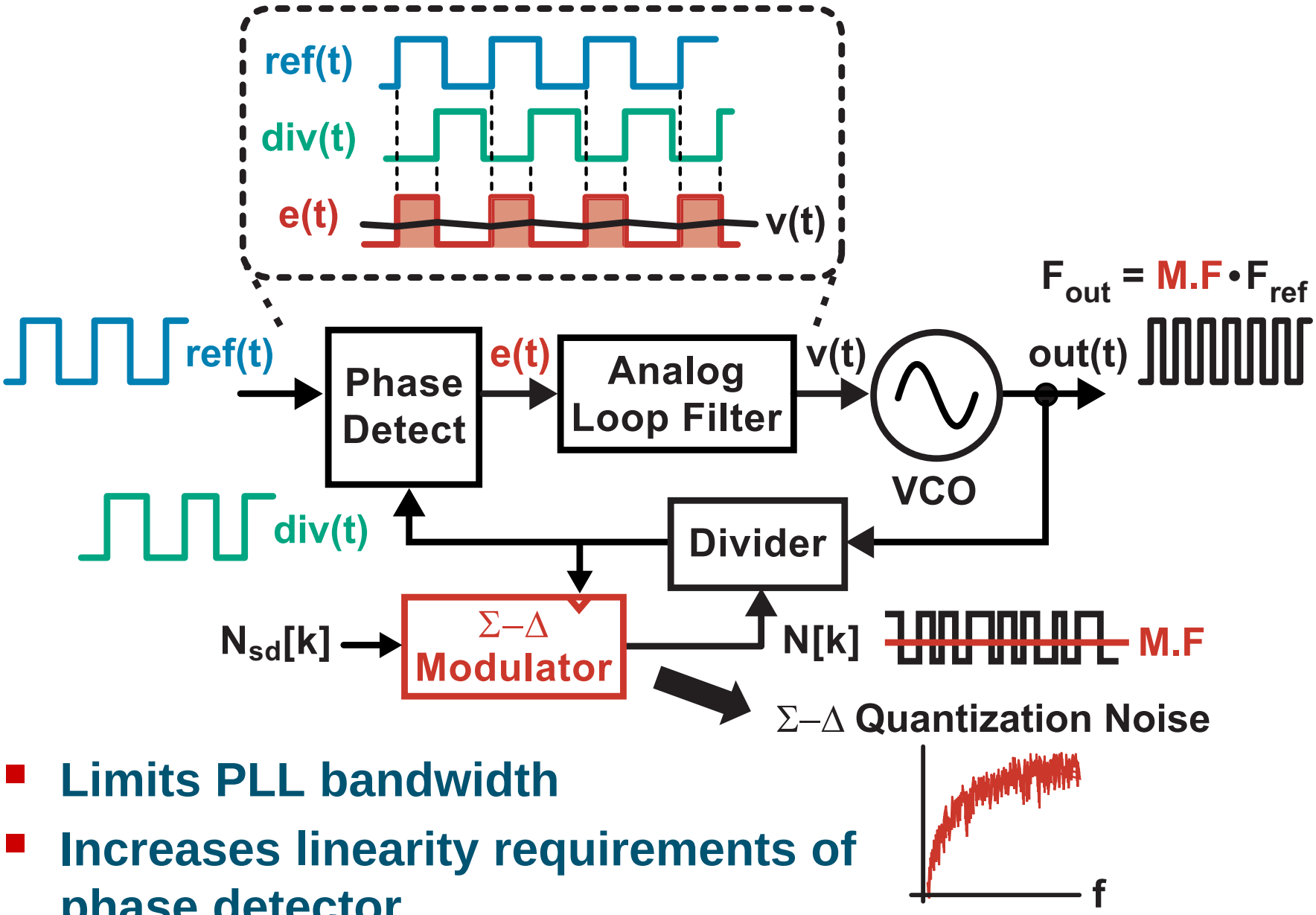
Fractional-N Frequency Synthesizers



- Dither divide value to achieve fractional divide values
  - PLL loop filter smooths the resulting variations

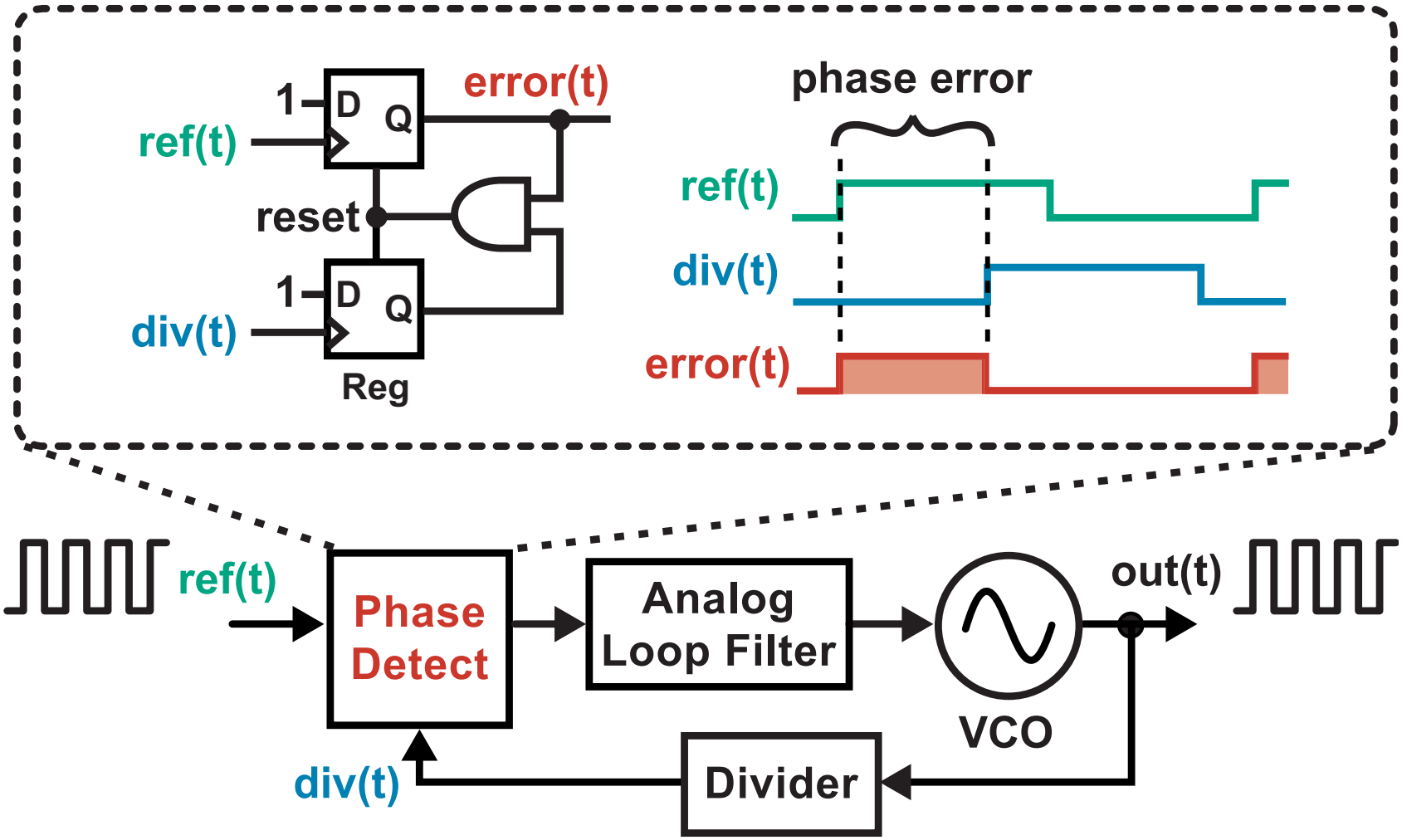
Very high frequency resolution is achieved

The Issue of Quantization Noise



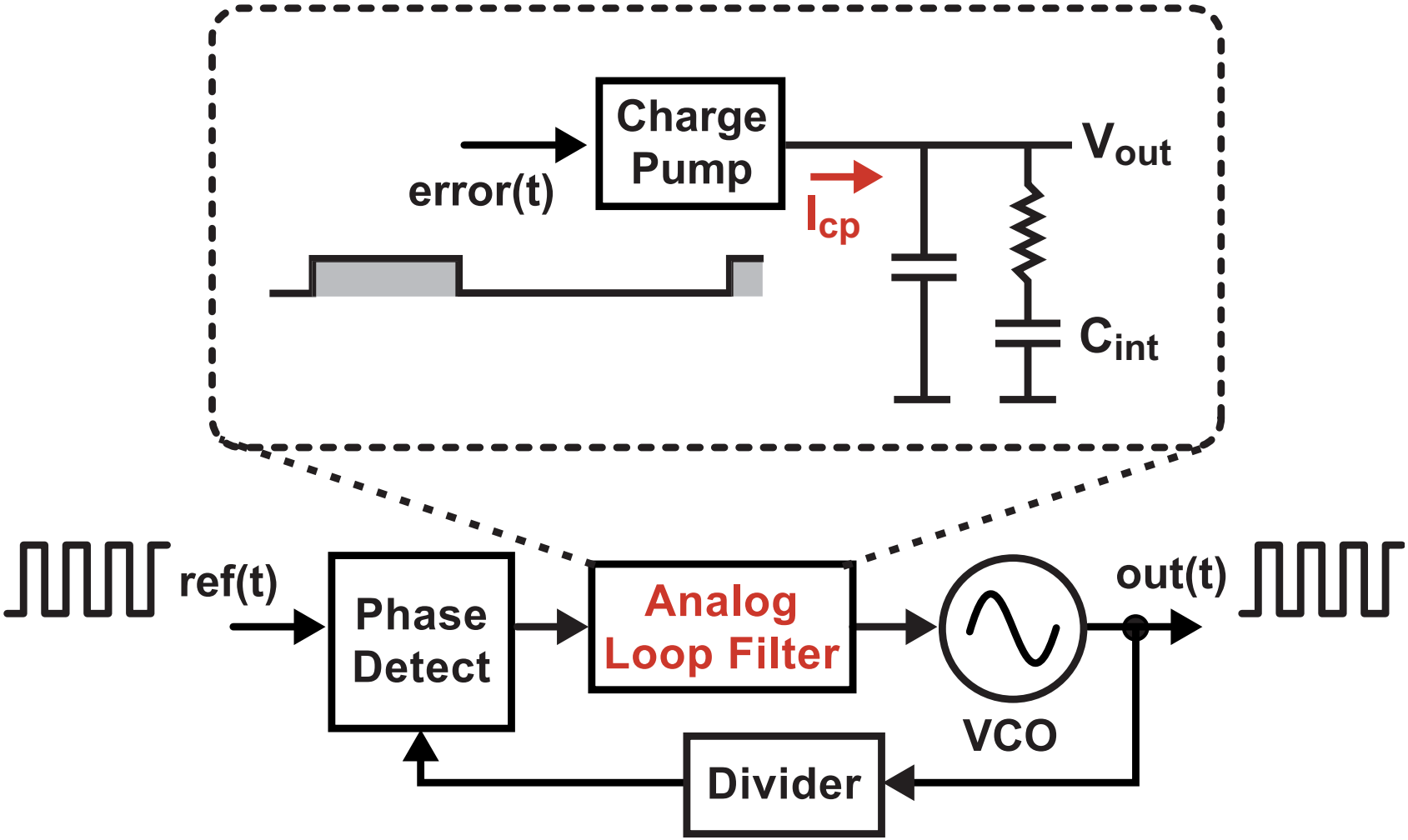
- Limits PLL bandwidth
- Increases linearity requirements of phase detector

Analog Phase Detection



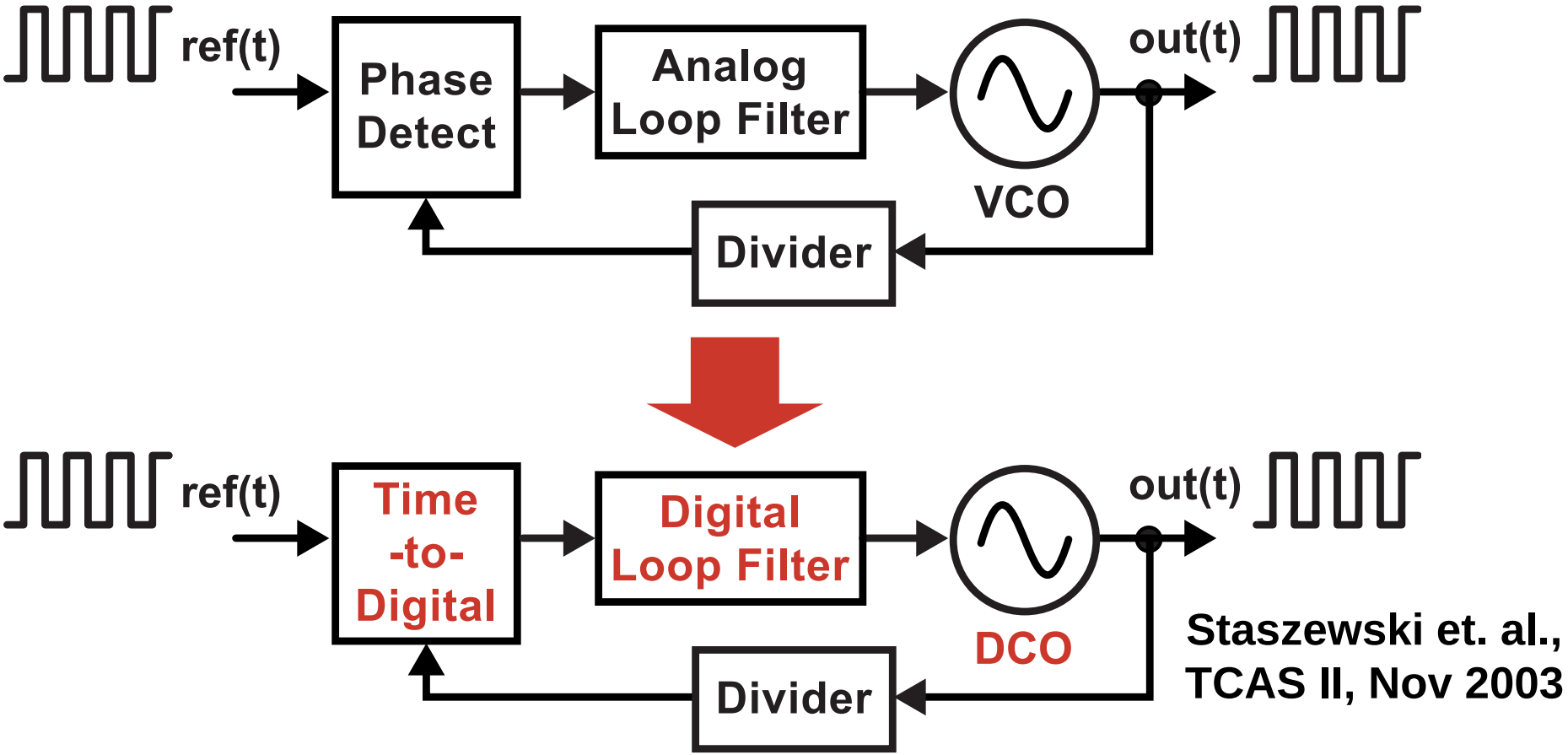
- Phase detector varies pulse width with phase error
- Loop filter smooths pulses to extract average value

Issues with Analog Loop Filter



- Charge pump: output resistance, mismatch, noise, leakage
  - Analog design requires significant effort, hard to port
- RC Network: large area

Should We Go All Digital ?



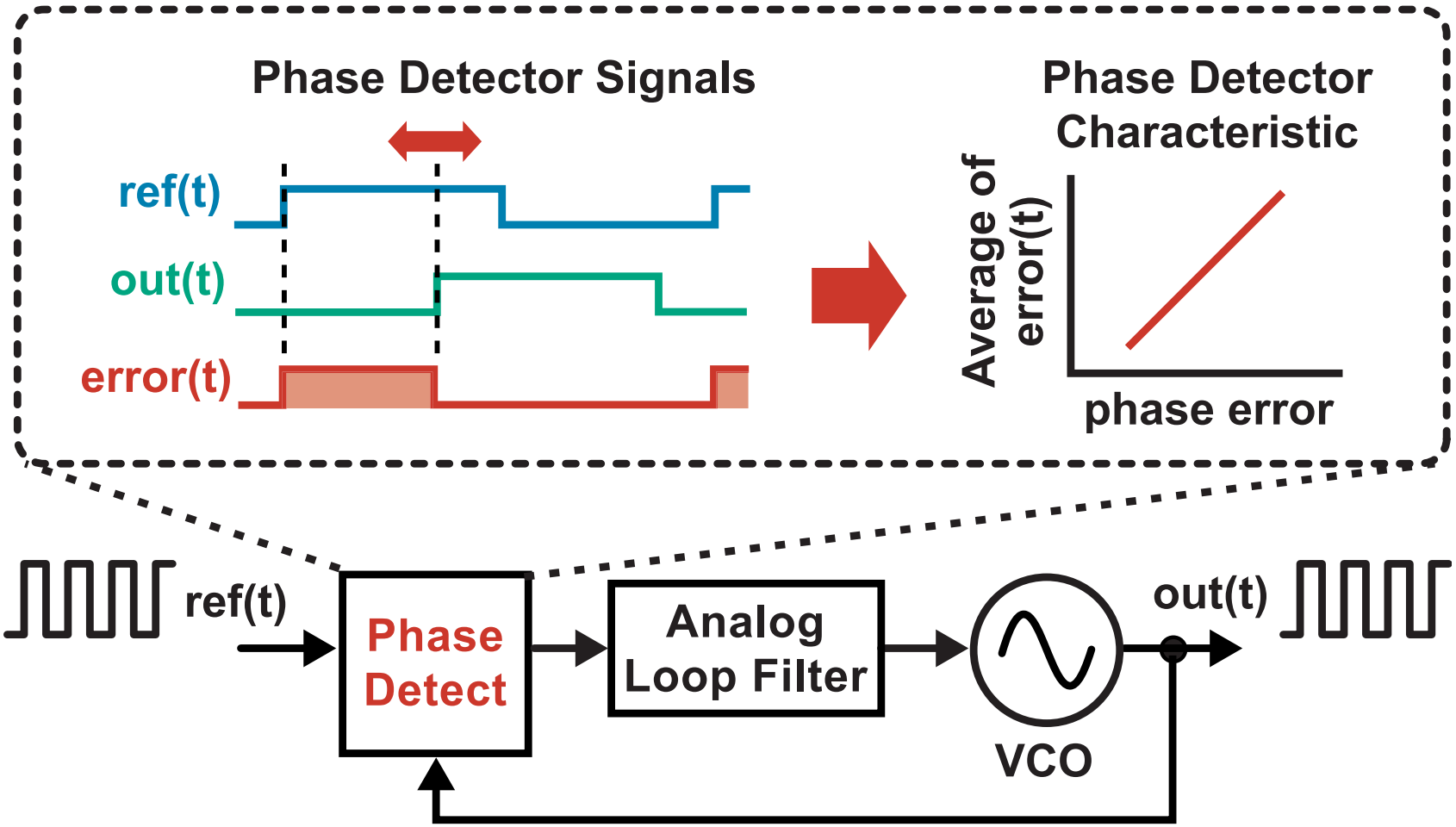
- Digital loop filter: compact area, digital flow
- Issue: difficult to achieve low area and power in older processes such as 0.18u CMOS
  - May not be worth the effort unless advanced CMOS available

Can We Achieve an Analog PLL with Lower Design Complexity and Adequate Performance?

Outline

- Background information on traditional analog PLL implementations and analysis
- Moving away from the traditional approach
  - XOR-based phase detection
  - Switched resistor loop filter
  - Switched capacitor frequency detection
- MEMS oscillator example

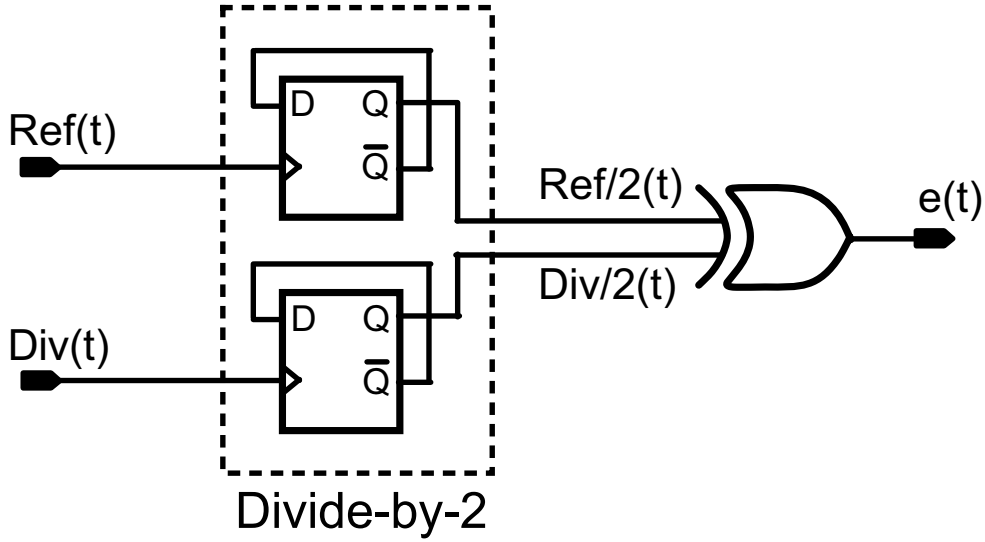
Key Characteristics of a Phase Detector

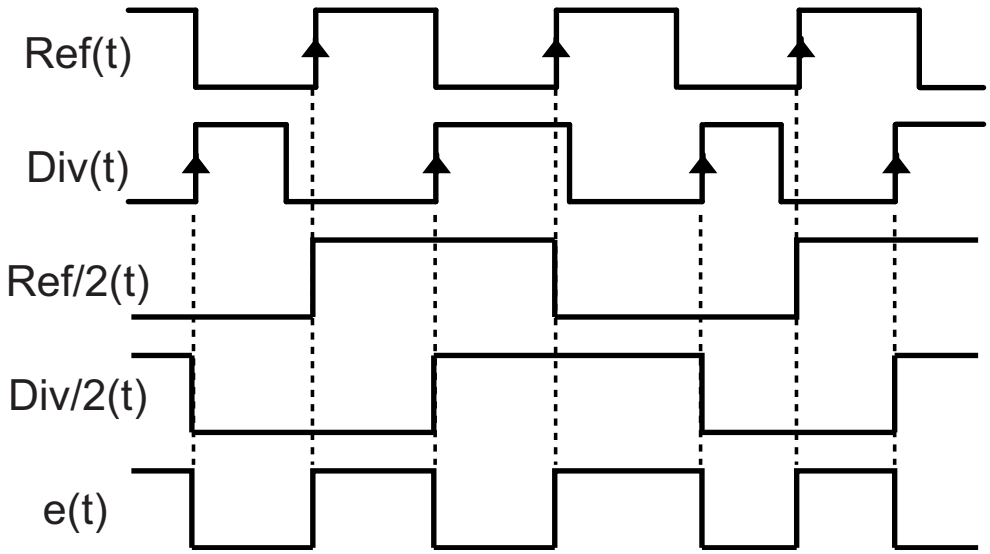


- Adequate phase detection range
  - Fractional-N PLLs need more range than Integer-N PLLs
- Linearity across operating range of phase detector
  - Fractional-N PLLs have issues with noise folding

XOR Phase Detector

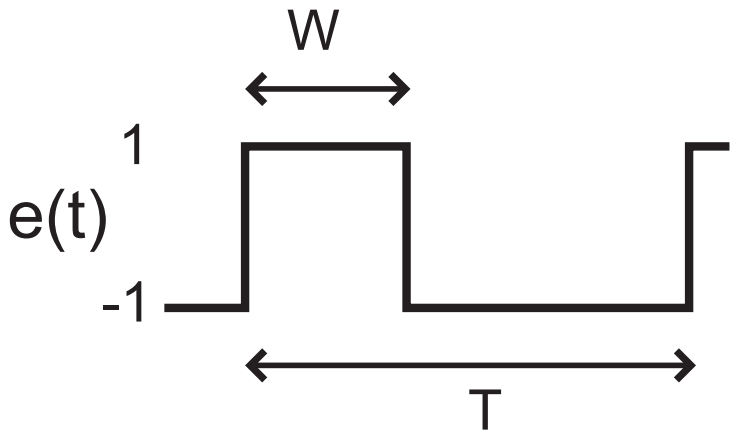
- Creates pulse widths that vary according to the phase difference between reference and divider output signals
- Simple implementation
- Divide-by-2 is used to eliminate impact of falling edges
  - Duty cycle of Ref(t) and Div(t) signals is no longer of concern





Modeling of XOR Phase Detector

- **Average value of pulses is extracted by loop filter**
  - **Look at detector output over one cycle:**

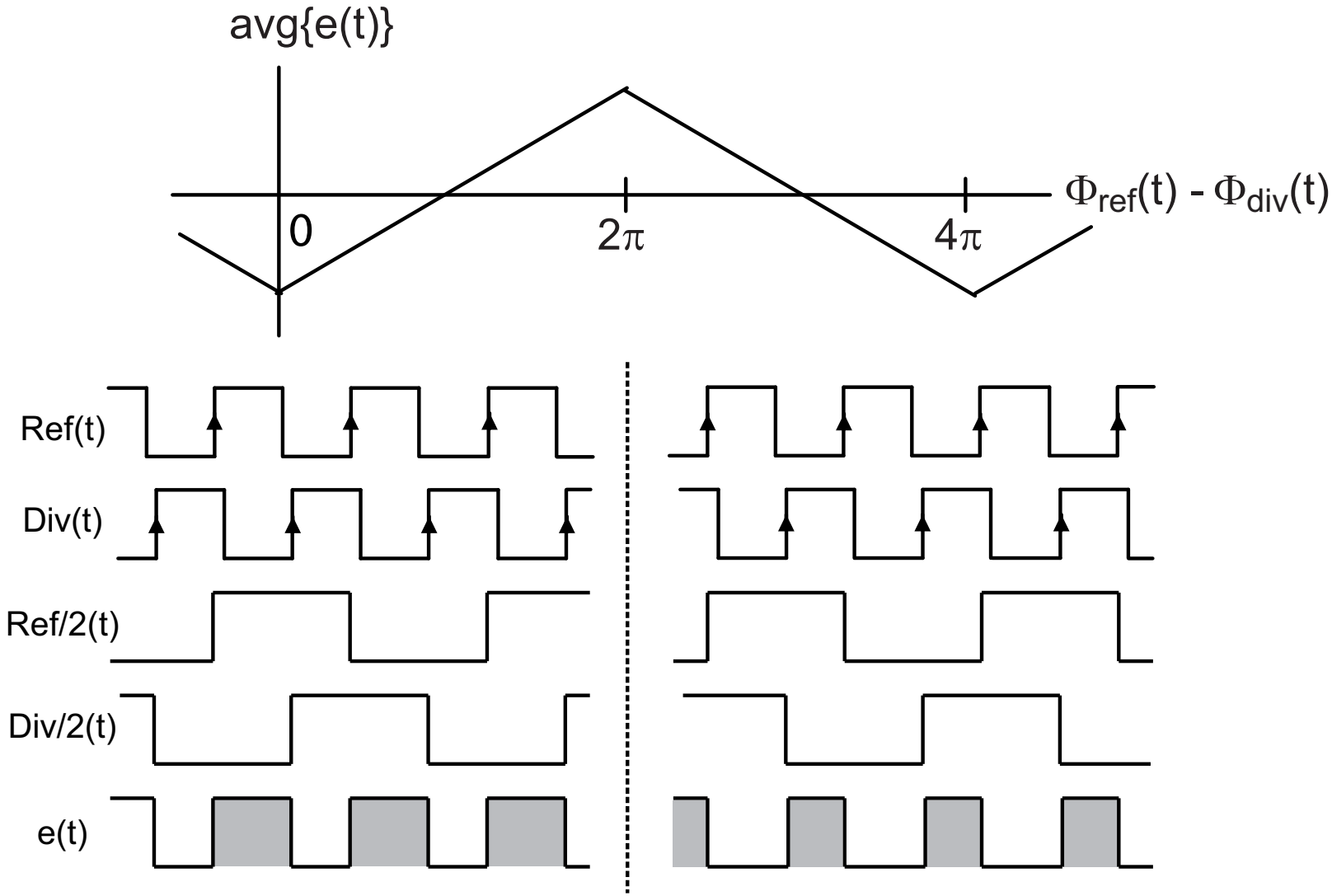


- **Equation:**

$$avg\{e(t)\} = -1 + 2\frac{W}{T}$$

Notice that the average error is a *linear* function of the pulse width *W* regardless of mismatch

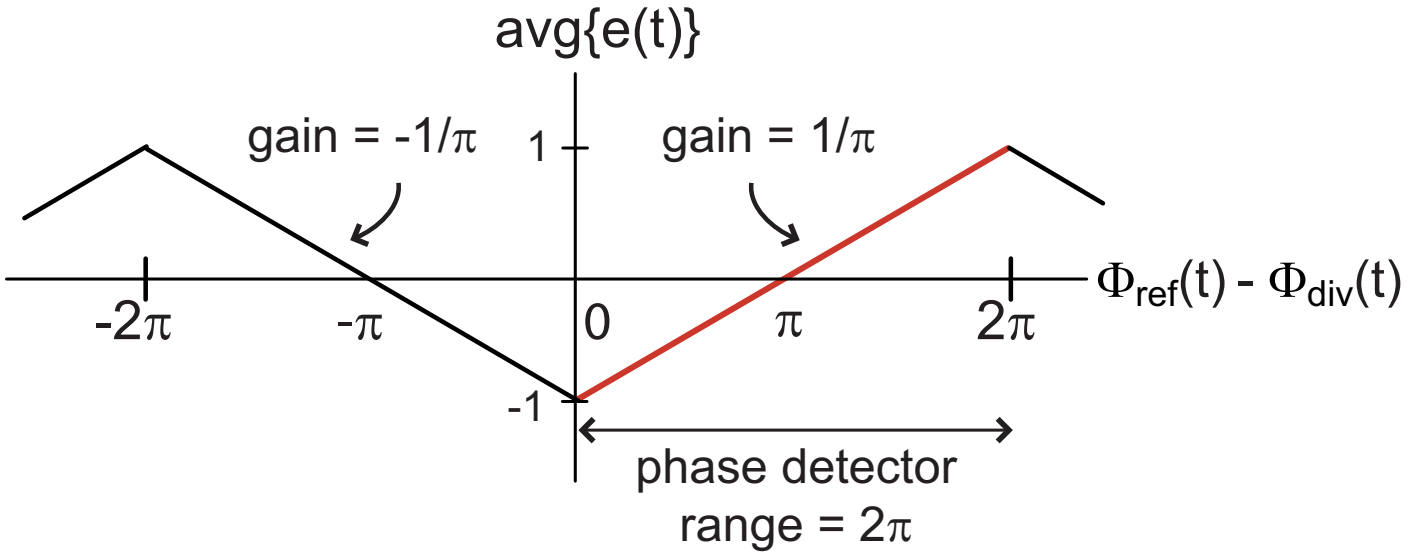
Overall XOR Phase Detector Characteristic



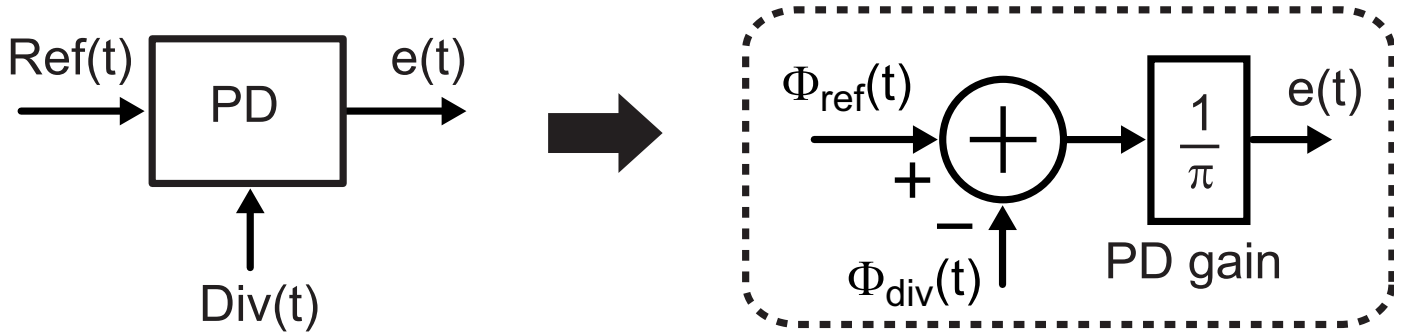
Gain flips in sign according to phase error region of phase detector

Modeling of XOR Phase Detector

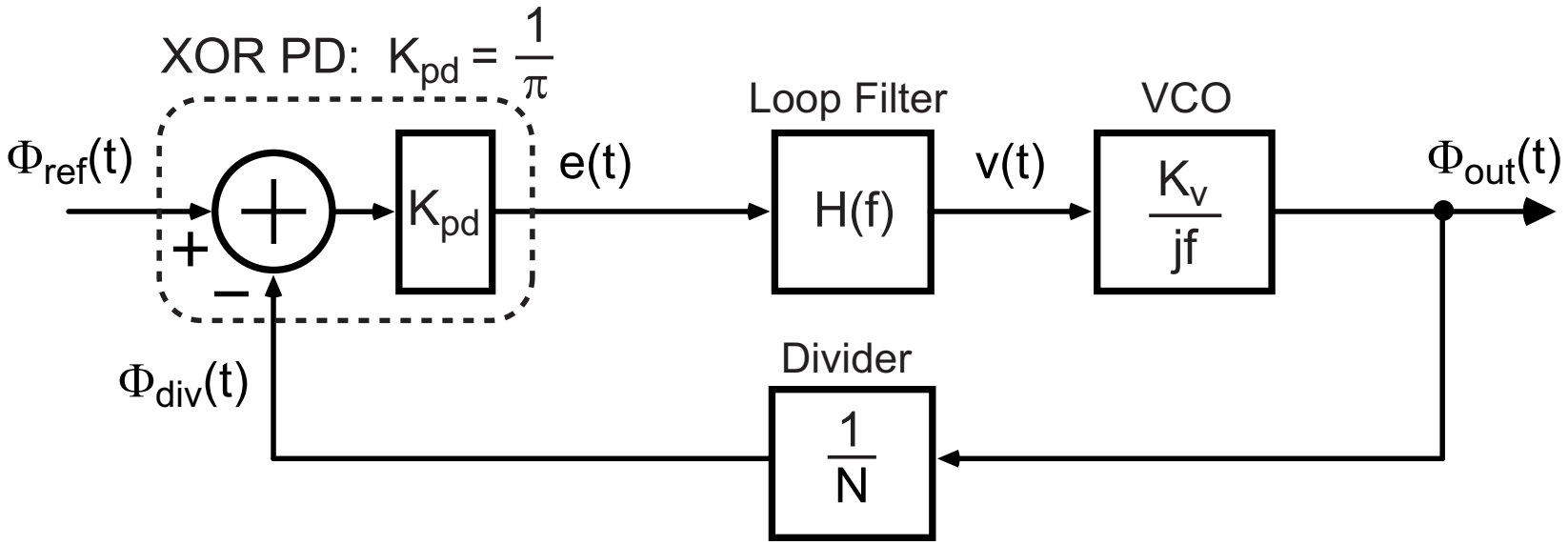
- **Assume phase difference is confined to same slope region**
  - **XOR PD model becomes a highly linear gain element**



- **Corresponding frequency-domain model**



Overall PLL Model with XOR Phase Detector



- **Define A(f) as *open loop* response**

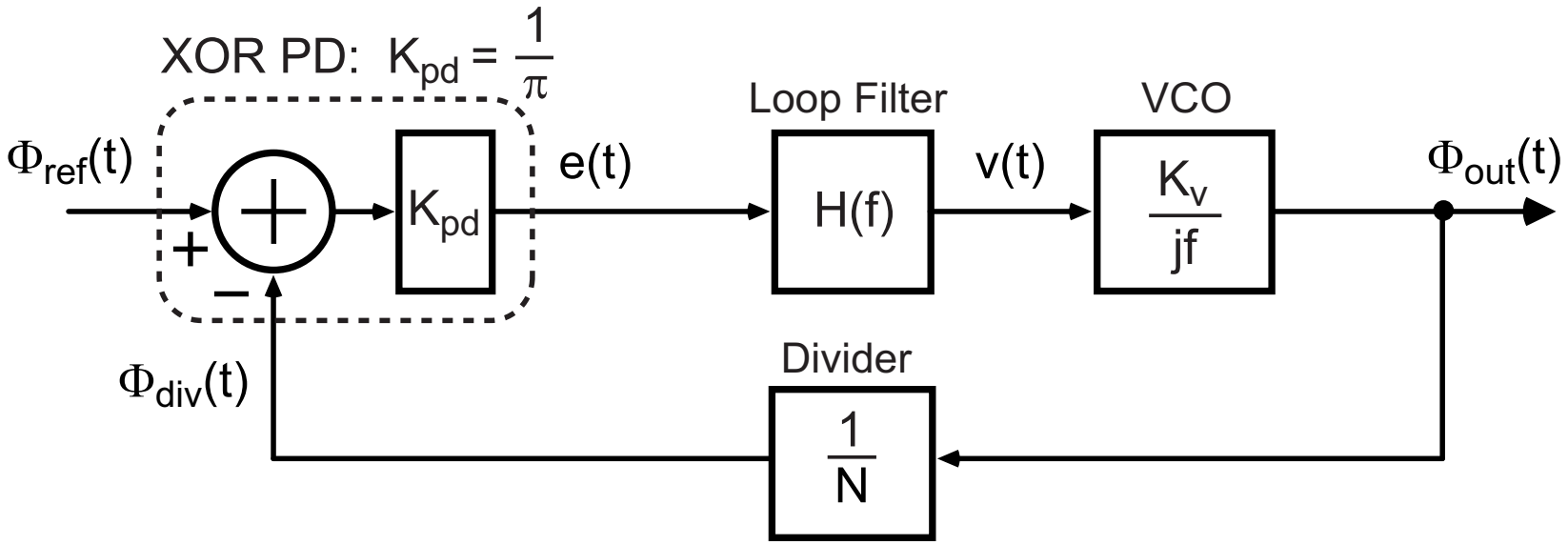
$$A(f) = K_{pd} H(f) \left(\frac{K_v}{jf}\right) \frac{1}{N}$$

  - **Where K_{pd} is defined as PD gain ($1/\pi$ for XOR PD)**

- **Define G(f) as a parameterizing *closed loop* function**

$$G(f) = \frac{A(f)}{1 + A(f)}$$

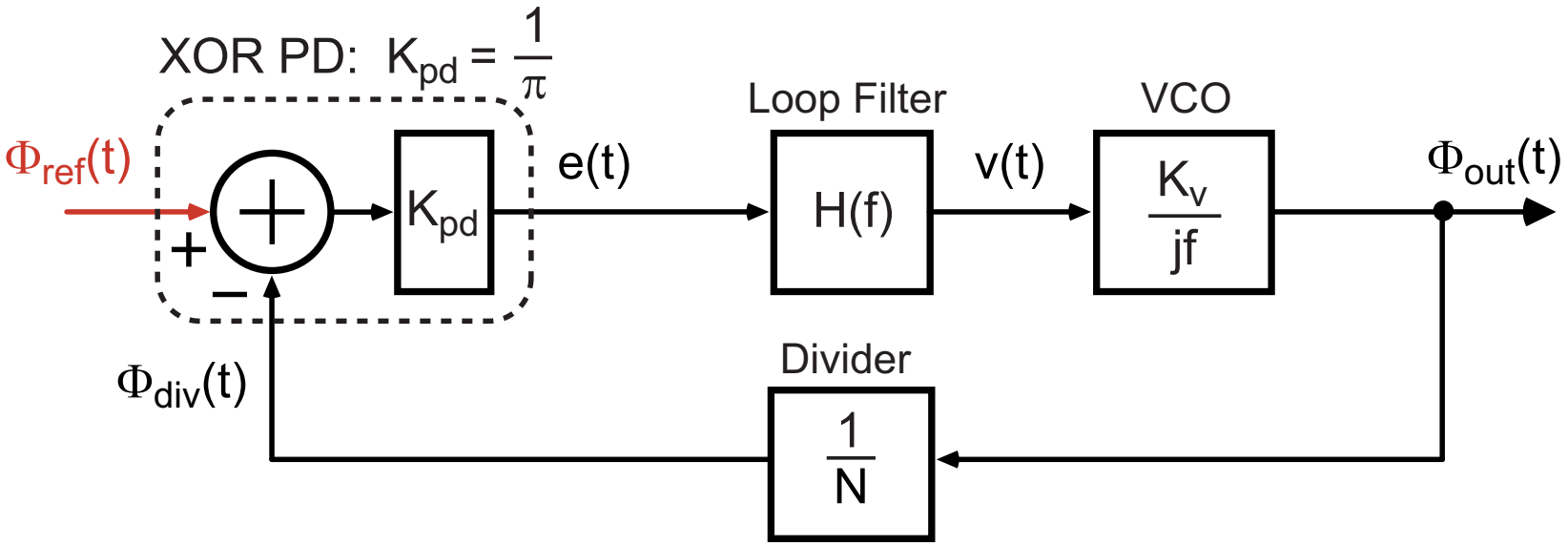
Key Properties of G(f) Function



$$A(f) = K_{pd} H(f) \left(\frac{K_v}{jf}\right) \frac{1}{N} \quad \Rightarrow \quad G(f) = \frac{A(f)}{1 + A(f)}$$

- G(f) always has a DC gain of 1
  - True since *A(f)* goes to infinity as *f* goes to 0
- G(f) is lowpass in nature
  - True since *A(f)* goes to 0 as *f* goes to infinity
- G(f) has bandwidth close to unity gain frequency of *A(f)*

Closed Loop Response From Ref to PLL Output



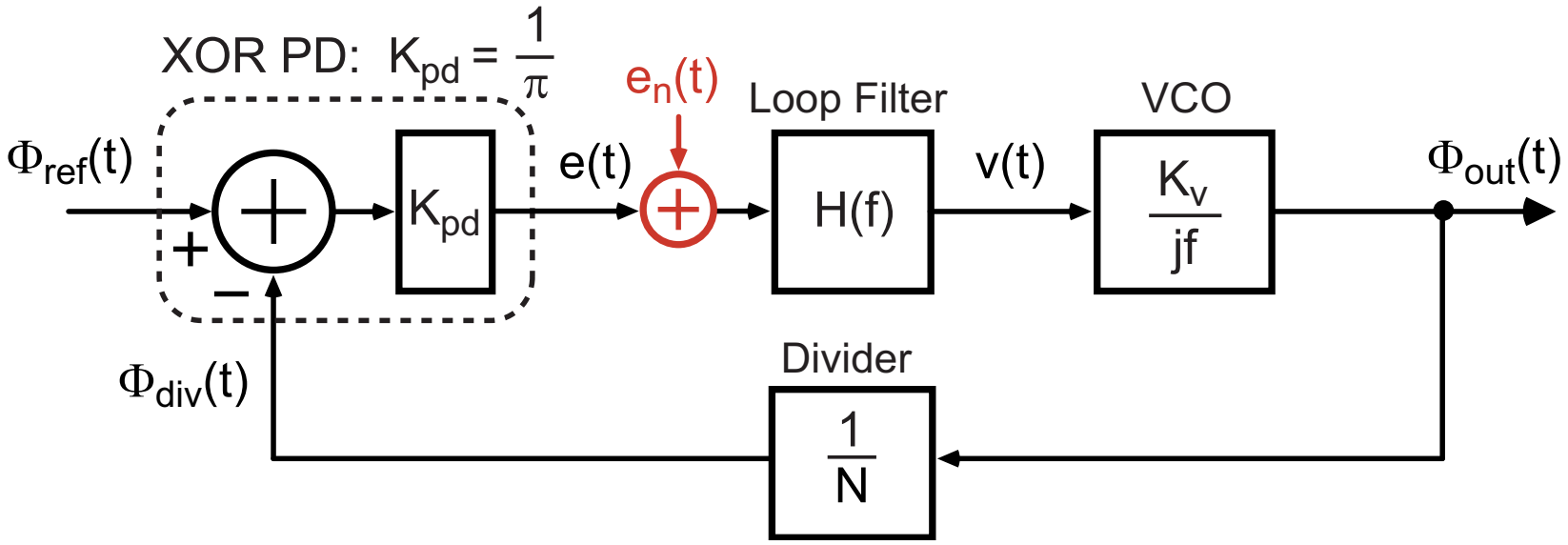
$$\frac{\Phi_{out}}{\Phi_{ref}} = \frac{K_{pd}H(f)K_v/(jf)}{1+(1/N)K_{pd}H(f)K_v/(jf)}$$

$$= N\frac{(1/N)K_{pd}H(f)K_v/(jf)}{1+(1/N)K_{pd}H(f)K_v/(jf)}$$

$$= N\frac{A(f)}{1+A(f)} = \boxed{NG(f)}$$

Lowpass with DC gain of *N*

Closed Loop Response From PD to PLL Output



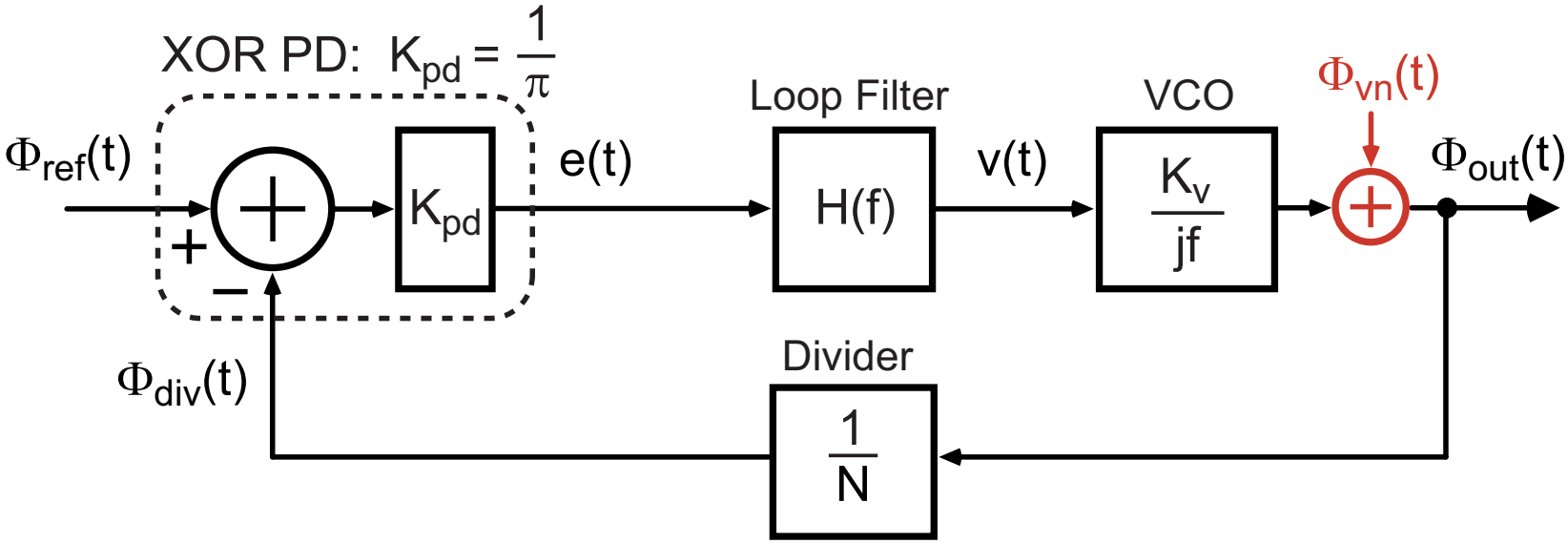
$$\frac{\Phi_{out}}{e_n} = \frac{H(f)K_v/(jf)}{1+(K_{pd}/N)H(f)K_v/(jf)}$$

$$= \frac{N}{K_{pd}} \frac{(K_{pd}/N)H(f)K_v/(jf)}{1+(K_{pd}/N)H(f)K_v/(jf)}$$

$$= \frac{N}{K_{pd}} \frac{A(f)}{1+A(f)} = \boxed{\frac{N}{K_{pd}} G(f)}$$

Lowpass with DC gain of N/K_{pd}

Closed Loop Response From VCO to PLL Output

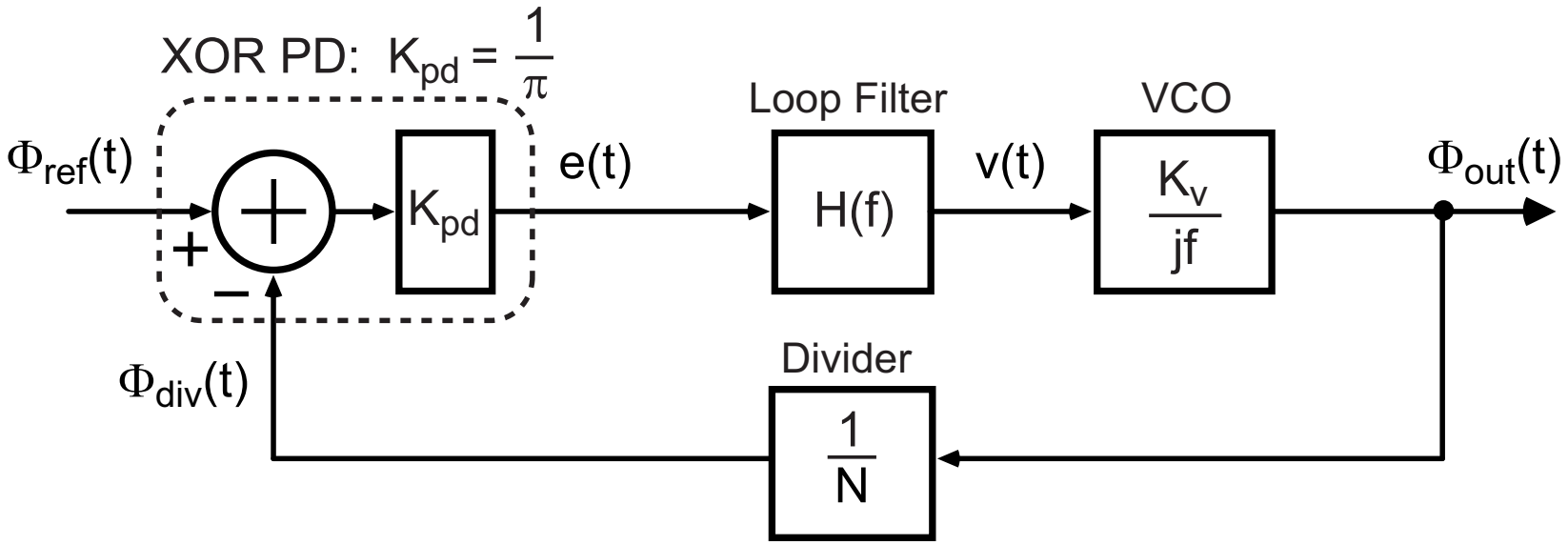


$$\frac{\Phi_{out}}{\Phi_{vn}} = \frac{1}{1 + (K_{pd}/N)H(f)K_v/(jf)}$$

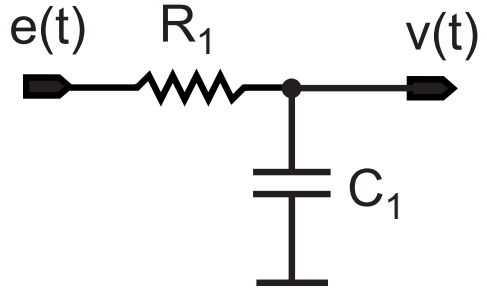
$$= \frac{1}{1 + A(f)} = 1 - \frac{A(f)}{1 + A(f)} = \boxed{1 - G(f)}$$

Highpass with high frequency gain of 1

Consider A First Order Loop Filter

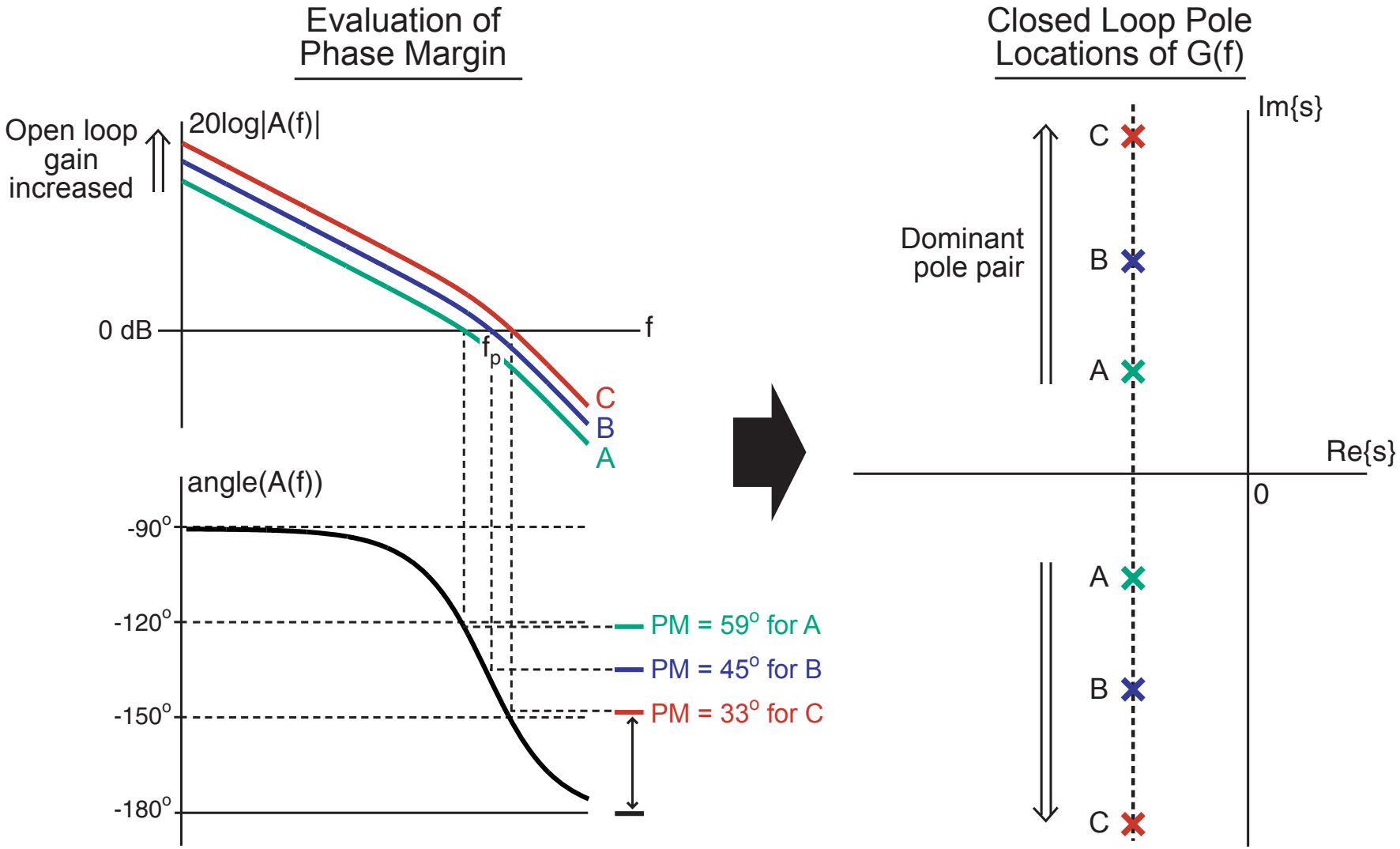


- **First order loop filter**



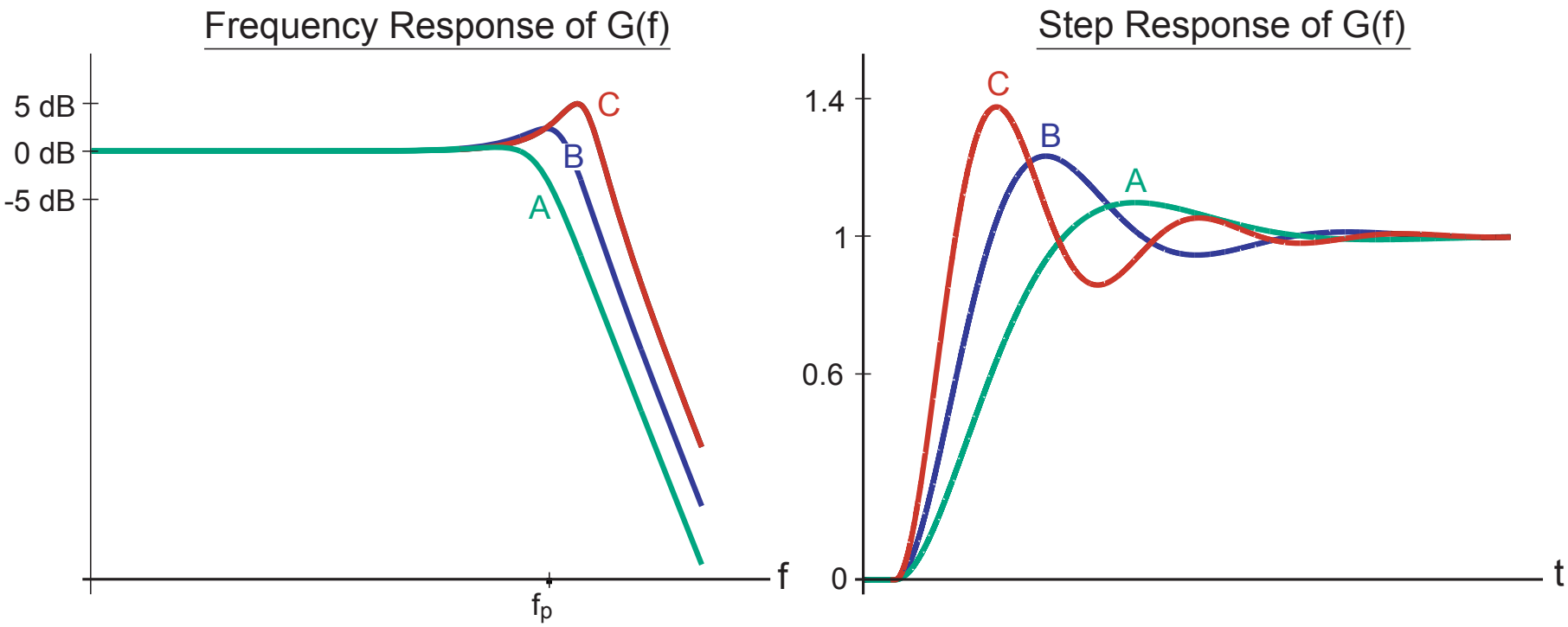
$$\Rightarrow H(f) = \frac{1}{1 + jf/f_p}$$

Closed Loop Poles Versus Open Loop Gain



- **Higher open loop gain leads to an increase in bandwidth but decrease in phase margin**
  - **Closed loop poles start exhibiting higher Q**

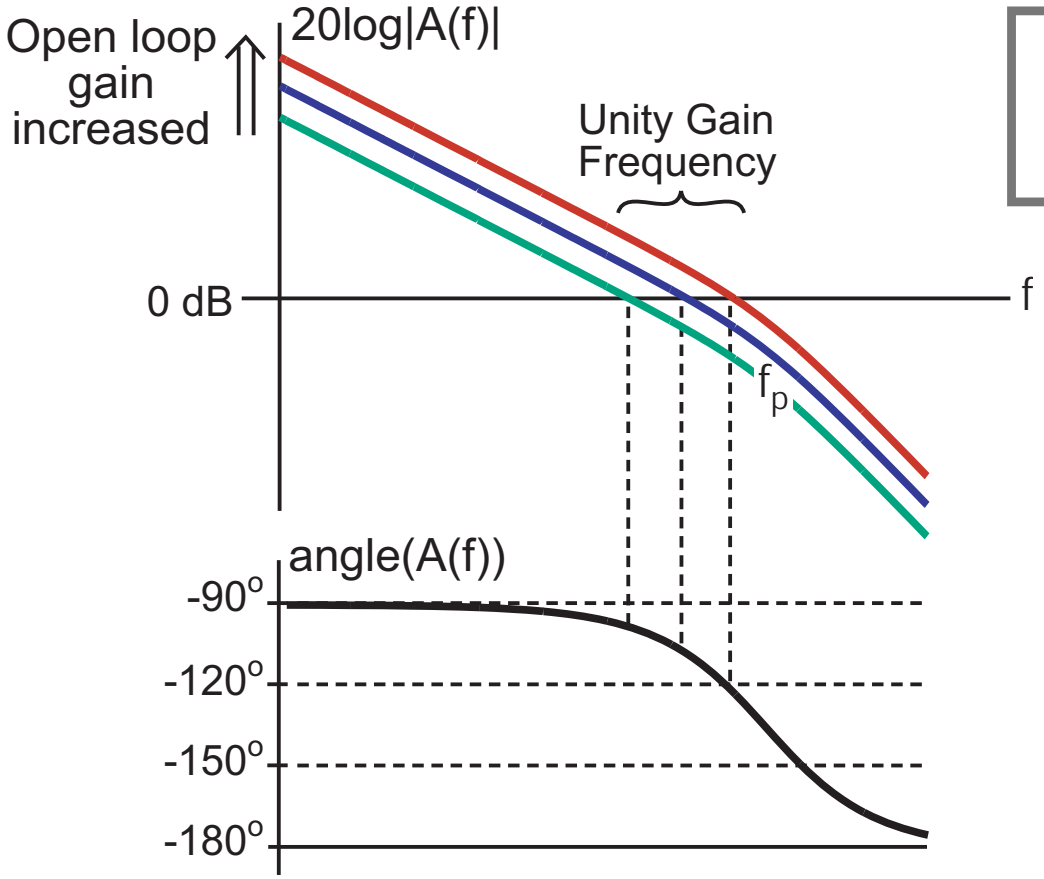
Corresponding Closed Loop Response



- **Decrease in phase margin leads to**
  - **Peaking in closed loop frequency response**
  - **Ringing in closed loop step response**

Design of PLL dynamics is similar to opamps and other classical feedback systems

The Problem with a First Order Loop Filter



$$A(f) = K_{pd} H(f) \left(\frac{K_v}{jf}\right) \frac{1}{N}$$

$$G(f) = \frac{A(f)}{1 + A(f)}$$

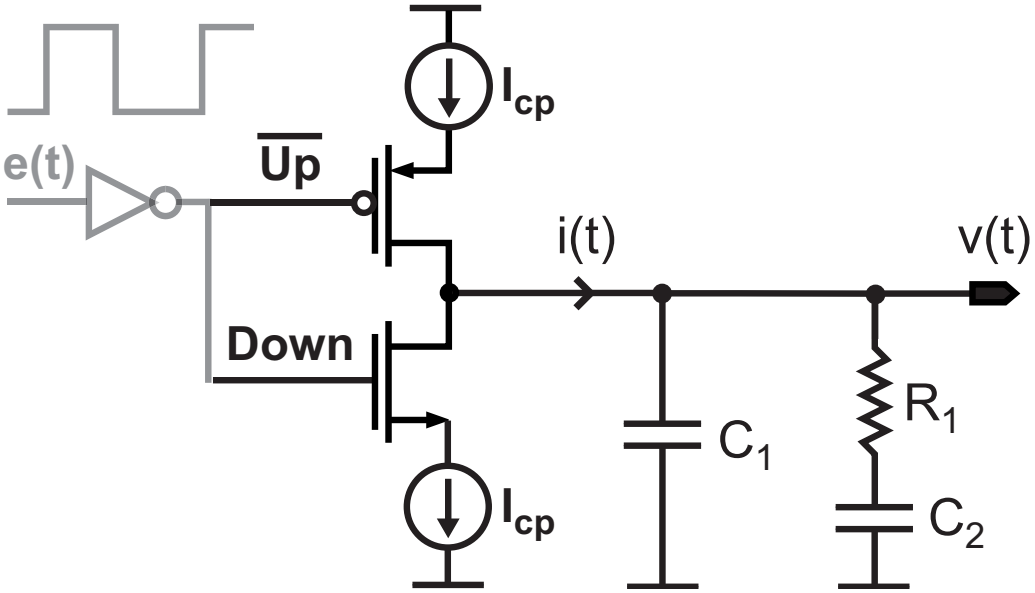
- Recall that bandwidth of G(f) is roughly the same as unity gain frequency of A(f)

- To achieve good phase margin, f_p >> unity gain frequency
  - Implies that H(f) ≈ 1 at unity gain frequency
  - Bandwidth of *G(f)* purely set by K_{pd}, K_v, and *N*

Limited freedom to choose desired closed loop bandwidth

Inclusion of a Charge Pump

- **Charge pump current adds a new parameter that allows more freedom in choosing the PLL bandwidth**
- **Lead/lag filter is a common loop filter with charge pump**
  - **Current into a capacitor forms integrator**
  - **Add extra pole/zero using resistor and additional capacitor**



Forms a Type II PLL

$$H(f) = \left(\frac{I_{cp}}{sC_{sum}}\right)\frac{1 + jf/f_z}{1 + jf/f_p}$$

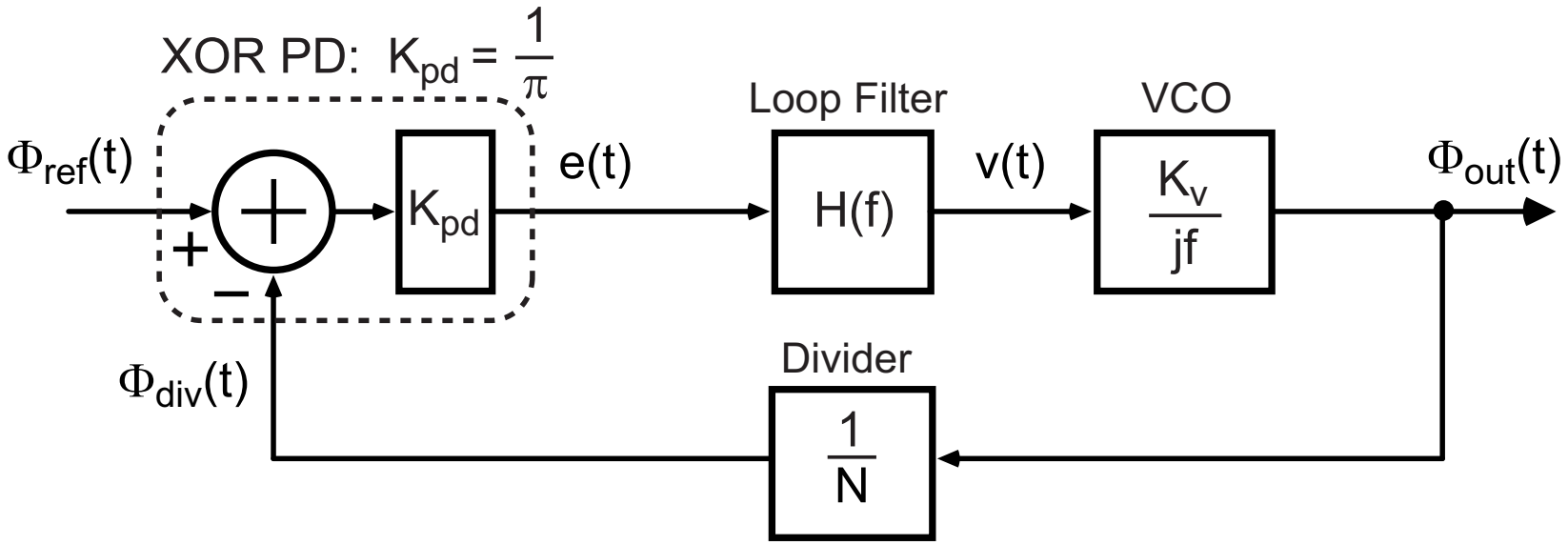
- **Where:**

$$C_{sum} = C_1 + C_2$$

$$f_z = \frac{1}{2\pi R_1 C_2}$$

$$f_p = \frac{C_1 + C_2}{2\pi R_1 C_1 C_2}$$

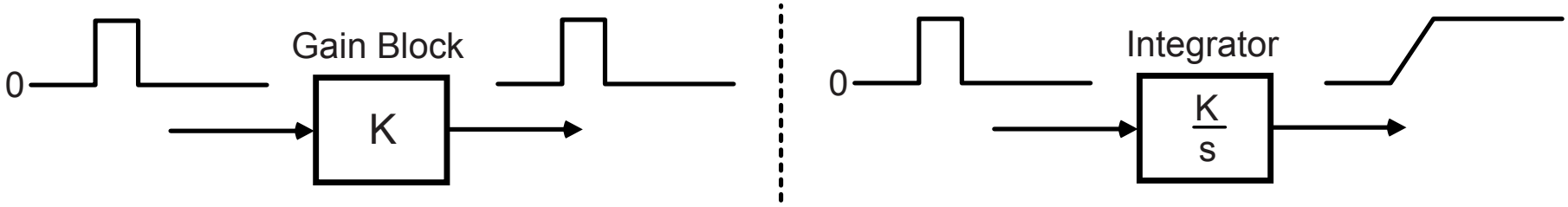
Type I versus Type II PLL Implementations



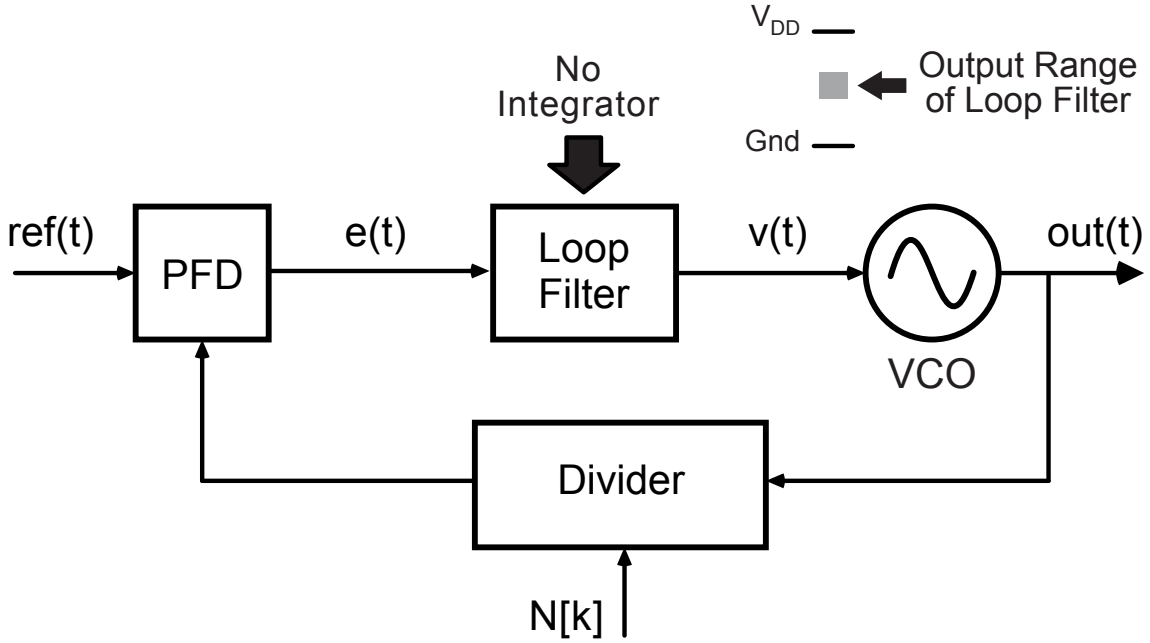
- **Type I: one integrator in PLL open loop transfer function *A(f)***
  - **VCO adds one integrator**
  - **Loop filter, *H(f)*, has no integrators**
- **Type II: two integrators in PLL open loop transfer function *A(f)***
  - **Loop filter, *H(f)*, has one integrator**

VCO Input Range Issue for Type I PLL Implementations

- DC output range of gain block versus integrator

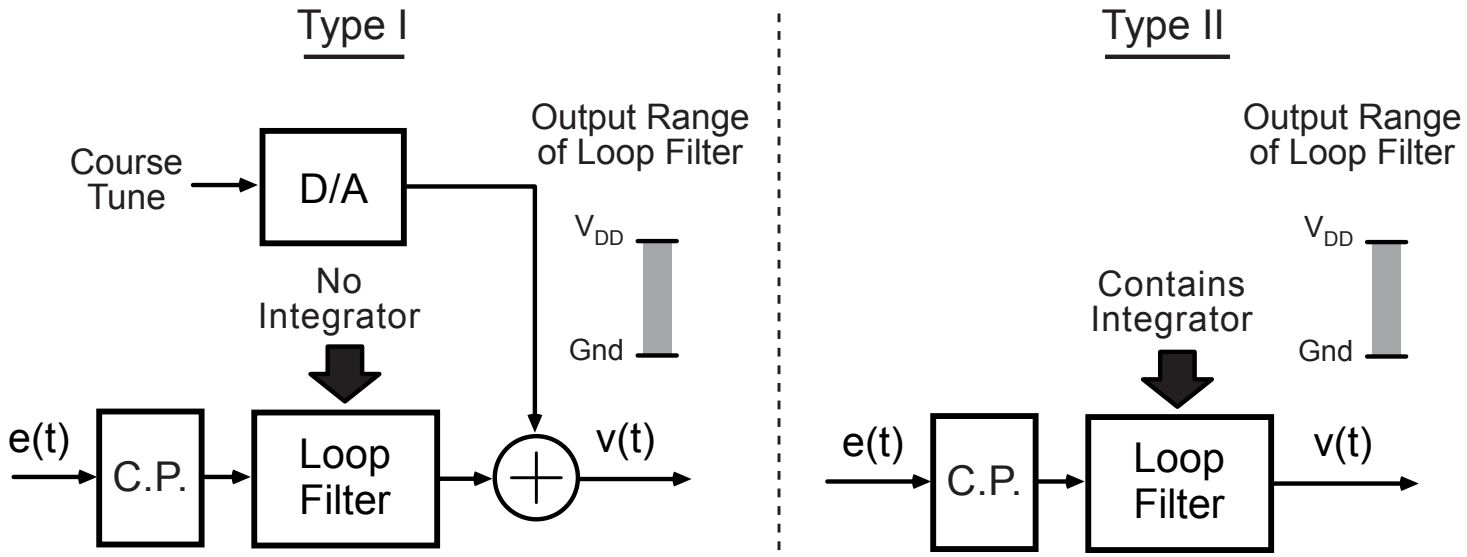


- Issue: often need to provide attenuation through loop filter to achieve a desired closed loop bandwidth
  - Loop filter output fails to cover full input range of VCO

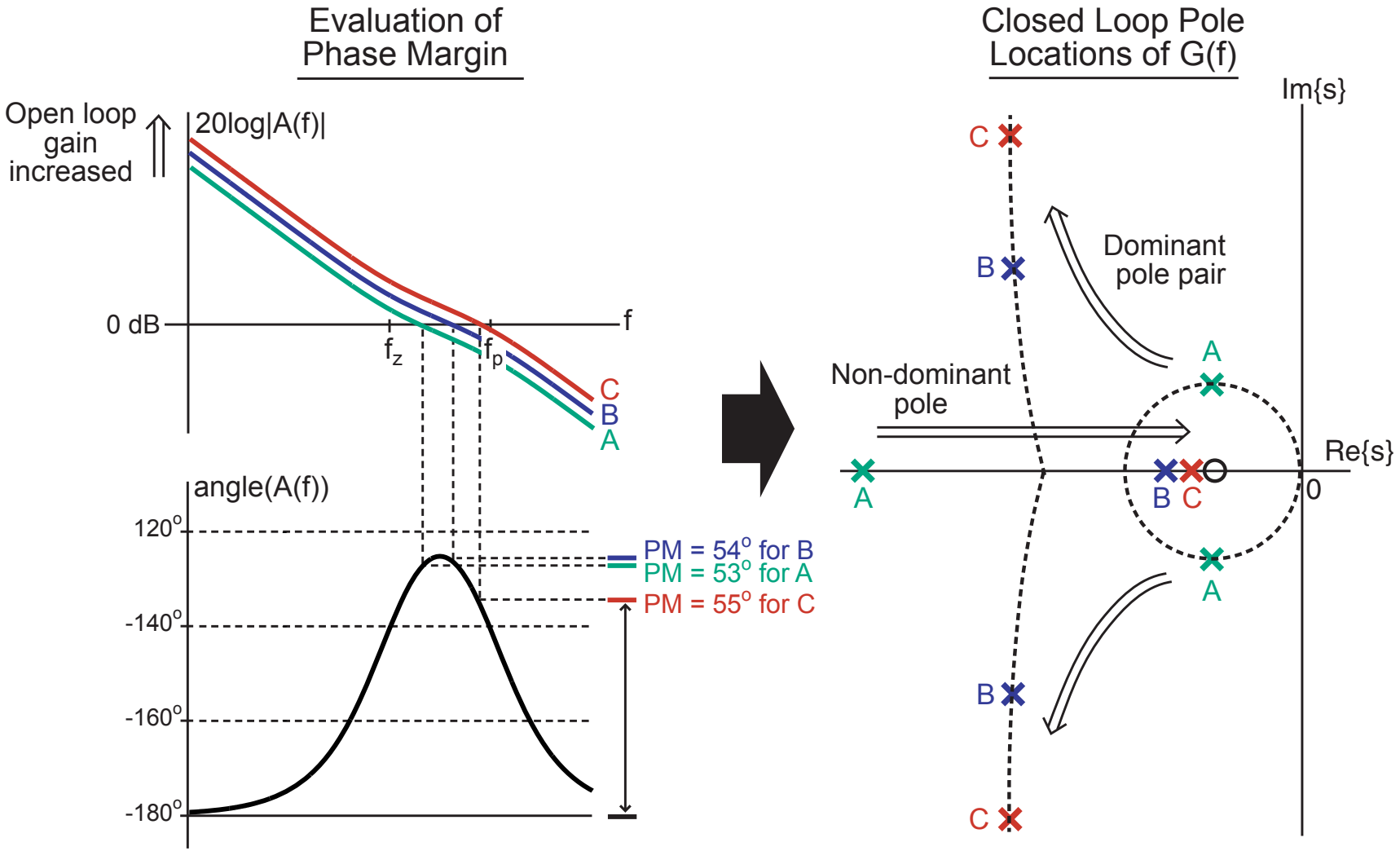


Options for Achieving Full Range Span of VCO

- **Type I**
  - **Add a D/A converter to provide coarse tuning**
    - Adds power and complexity
    - Steady-state phase error inconsistently set
- **Type II**
  - **Integrator automatically provides DC level shifting**
    - Low power and simple implementation
    - Steady-state phase error always set to zero

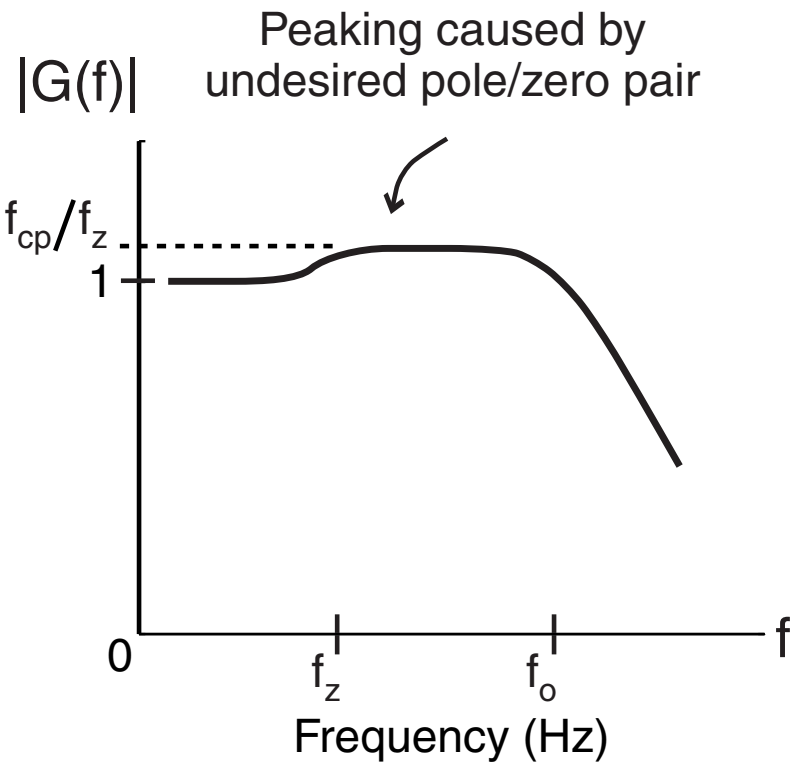


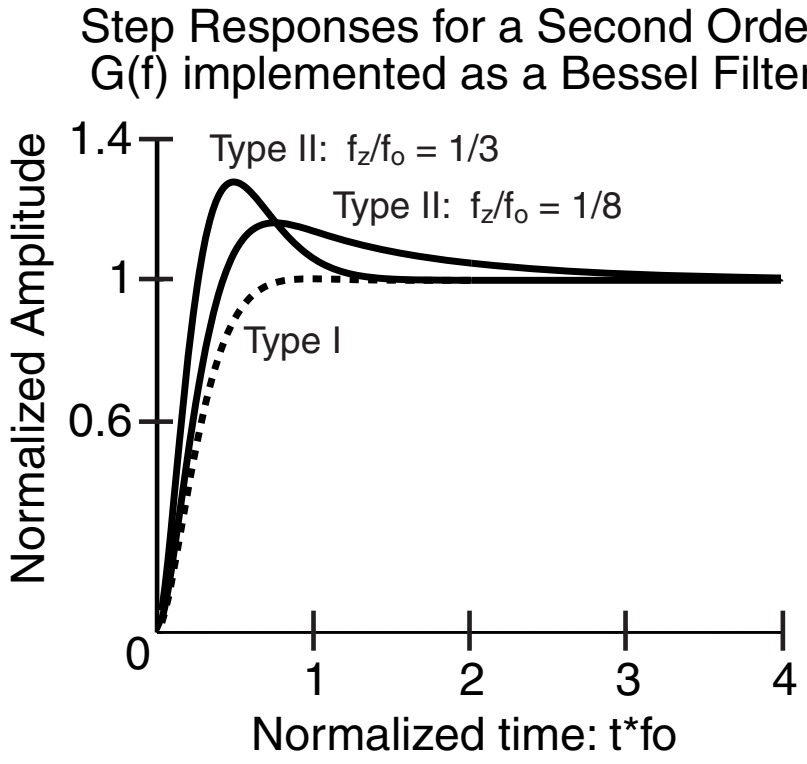
Design of Type II, Charge Pump PLL



- Place f_z and f_p based on phase margin, and open loop gain based on desired PLL bandwidth
  - Charge pump offers high flexibility in choosing PLL bandwidth

Negative Issues For Type II PLL Implementations

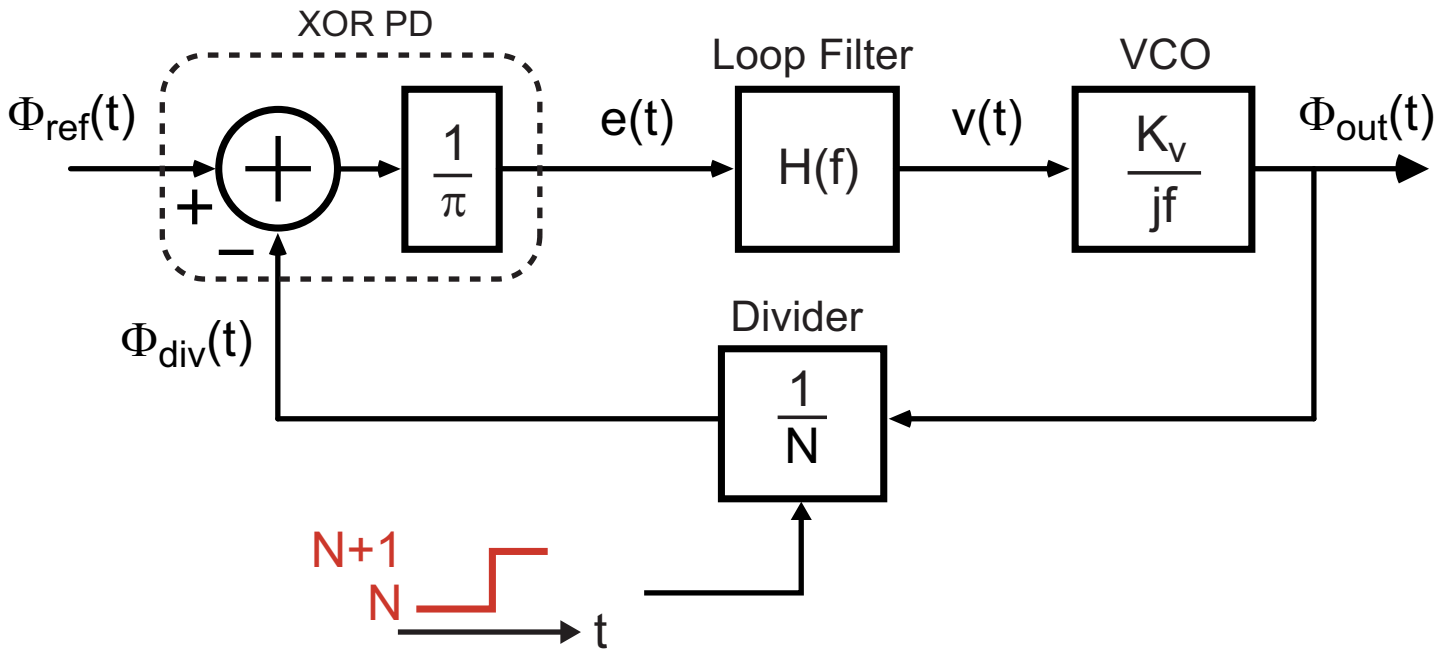




- **Parasitic pole/zero pair causes**
  - **Peaking in the closed loop frequency response**
    - Increases PLL phase noise
  - **Extended settling time due to parasitic "tail" response**
    - Bad for applications demanding fast settling time

The Need for Frequency Detection

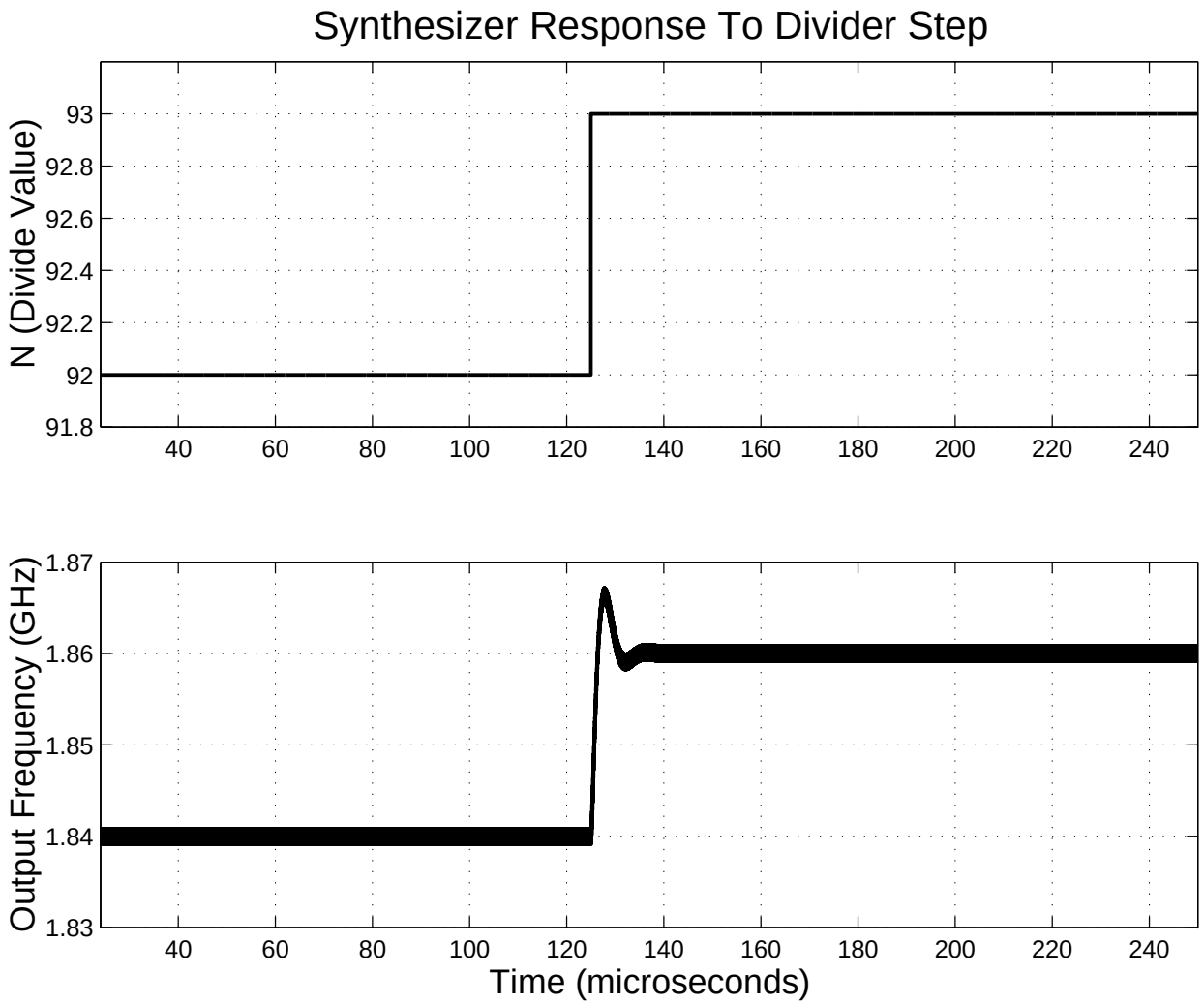
Response of PLL to Divide Value Changes



- **Change output frequency by changing the divide value**
- **Classical approach provides no direct model of impact of divide value variations**
  - **Treat divide value variation as a perturbation to a linear system and use the PLL closed loop response**
- **More advanced PLL models include divide value variations**
  - M.H. Perrott, M.D. Trott, C.G. Sodini, "A modeling approach for Σ-Δ fractional-N frequency synthesizers allowing straightforward noise analysis," JSSC, vol. 37, pp. 1028-1038, Aug. 2002.

Response of an Actual PLL to Divide Value Change

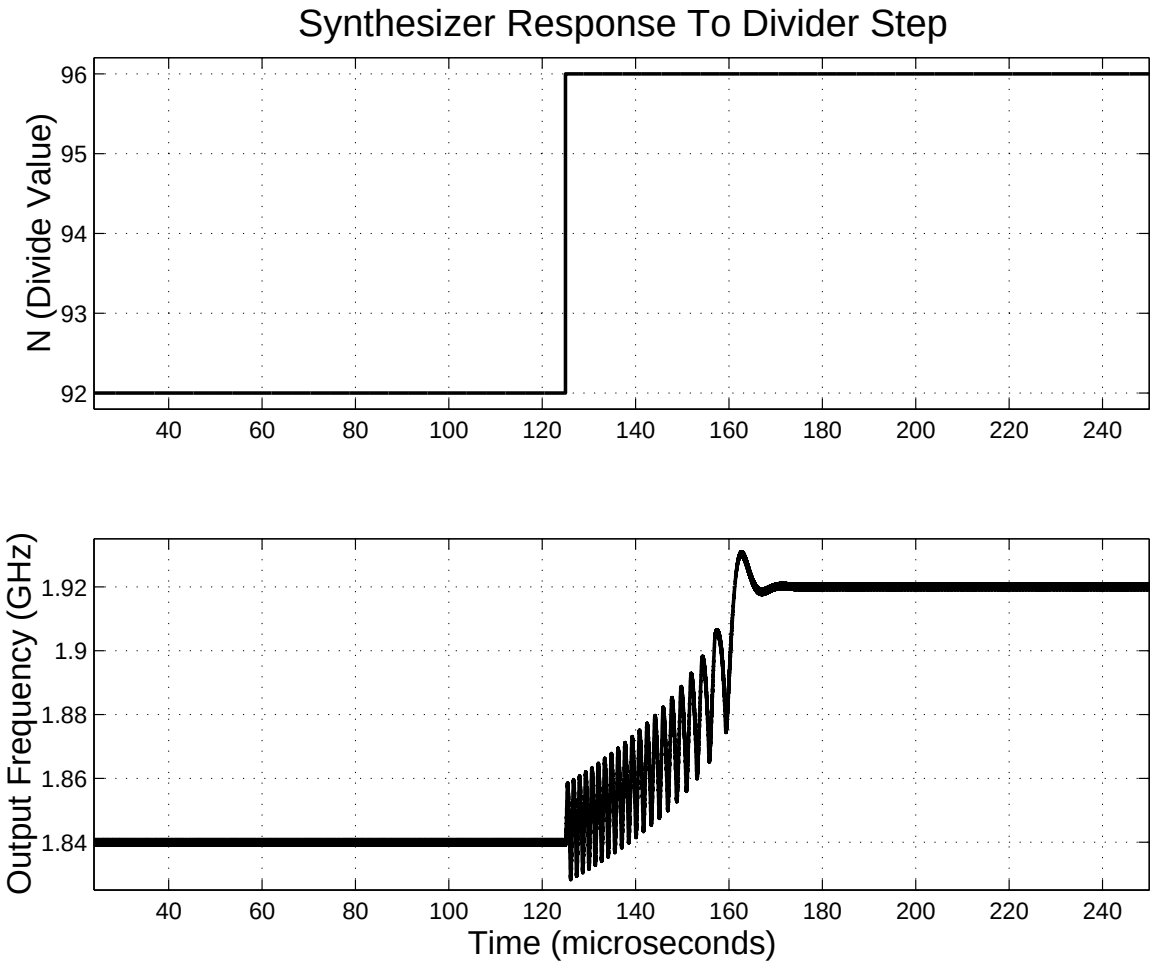
- **Example: Change divide value by one**



- **PLL responds according to linear model of closed loop response!**

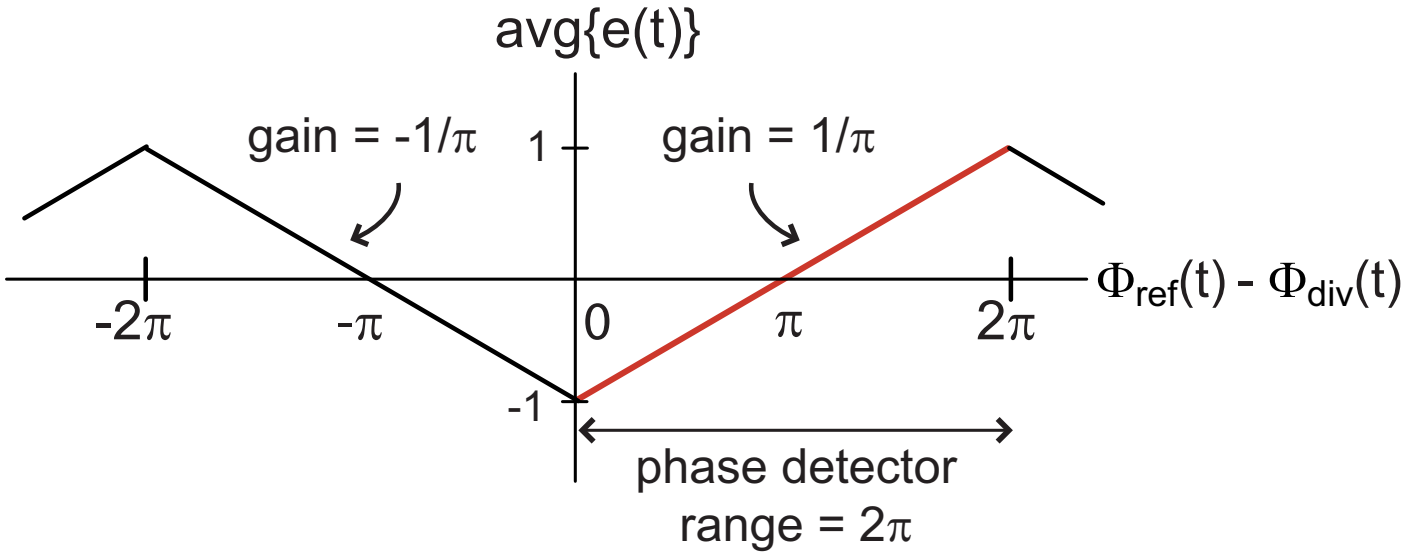
What Happens with Large Divide Value Variations?

- **PLL response does not fit linear model**



  - **What is happening here?**

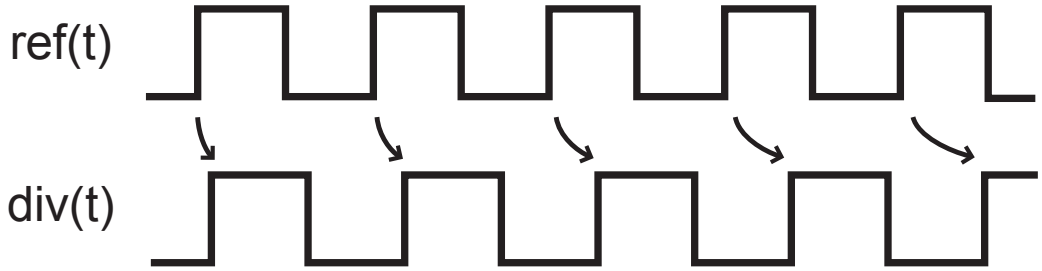
Recall Phase Detector Characteristic



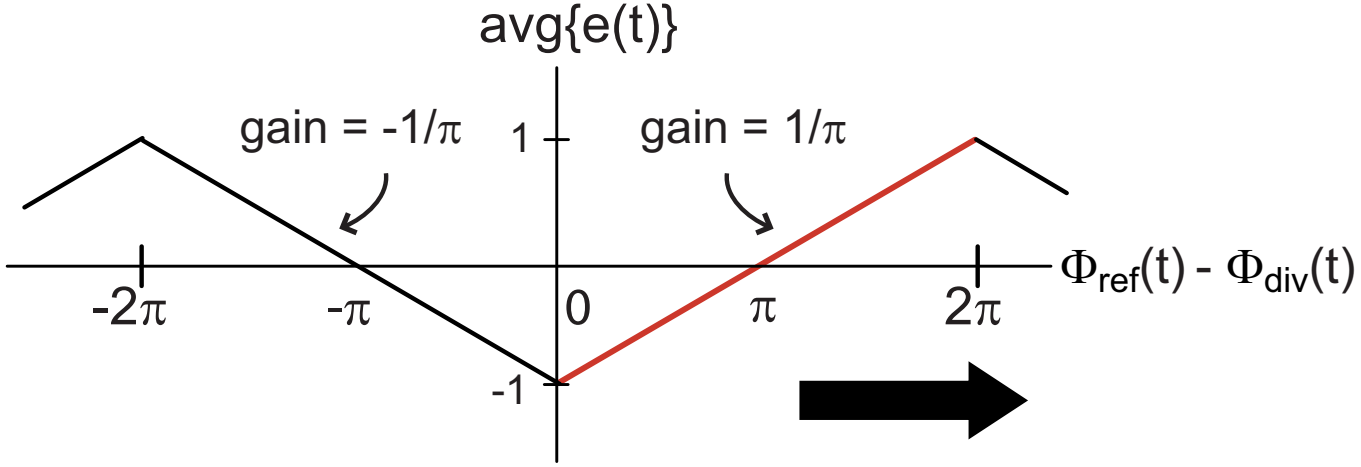
- To simplify modeling, we assumed that we always operated in a confined phase range (0 to 2π)
  - Led to a simple PD model
- Large perturbations knock us out of that confined phase range
  - PD behavior varies depending on the phase range it happens to be in

Cycle Slipping

- **Consider the case where there is a frequency offset between divider output and reference**
  - **We know that phase difference will accumulate**

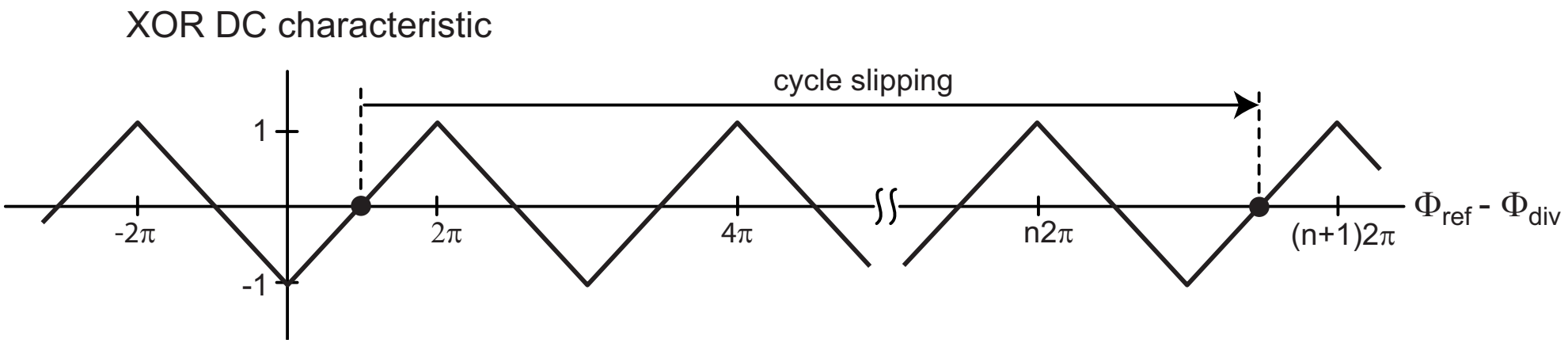


- **Resulting ramp in phase causes PD characteristic to be swept across its different regions (cycle slipping)**



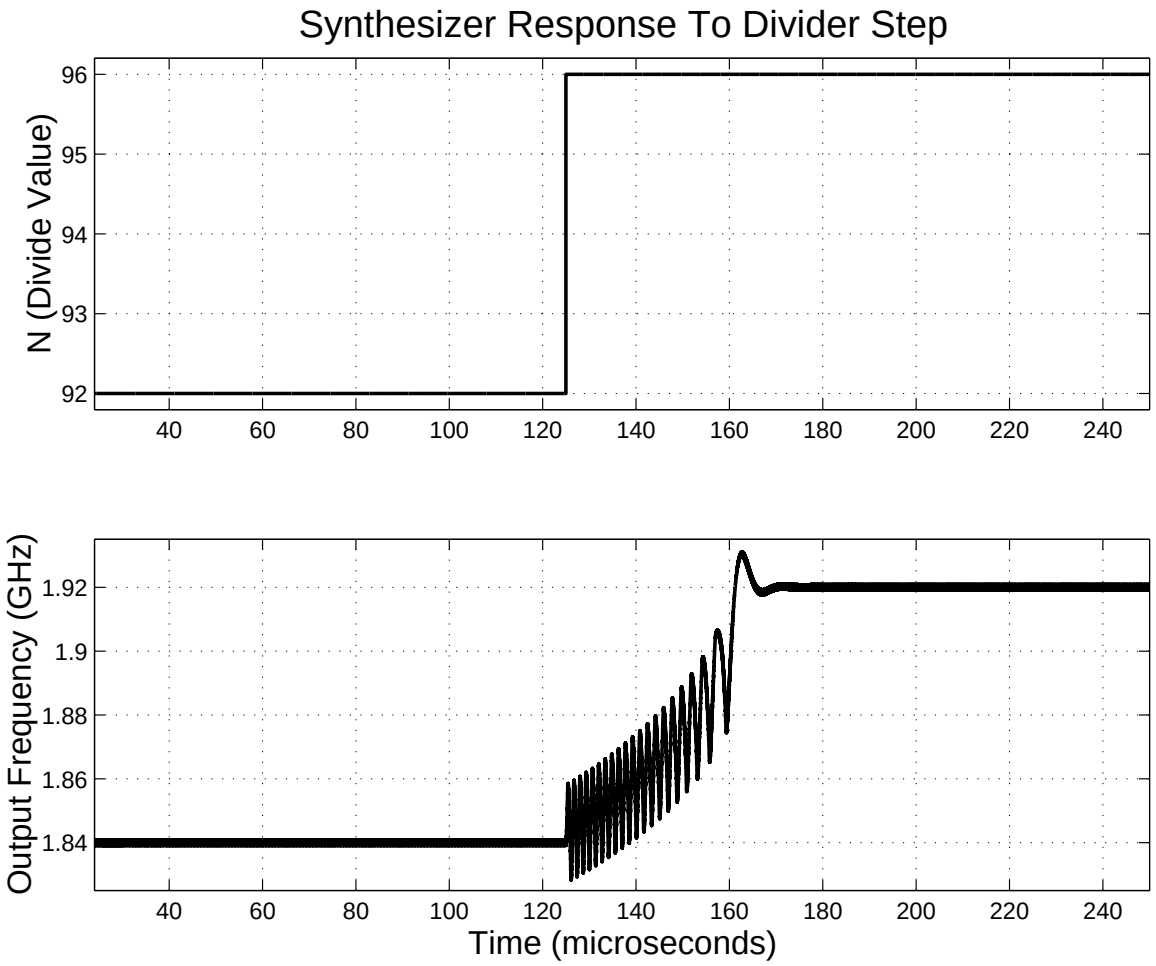
Impact of Cycle Slipping

- **Loop filter averages out phase detector output**
- **Severe cycle slipping causes phase detector to alternate between regions very quickly**
  - **Average value of XOR characteristic can be close to zero**
  - **PLL frequency oscillates according to cycle slipping**
  - **In severe cases, PLL will not re-lock**
    - PLL has finite frequency lock-in range!



Back to PLL Response Shown Previously

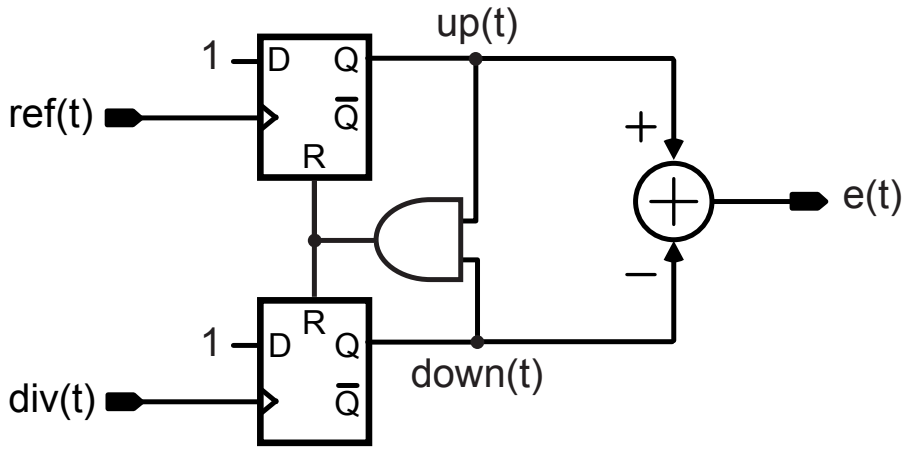
- **PLL output frequency indeed oscillates**
  - **Eventually locks when frequency difference is small enough**

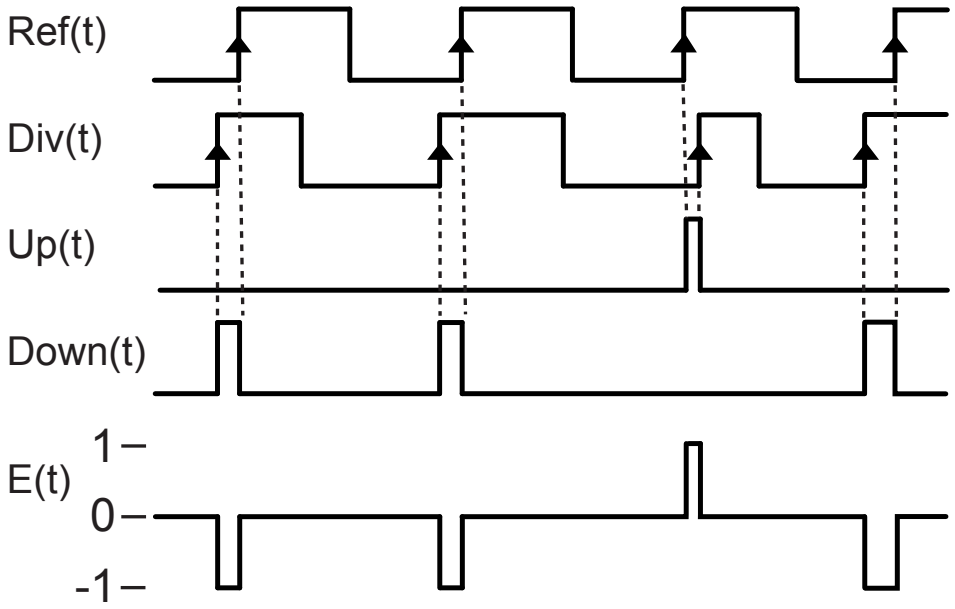


  - **How do we extend the frequency lock-in range?**

Phase Frequency Detectors (PFD)

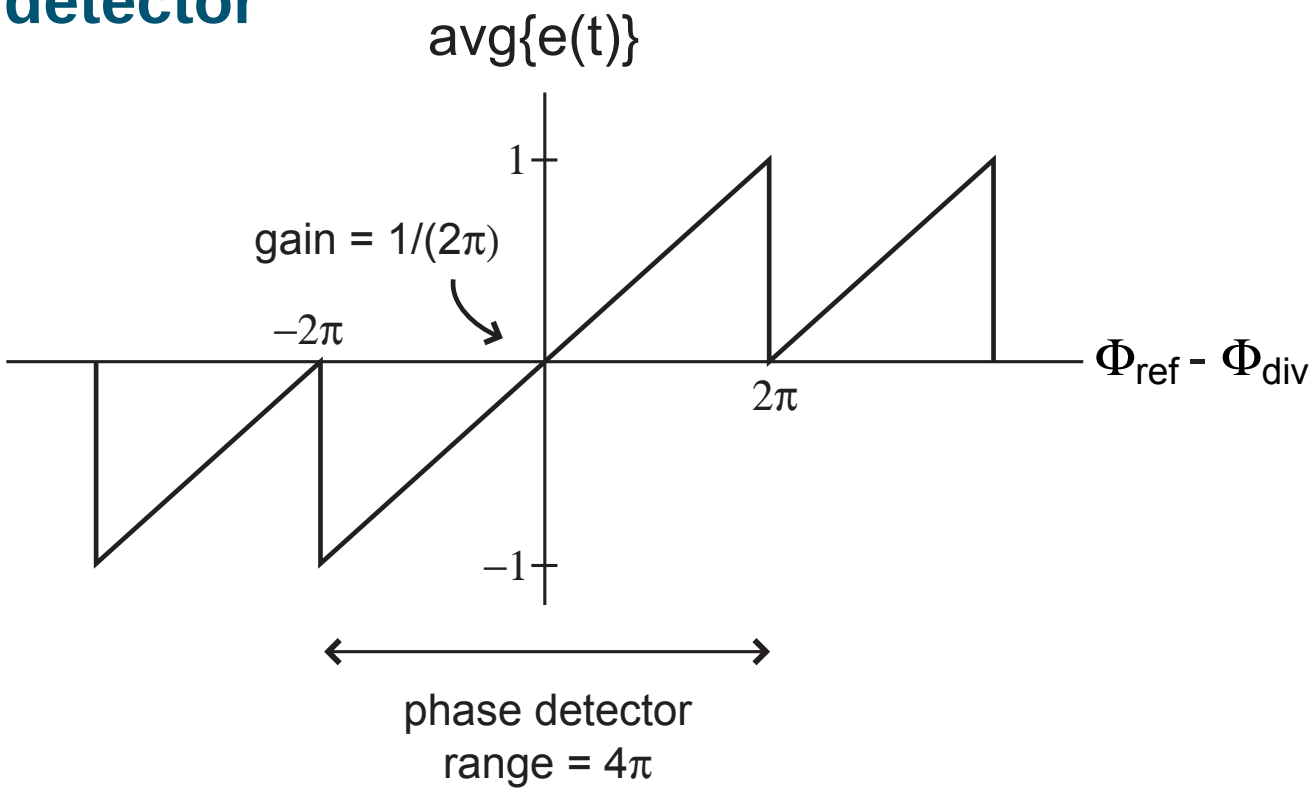
- **Example: Tristate PFD**





Tristate PFD Characteristic

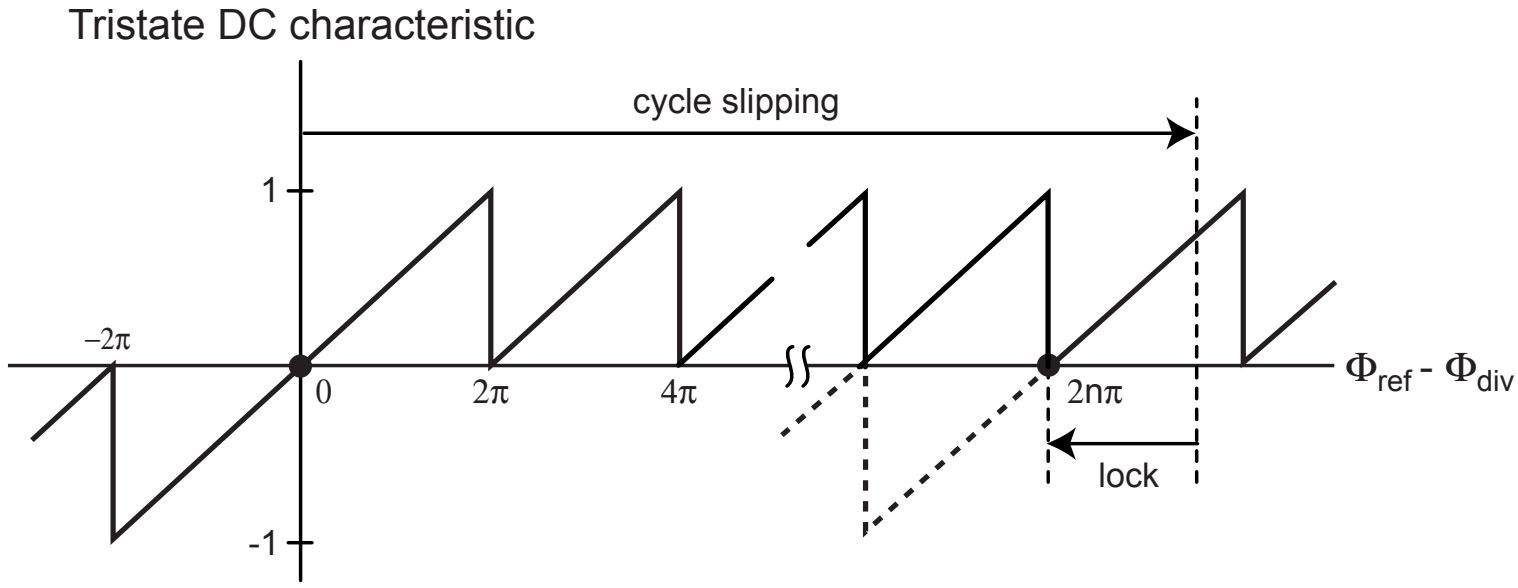
- **Calculate using similar approach as used for XOR phase detector**



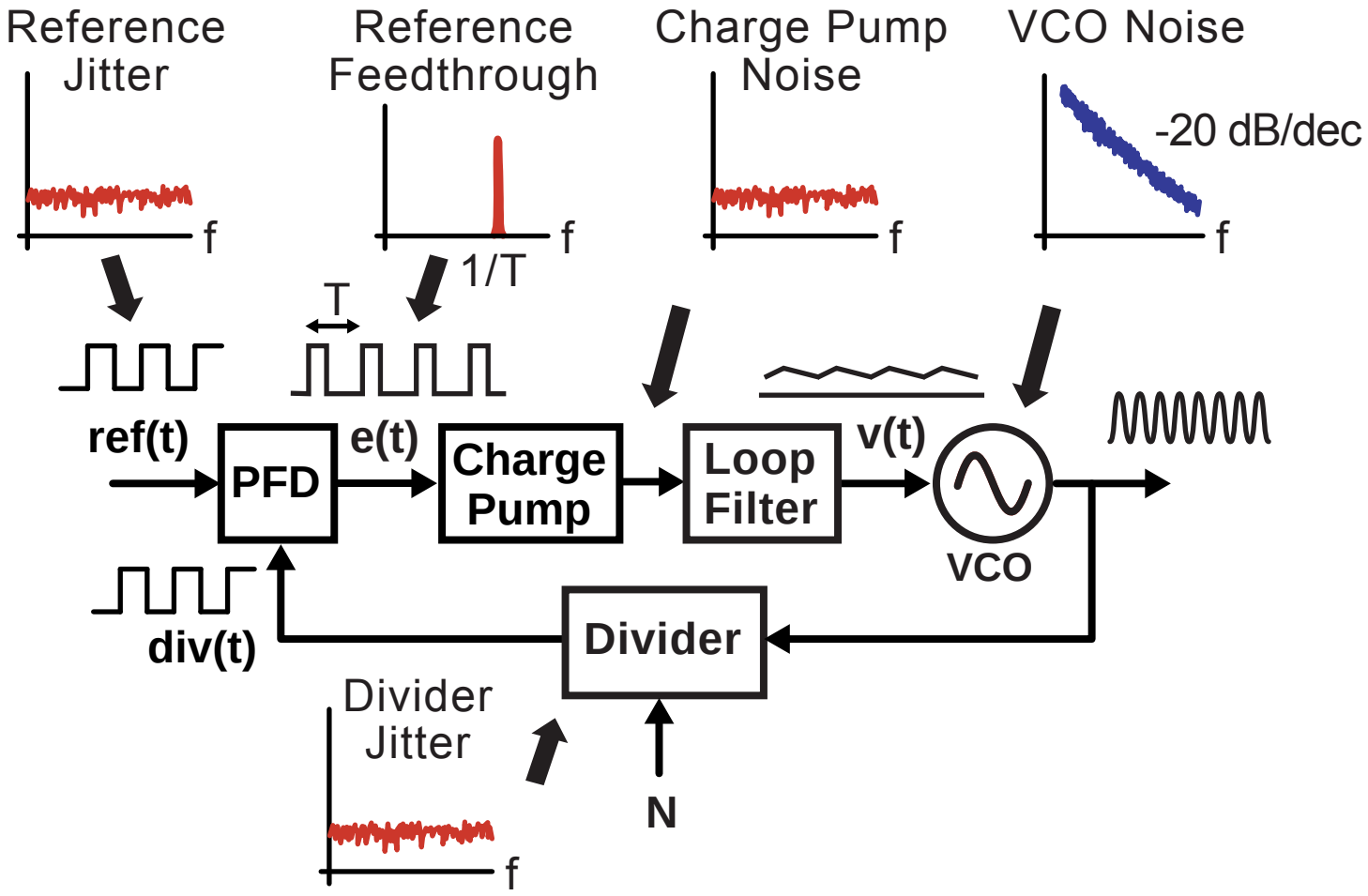
- **Note that phase error characteristic is asymmetric about zero phase**
  - **Key attribute for enabling frequency detection**

PFD Enables PLL to Always Regain Frequency Lock

- Asymmetric phase error characteristic allows positive frequency differences to be distinguished from negative frequency differences
  - Average value is now positive or negative according to sign of frequency offset
  - PLL will always relock for type II PLL

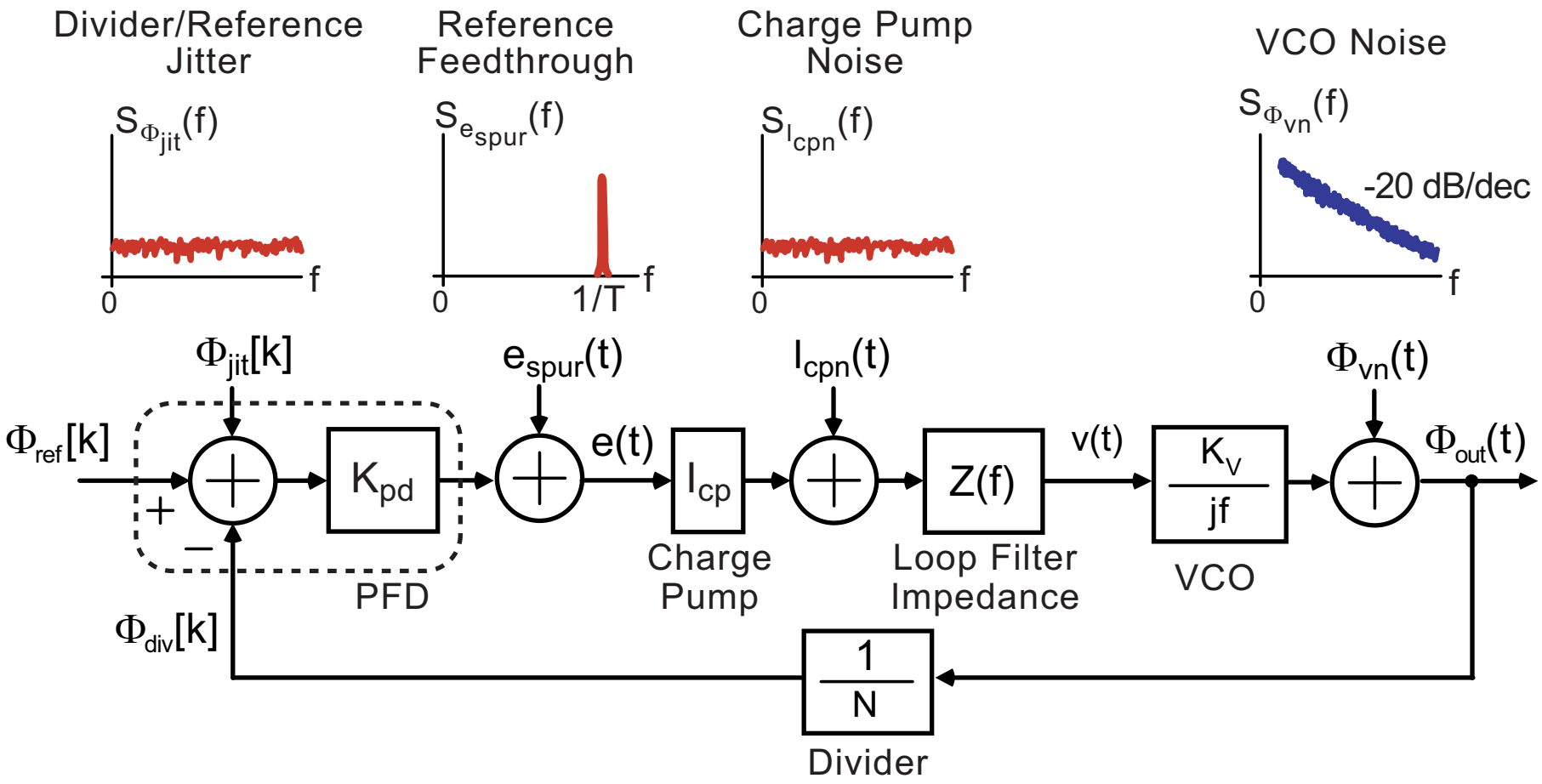


The Issue of Noise



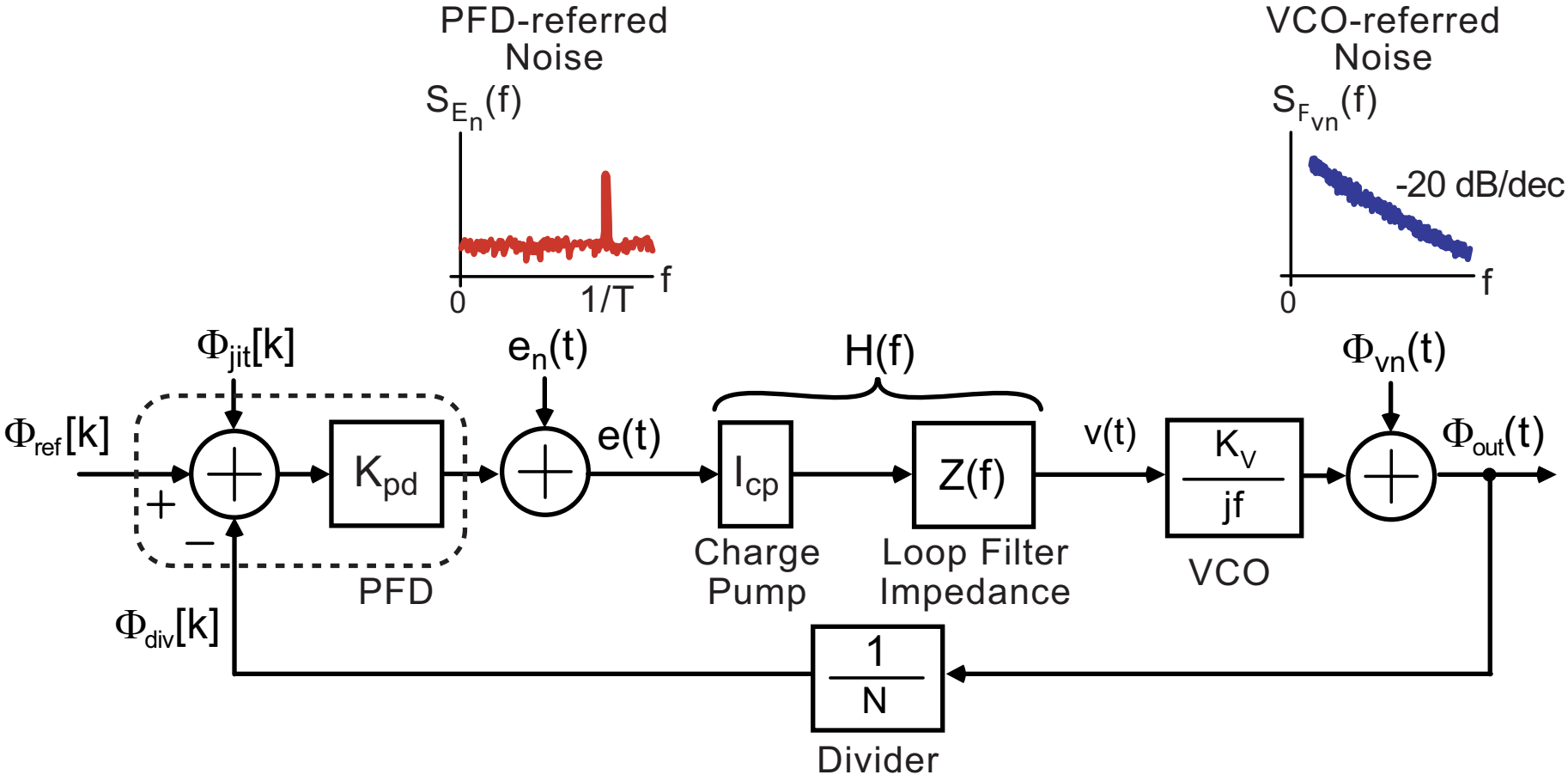
- Each PLL component contributes noise that impacts overall PLL output phase noise
- Achievement of adequately low PLL phase noise is a key issue when designing a PLL

Modeling the Impact of Noise on Output Phase of PLL



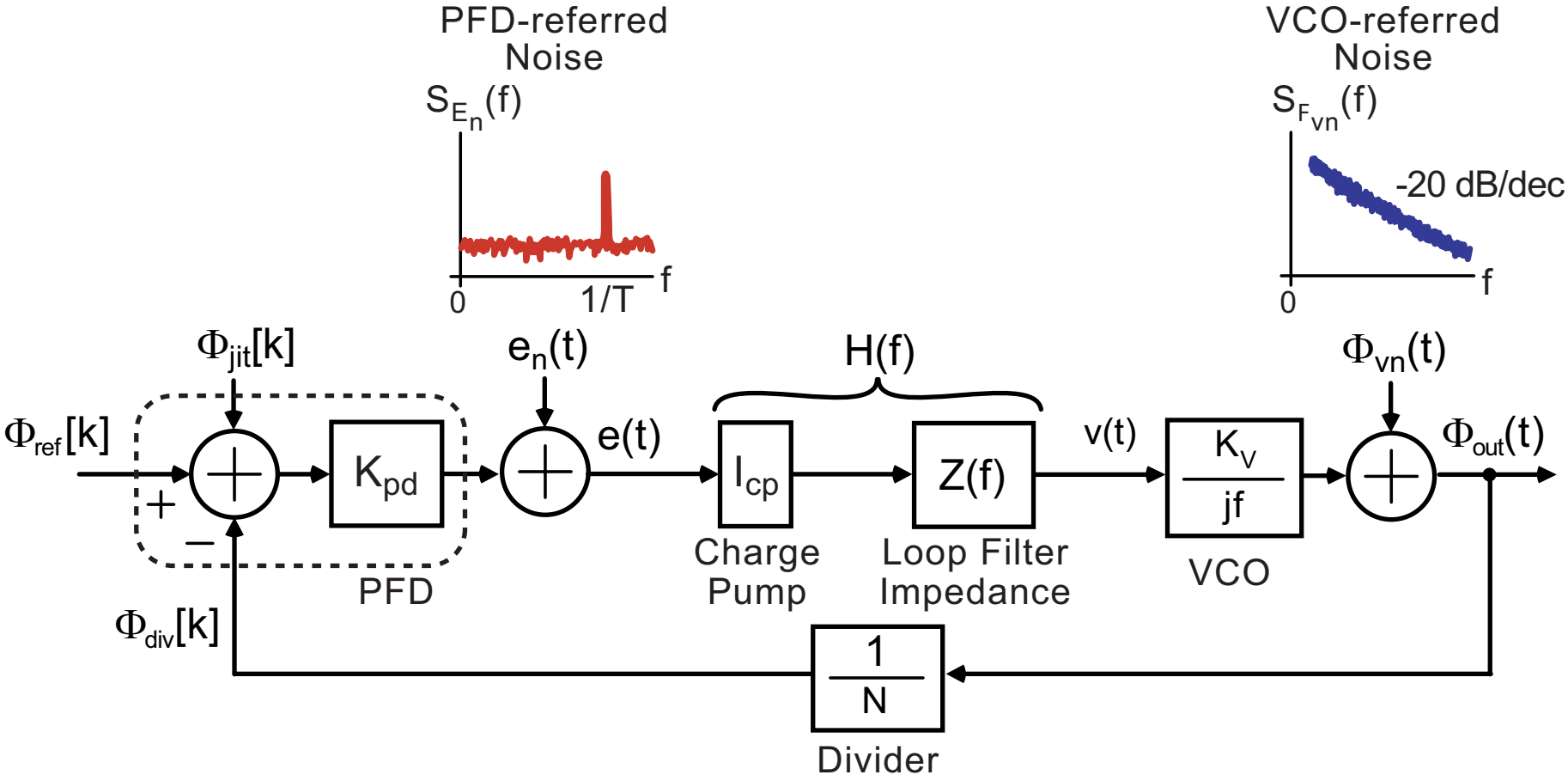
- **Determine impact on output phase by deriving transfer function from each noise source to PLL output phase**
  - **There are a lot of transfer functions to keep track of!**

Simplified Noise Model



- **Refer all non-VCO PLL noise sources to the PFD output**
  - **PFD-referred noise corresponds to the sum of these noise sources referred to the PFD output**
  - **Typically, charge pump noise dominates PFD-referred noise**

Leverage Previous Transfer Function Analysis



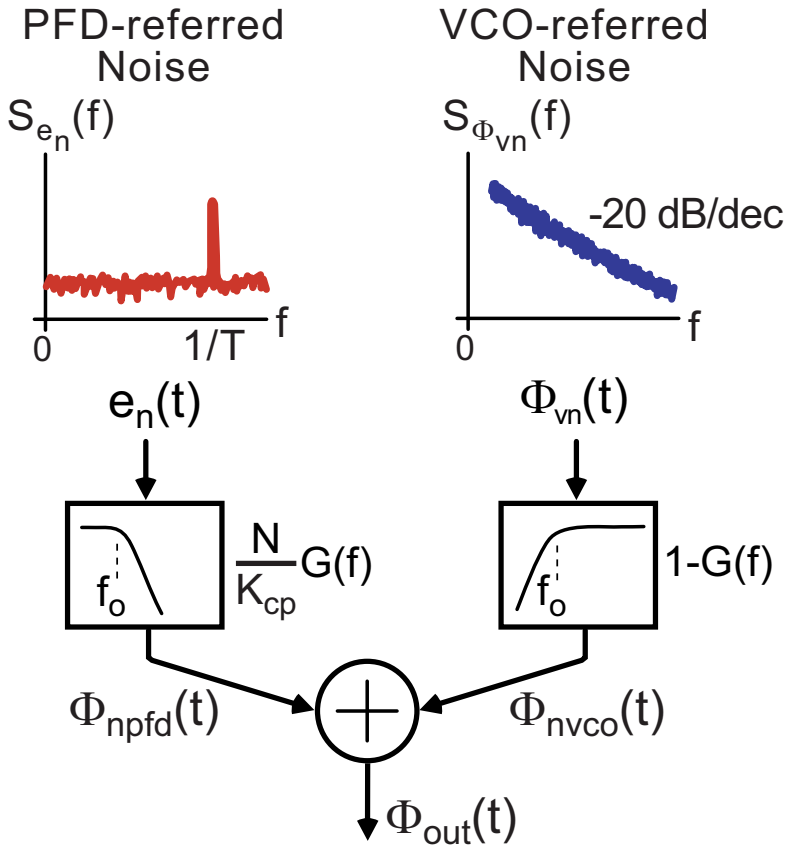
- **PFD-referred noise**
  - **Lowpass with DC gain of N/K_{pd}**

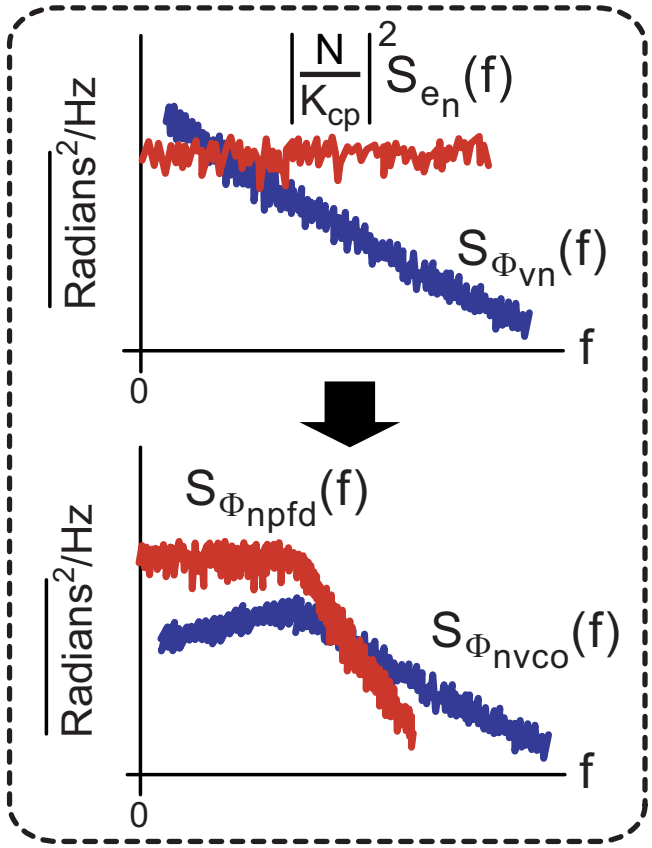
$$\frac{\Phi_{out}}{e_n} = \frac{N}{K_{pd}} G(f)$$

- **VCO-referred noise**
  - **Highpass with gain of 1**

$$\frac{\Phi_{out}}{\Phi_{vn}} = 1 - G(f)$$

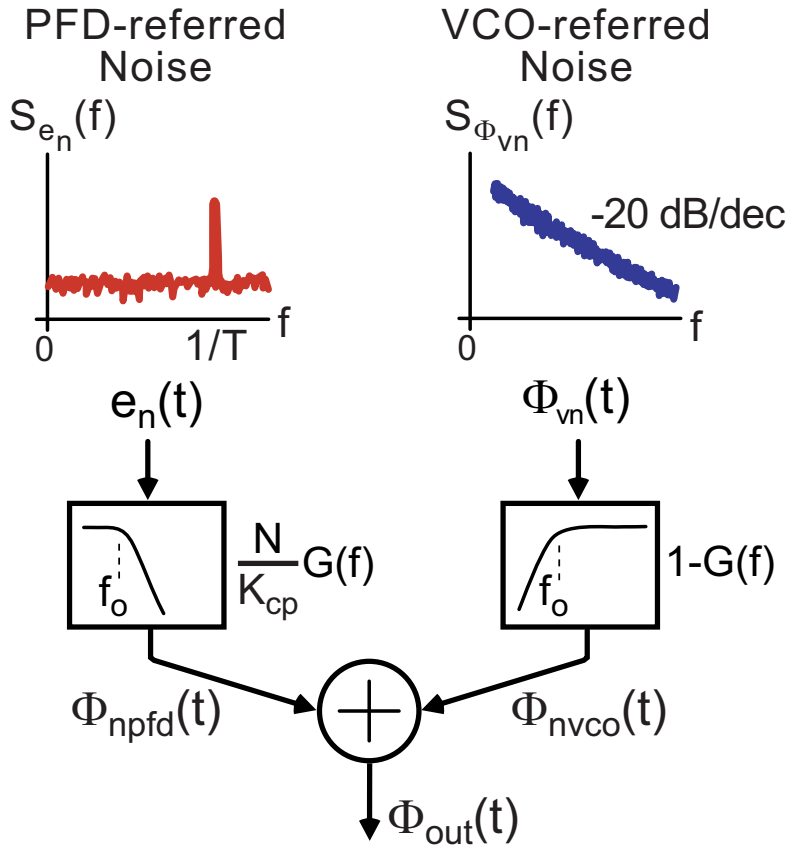
Transfer Function View of PLL Phase Noise

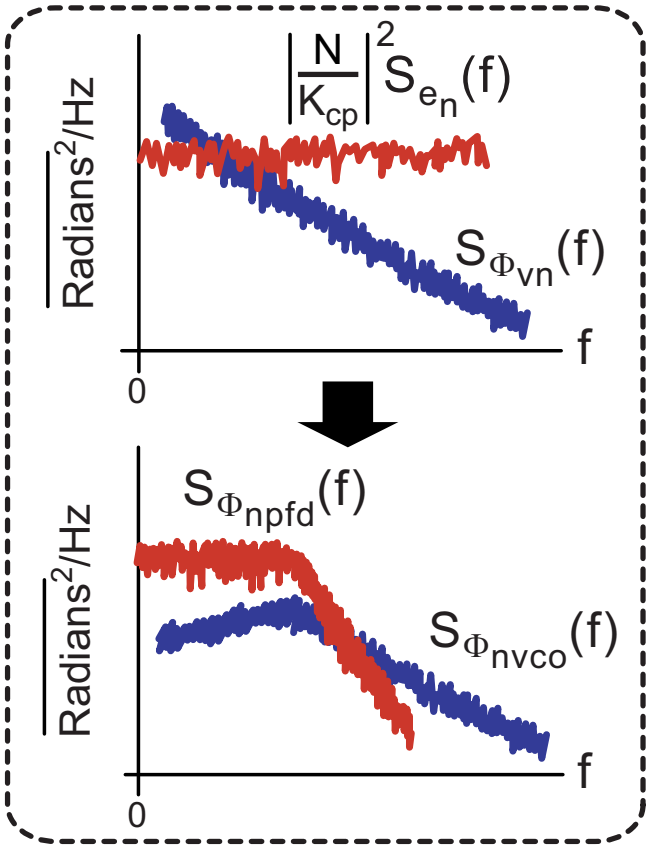




- **PFD-referred noise dominates at low frequencies**
  - **Corresponds to close-in phase noise of synthesizer**
- **VCO-referred noise dominates at high frequencies**
  - **Corresponds to far-away phase noise of synthesizer**

Spectral Density of PLL Phase Noise Components





- **PFD-referred noise:**

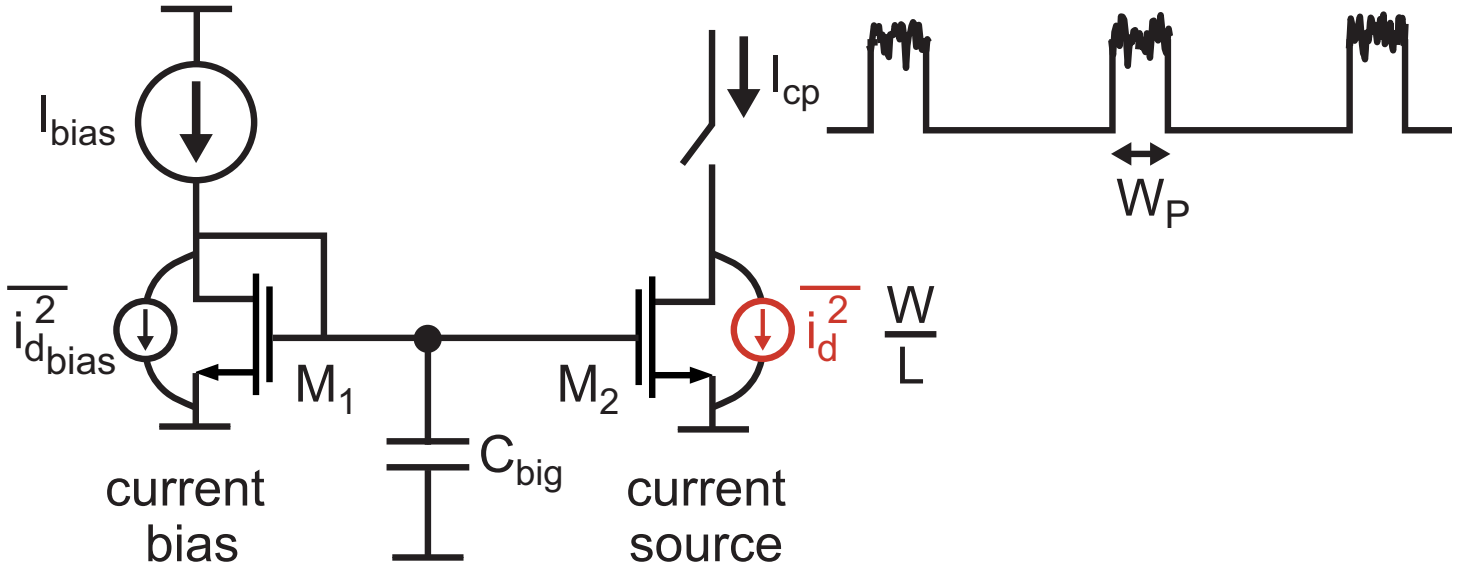
$$S_{\Phi_{npfd}}(f) = \left|\frac{N}{K_{pd}}G(f)\right|^2 S_{\Phi_{en}}(f)$$

- **VCO-referred noise:**

$$S_{\Phi_{nvco}}(f) = |1 - G(f)|^2 S_{\Phi_{vn}}(f)$$

- **Overall:** $S_{\Phi_{out}}(f) = S_{\Phi_{npfd}}(f) + S_{\Phi_{nvco}}(f)$

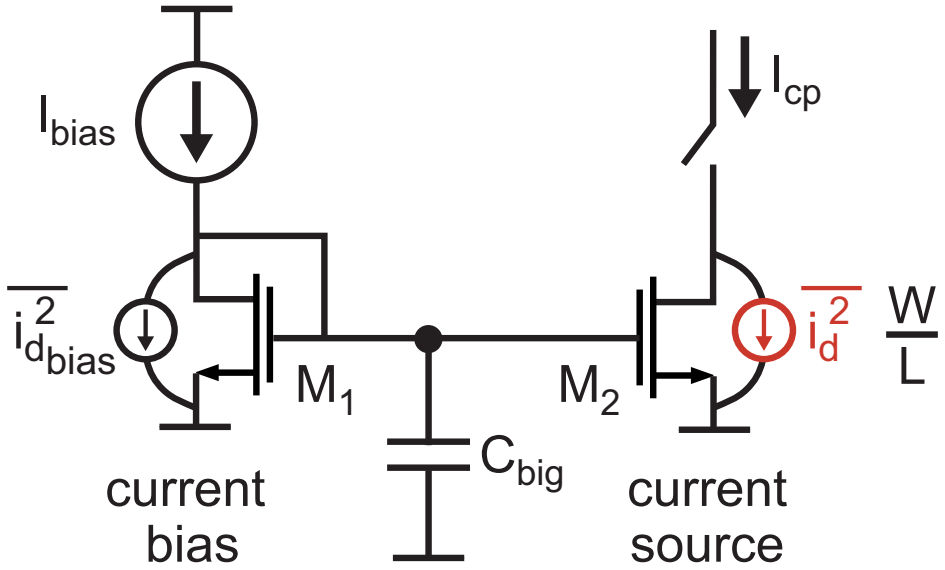
Take a Closer Look at Charge Pump Noise



- **Spectral density of charge pump noise is a function of device noise and pulse width**
  - **Short pulse widths reduce effective charge pump noise**

Tristate PFD has an advantage of allowing short pulse widths (i.e., lower noise) during steady-state operation

Impact of Transistor Current Magnitude on Noise



- **Charge pump noise will be related to the current it creates as**

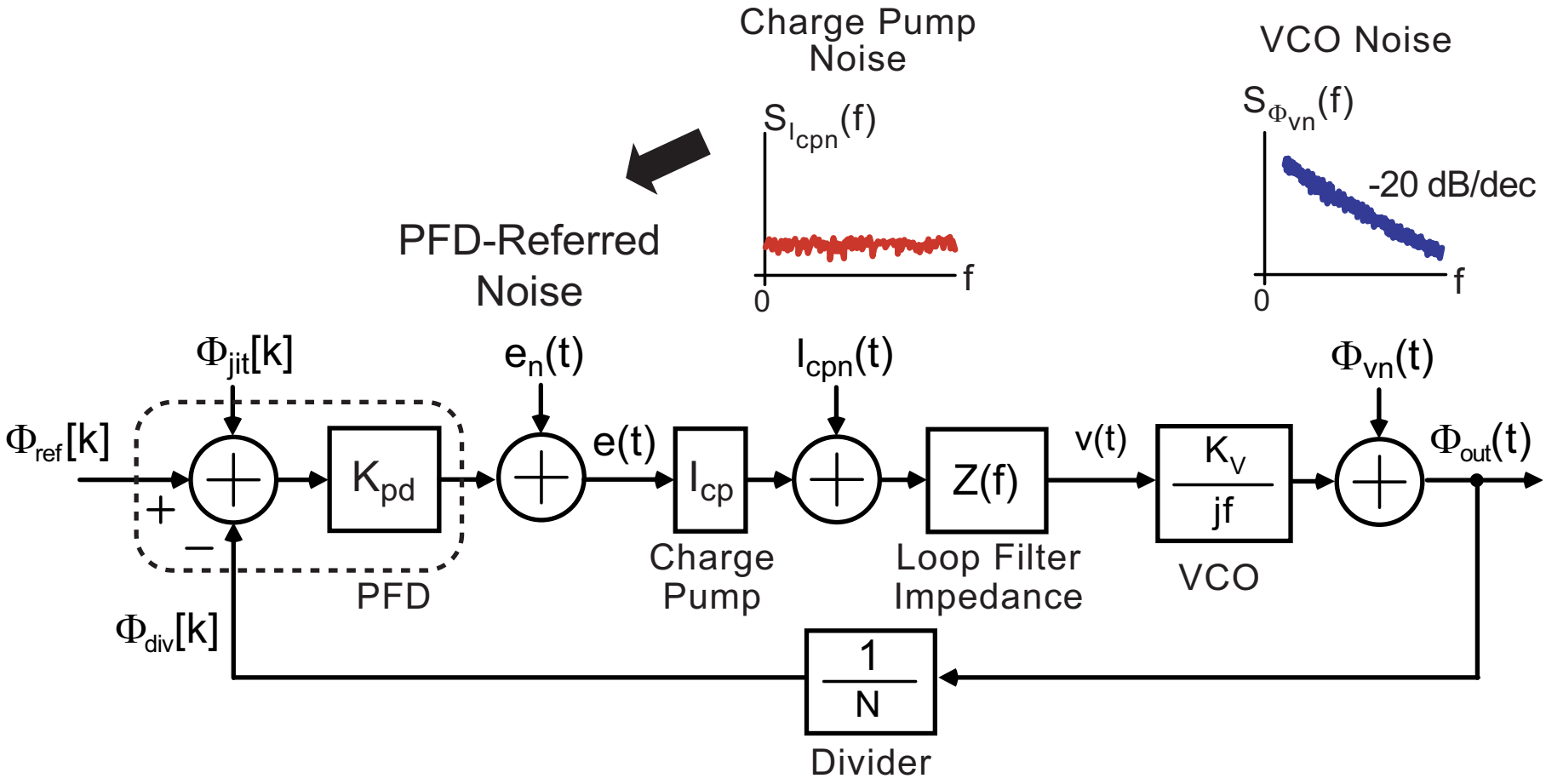
$$S_{I_{cpn}}(f) \propto \frac{\overline{I_{cp}^2}}{\Delta f} = 4kT\gamma g_{do}$$

- **Recall that g_{do} is the channel resistance at zero V_{ds}**
  - **At *a fixed current density*, we have**

$$g_{do} \propto \sqrt{I_{cp}W} \propto I_{cp} \quad \Rightarrow \quad \boxed{S_{I_{cpn}}(f) \propto I_{cp}}$$

  - **Therefore, charge pump noise is proportional to I_{cp}**

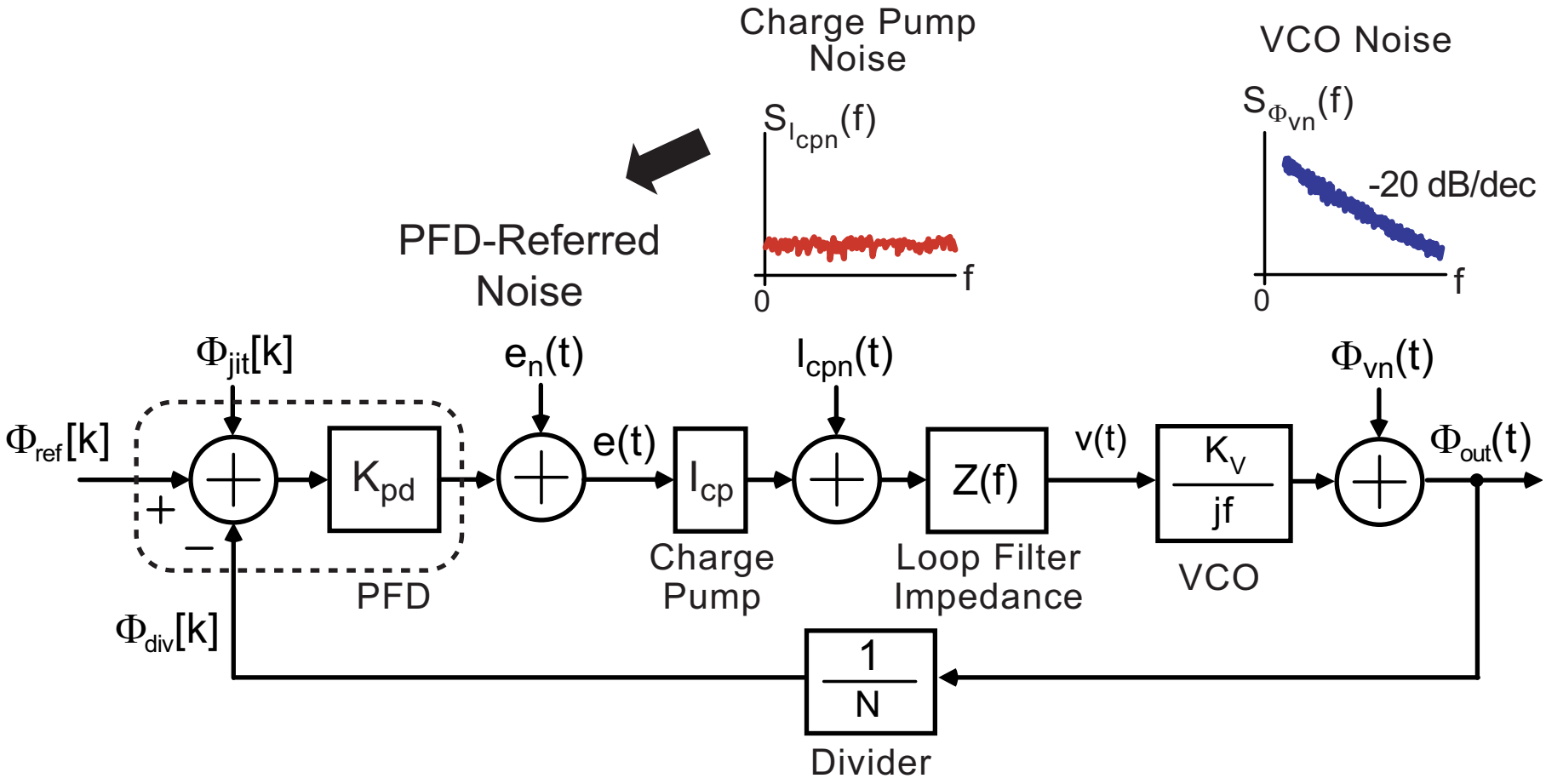
Analysis of Charge Pump Noise Impact



- **Transfer function from charge pump noise to PLL output is found by referring noise to PFD output by factor $1/I_{cp}$**

$$\frac{\Phi_{out}}{I_{cpn}} = \left(\frac{1}{I_{cp}}\right)\frac{\Phi_{out}}{e_n} = \left(\frac{1}{I_{cp}}\right)\frac{N}{K_{pd}}G(f)$$

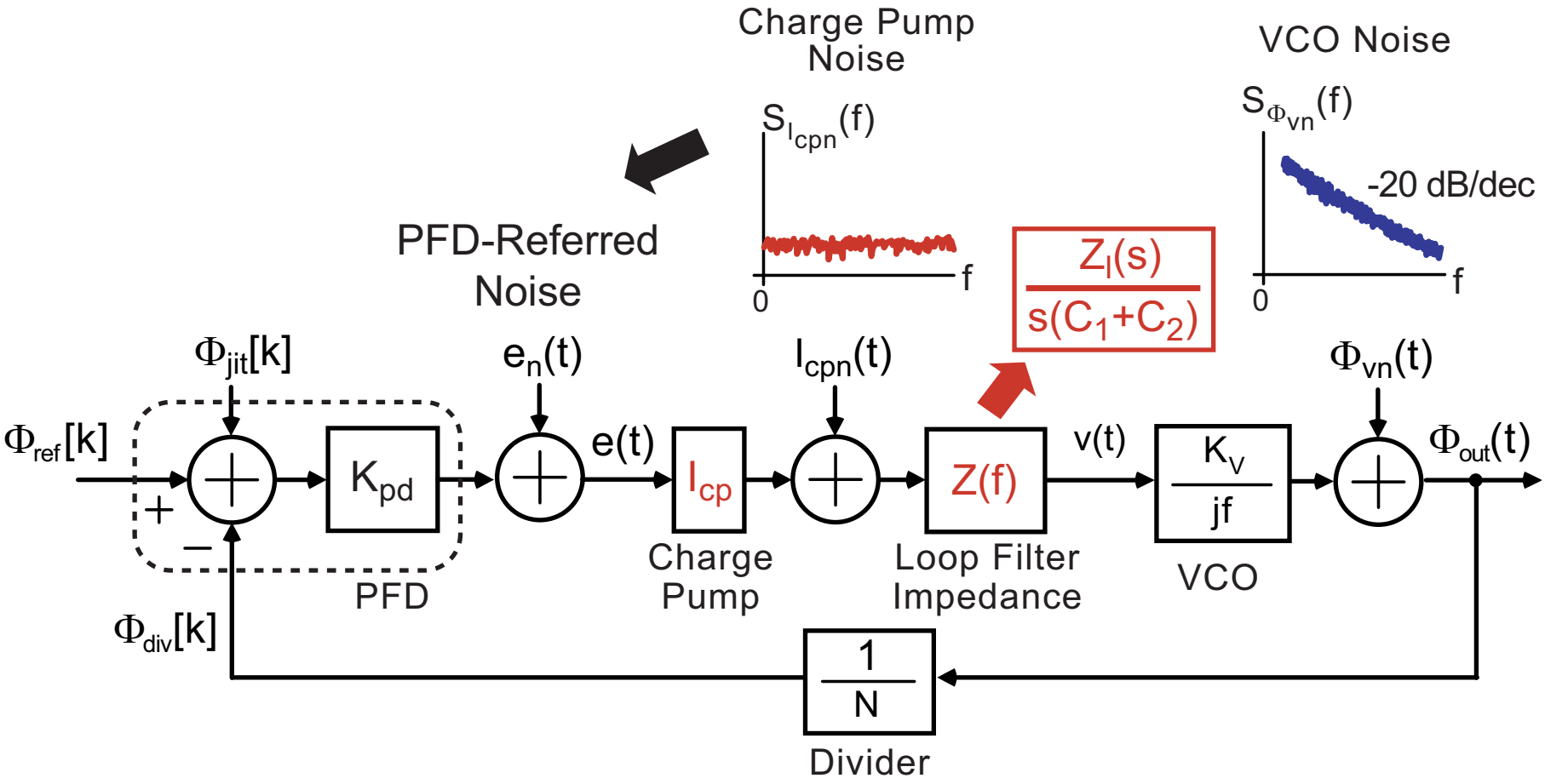
Increasing I_{cp} Leads to Reduced Noise at PLL Output



- **Output phase noise due to charge pump:**

$$S_{\Phi_{out}}(f) = \left|\left(\frac{1}{I_{cp}}\right)\frac{N}{K_{pd}}G(f)\right|^2 S_{I_{cpn}}(f) \propto \left|\frac{1}{I_{cp}}\right|^2 I_{cp} \quad \boxed{\propto \frac{1}{I_{cp}}}$$

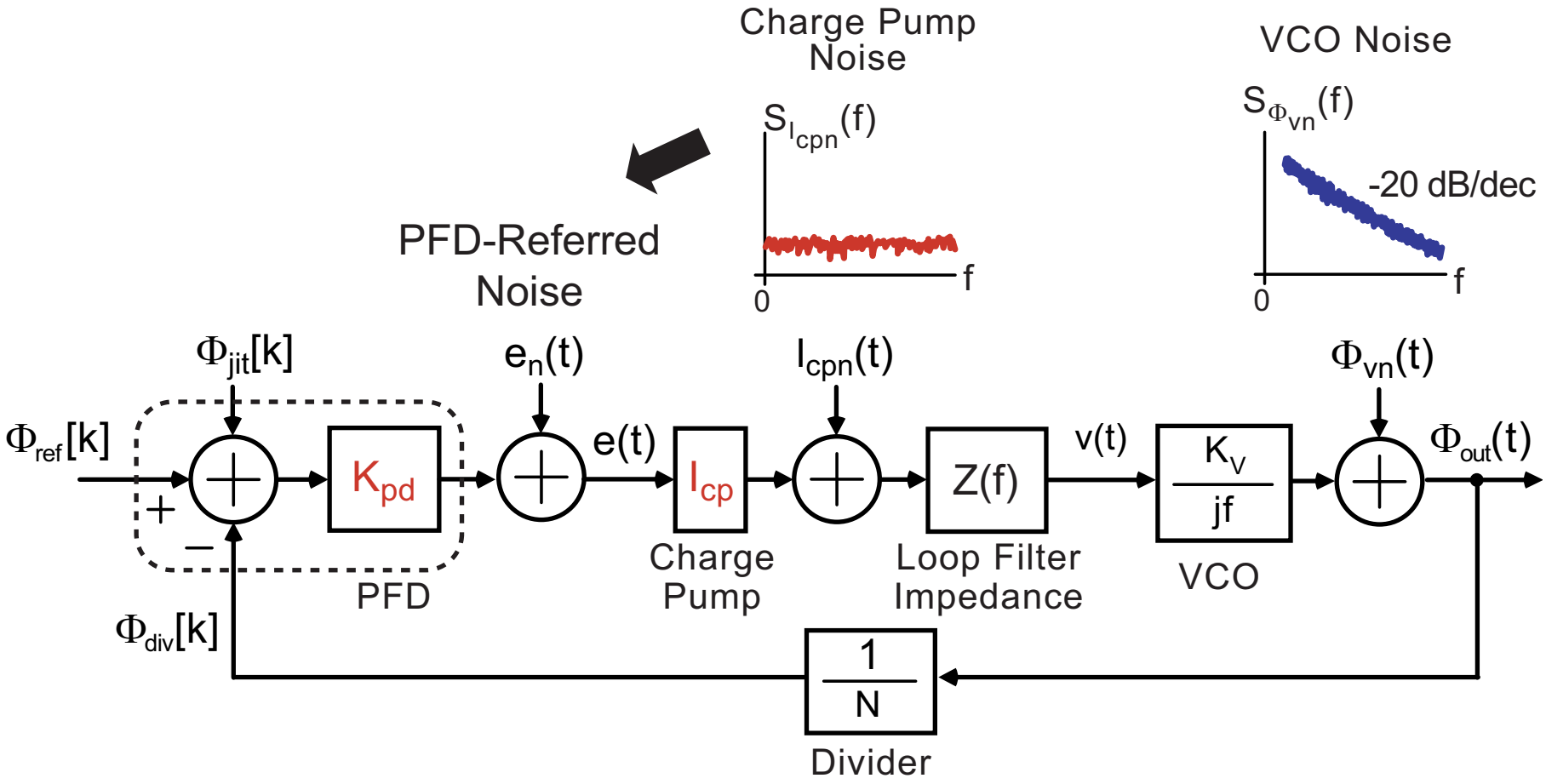
Issue: Increasing I_{cp} Leads to Larger Loop Filter



- **To keep PLL BW unchanged, assume $I_{cp}/(C_1+C_2)$ is held constant (to maintain open loop gain)**

Area gets larger since increasing I_{cp} leads to increased loop filter capacitance (C_1+C_2)

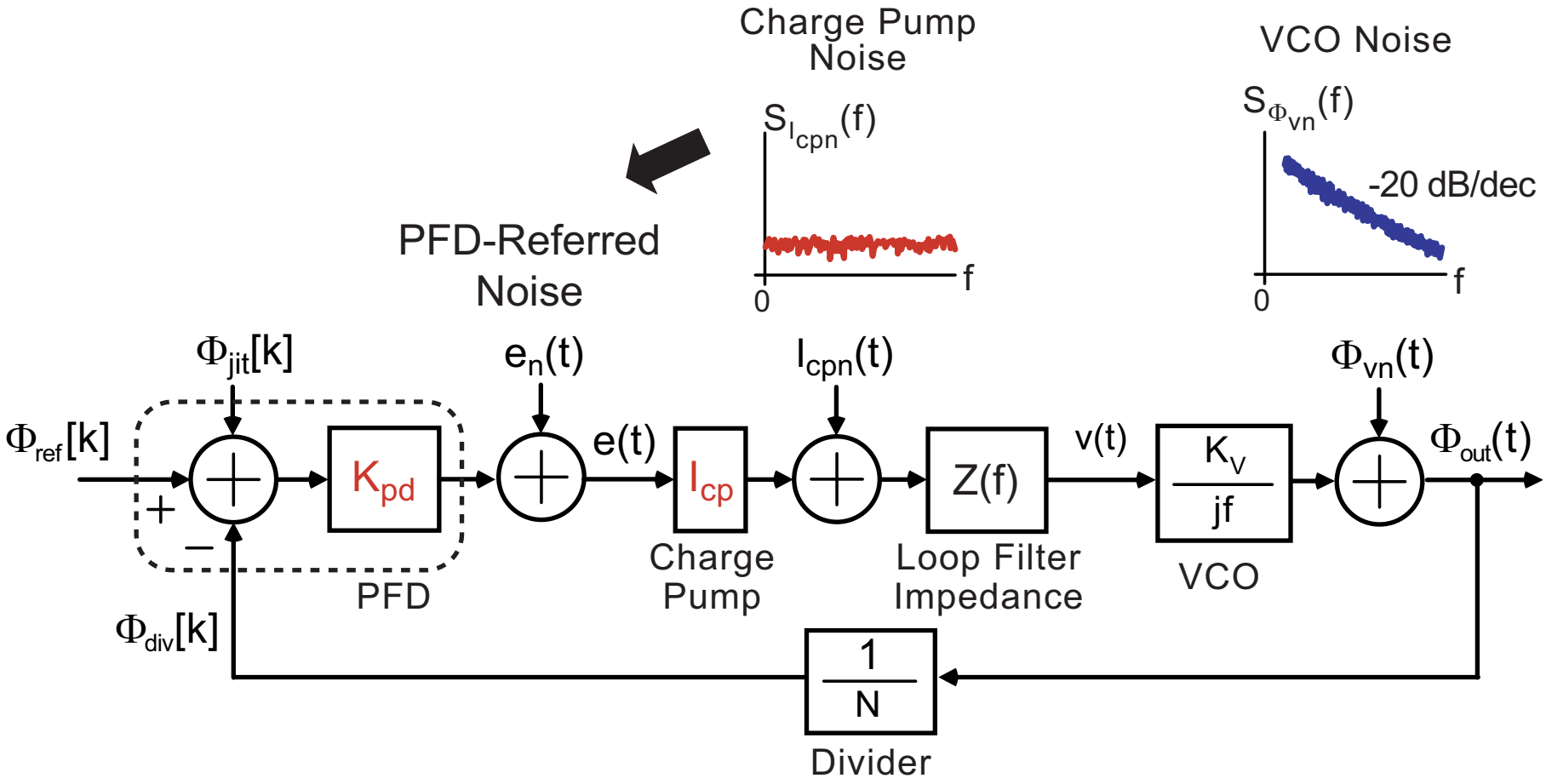
Better Approach: Increase PD Gain to Lower Noise



- **To keep PLL BW unchanged, assume $I_{cp}K_{pd}$ held constant**
  - **Loop filter can remain *unchanged* as K_{pd} is increased**

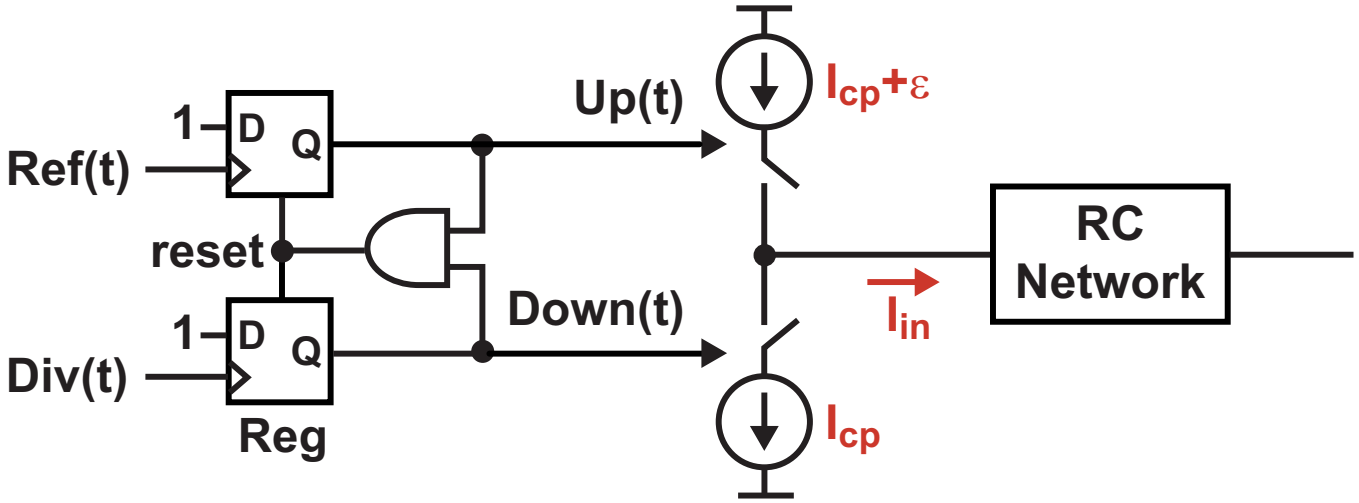
$$S_{\Phi_{out}}(f) = \left|\left(\frac{1}{I_{cp}}\right)\frac{N}{K_{pd}}G(f)\right|^2 S_{I_{cpn}}(f) \propto I_{cp} \quad \boxed{\propto \frac{1}{K_{pd}}}$$

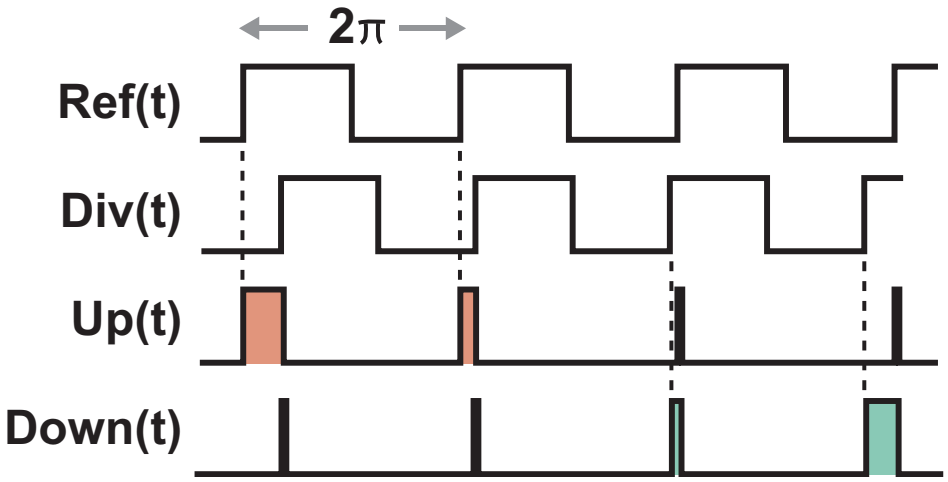
Can We Increase PD Gain for a Charge Pump PLL?



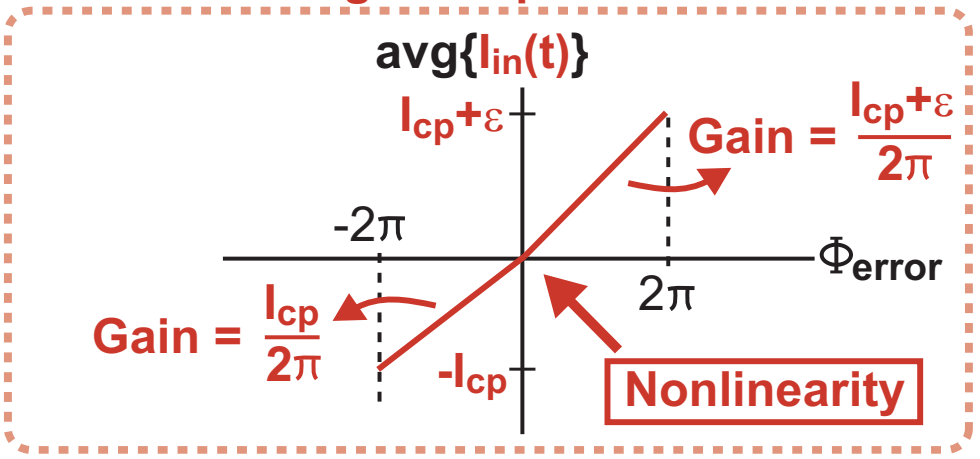
- **XOR-based PD provides factor of two higher gain than a tristate PFD**
  - **Key issue: carries an overall noise penalty since the charge pump is never gated off (i.e., generates long pulses)**
  - **XOR PD rarely used due to its noise penalty**

Key Issue of Tristate PFD: Charge Pump Mismatch



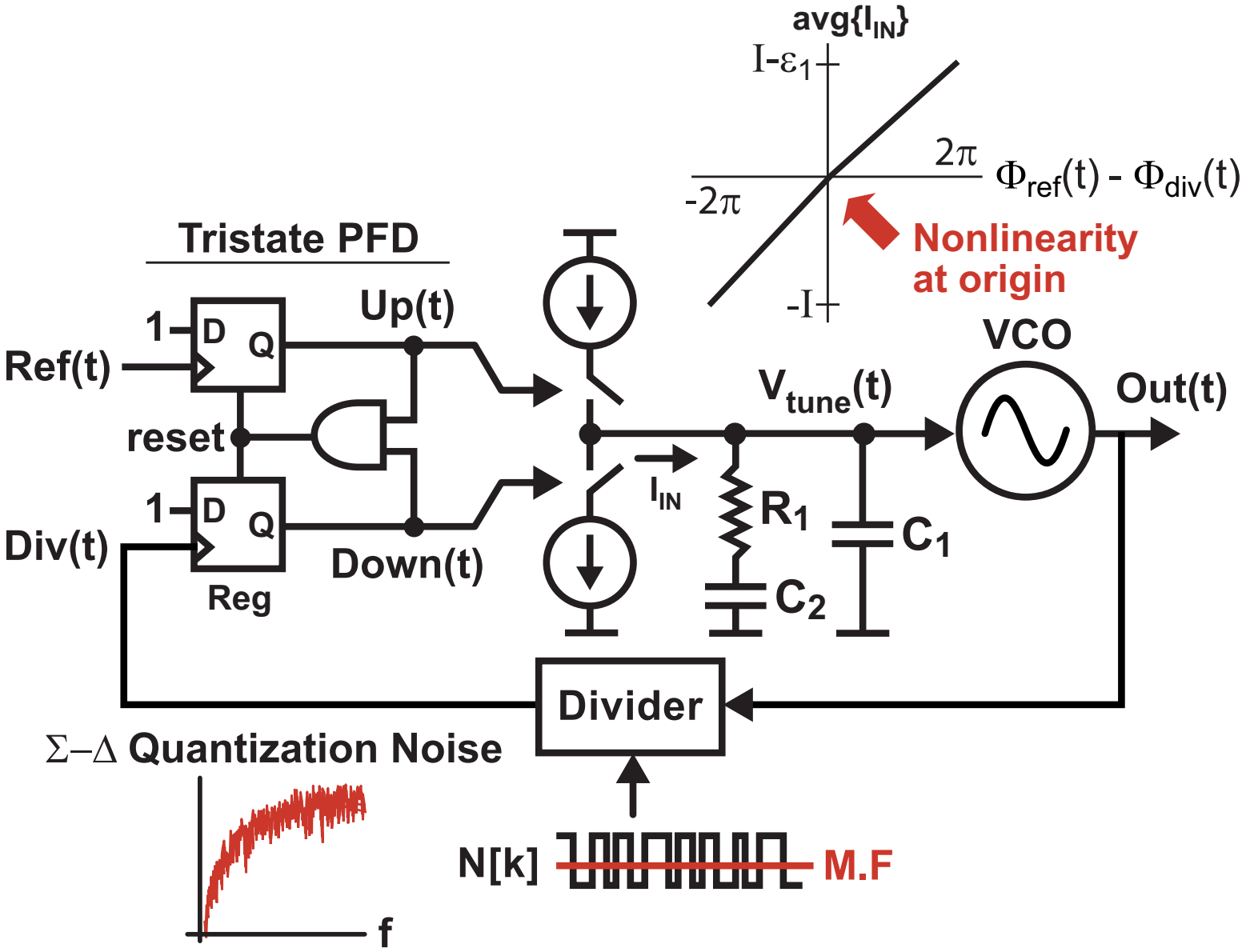


PD & Charge Pump Characteristic



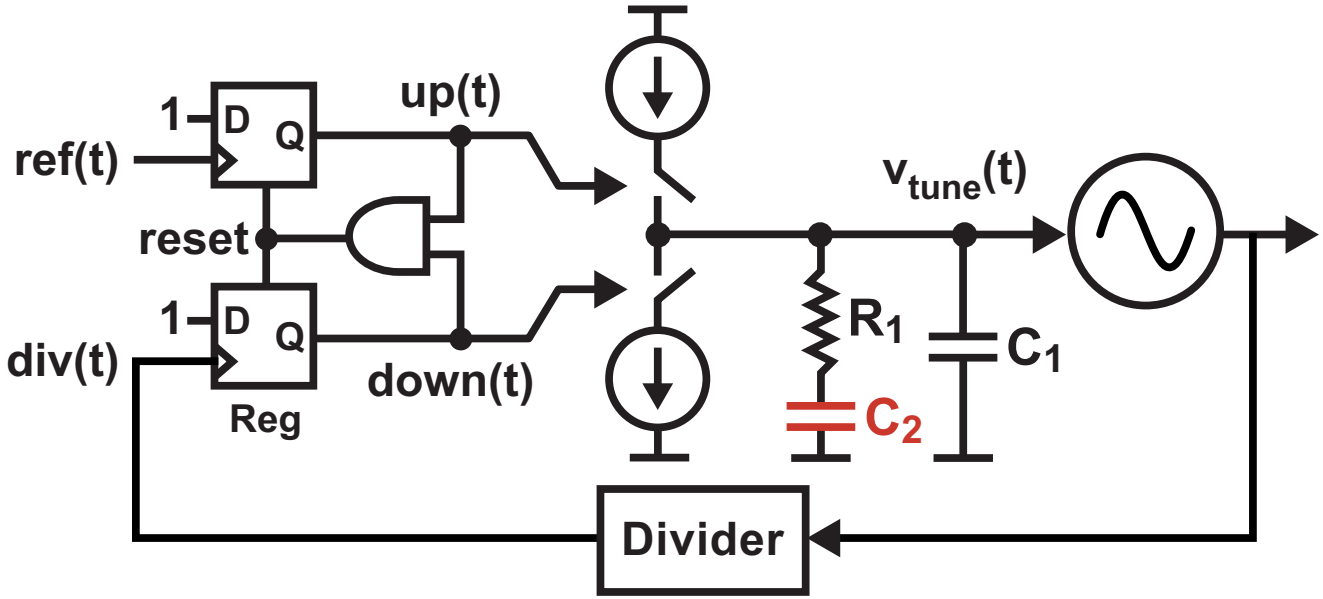
- Mismatch of charge pump Up/Down currents leads to nonlinearity in the PLL phase comparison path when tristate PFD used

Nonlinearity Causes Noise Folding with Frac-N PLLs



- Significant analog design effort is often required to avoid this issue

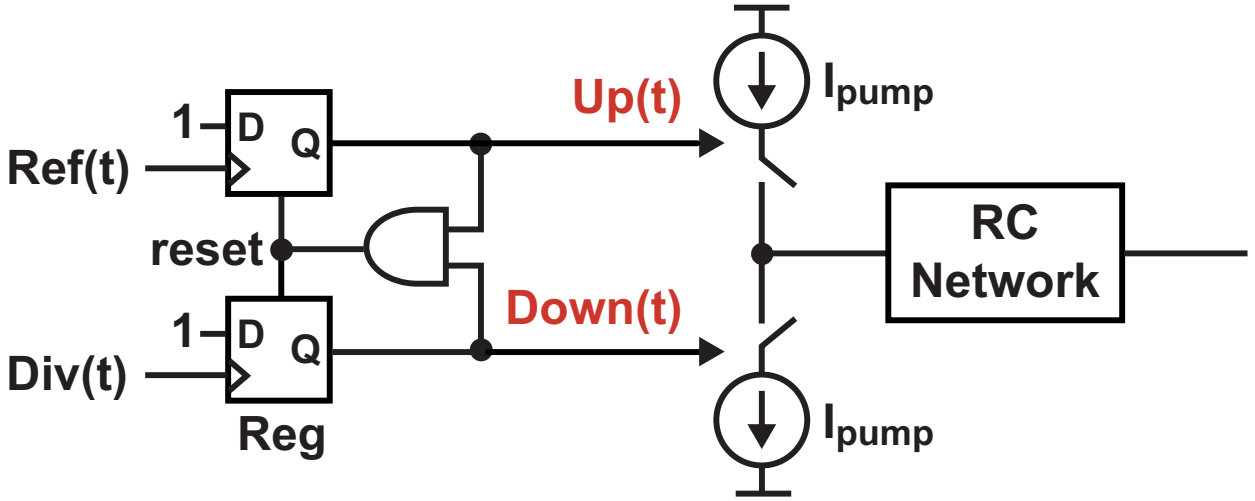
Summary of Charge Pump PLL Issues

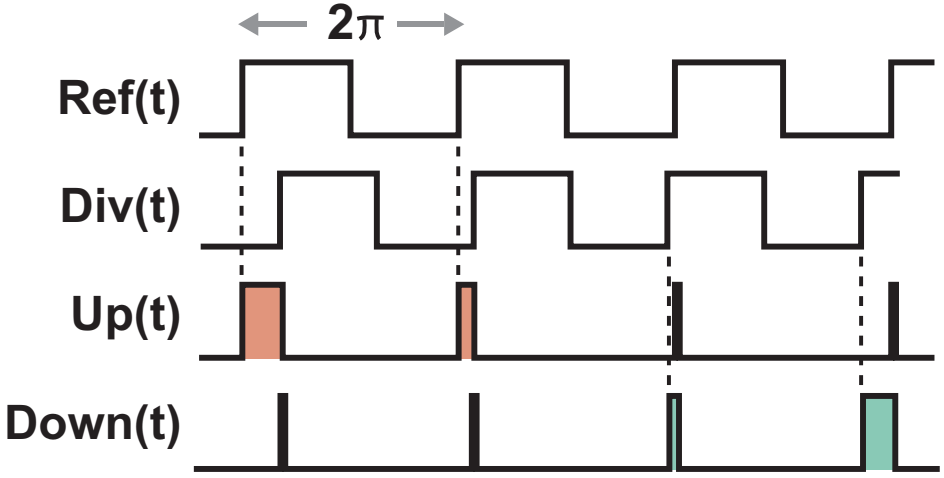


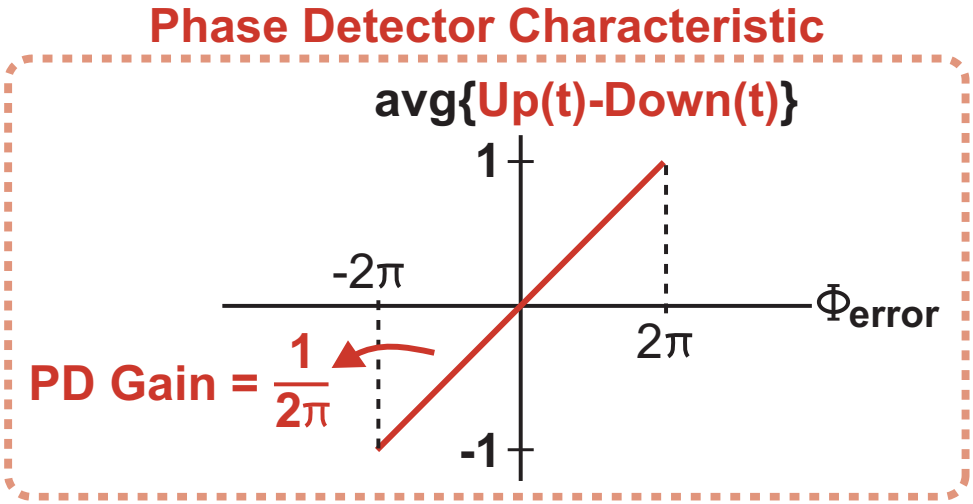
- Tristate PFD has issues with
  - Low PD gain – leads to increased loop filter for given PLL noise
  - Charge pump nonlinearity – causes quantization noise folding
- Charge Pump has issues with
  - Nontrivial analog design effort for wide range, high output impedance, low leakage, reasonable matching, low noise

Are there alternative analog PLL architectures?

How Do We Achieve Higher PD Gain?

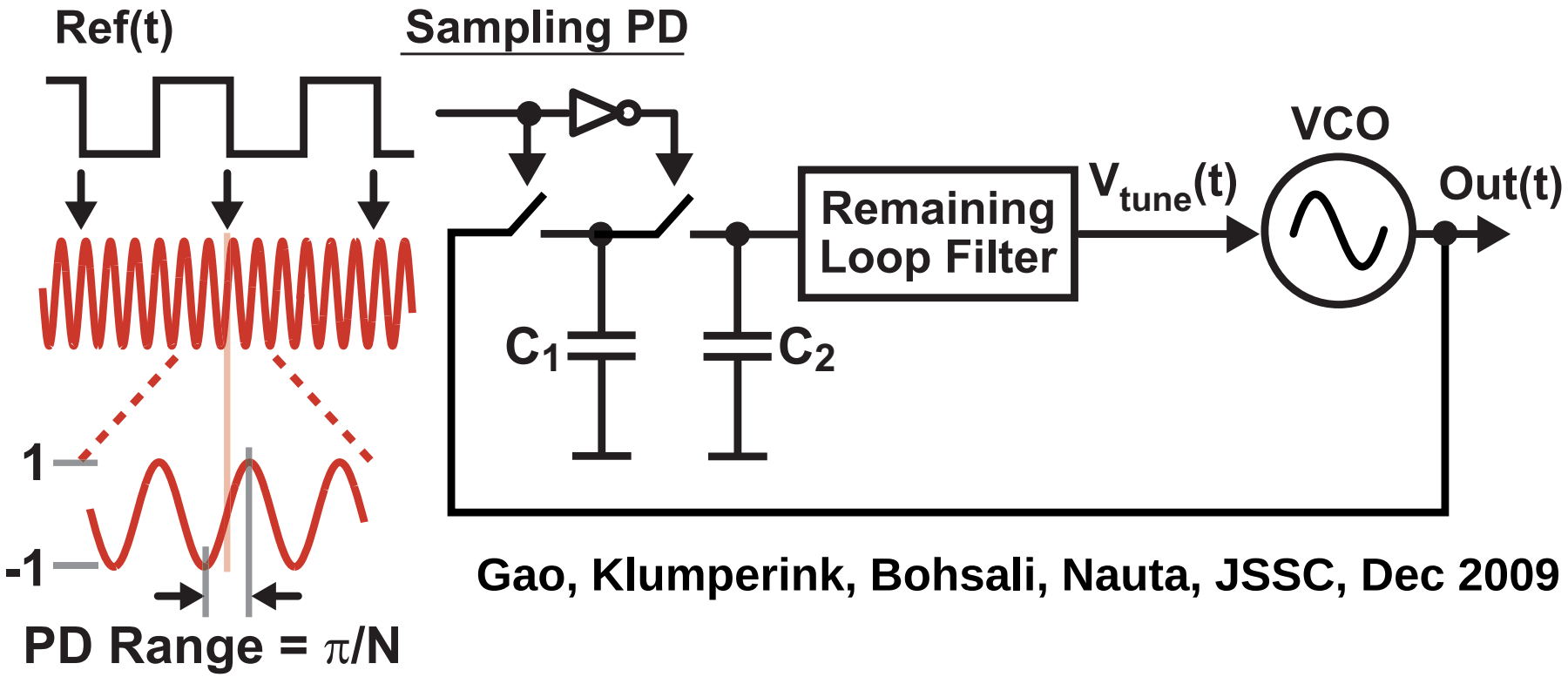






- Use tristate PD as our starting point
  - Range of detector spans 2 Reference periods (i.e., 4π radians)
  - PD gain is 2/(PD range) = 2/(4π) = 1/(2π)

Sampled PD Achieves Much Higher PD Gain

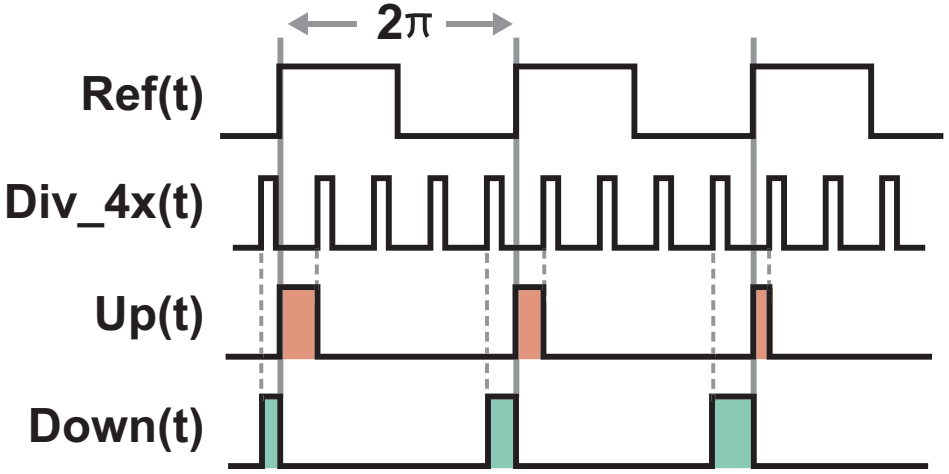


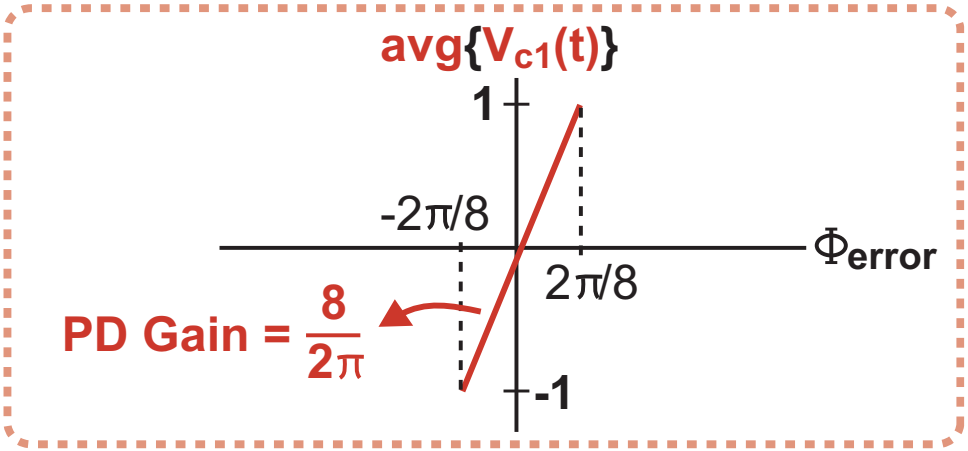
Gao, Klumperink, Bohsali, Nauta, JSSC, Dec 2009

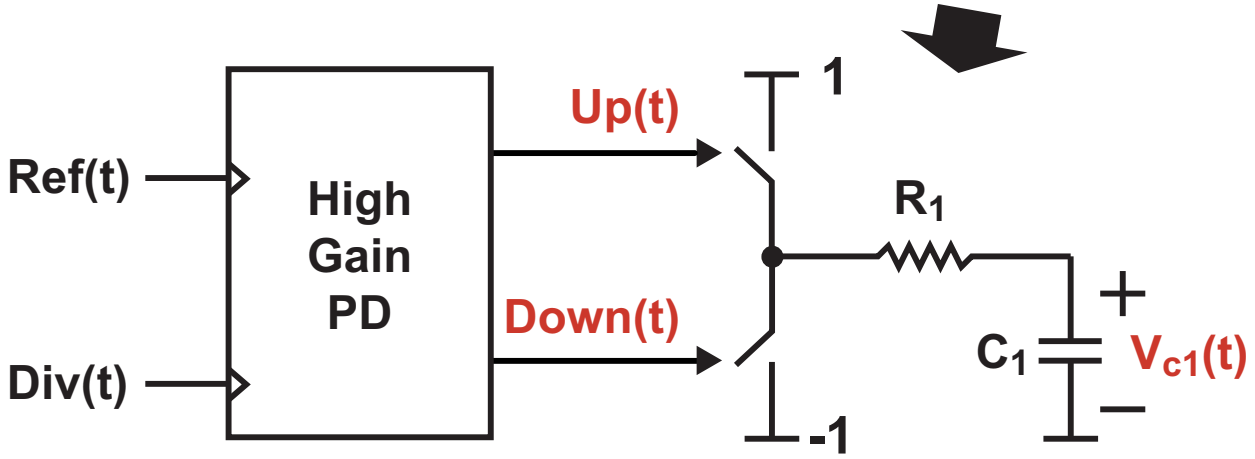
- **Directly sample VCO signal at reference edges**
  - **PD gain becomes 2/(π/N) = 2N/π assuming**
    - N = VCO Frequency)/(Ref Frequency)
    - PD output voltage range assumed to be -1 to 1

Yields much lower in-band PLL noise, but constrained to integer-N PLL structures

Achieving Higher PD Gain for a Fractional-N PLL

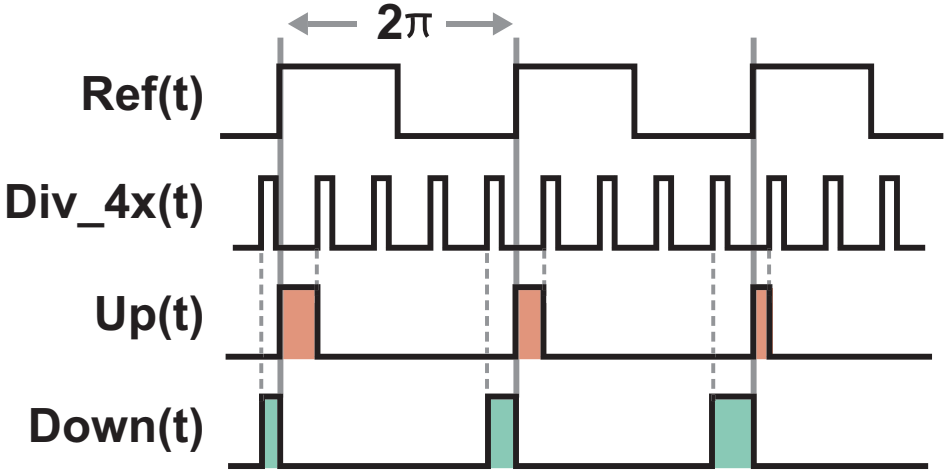


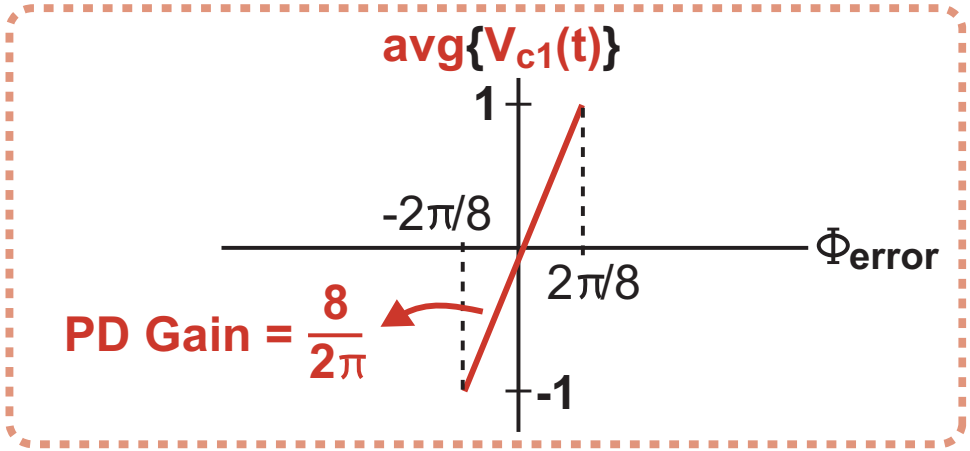




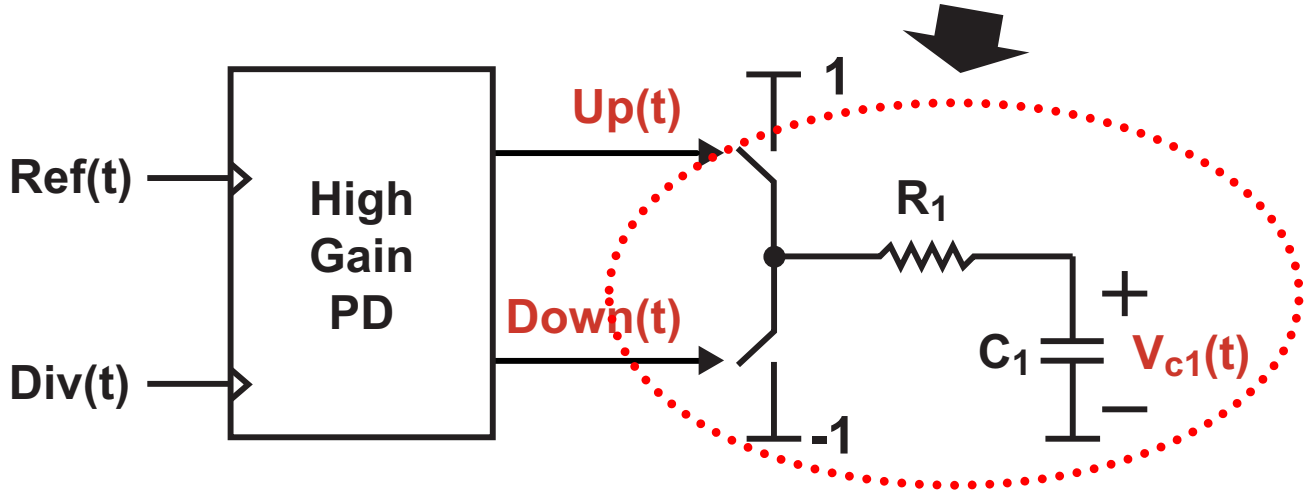
- Develop a PD with reduced phase error range in which Up/Down pulses vary in width in opposite directions
  - Need an appropriate loop filter topology that properly leverages the reduced PD range for higher PD gain

Key Implementation Detail: Use Switched Resistor



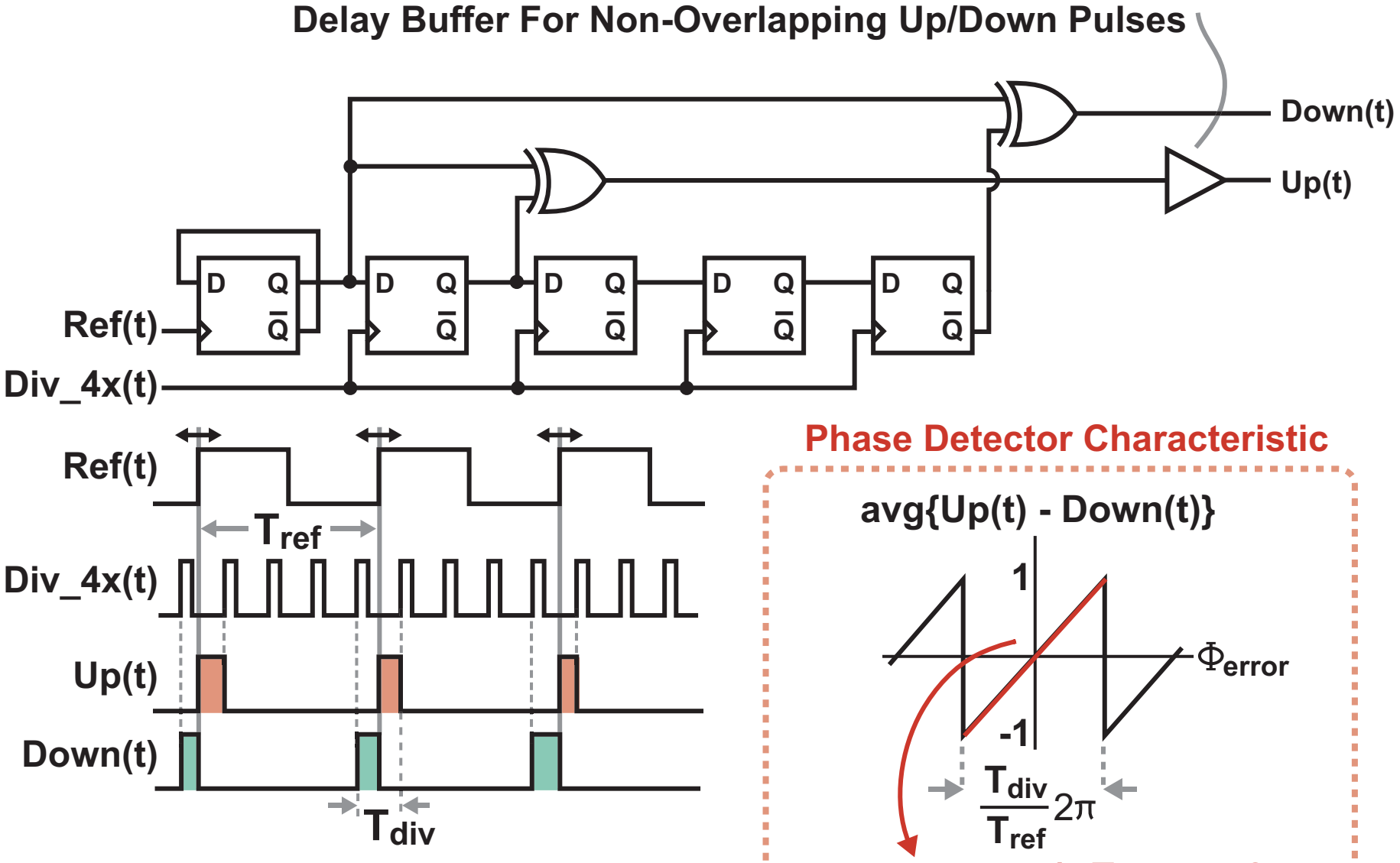


See also:
Hedayati, Bakkaloglu
RFIC 2009



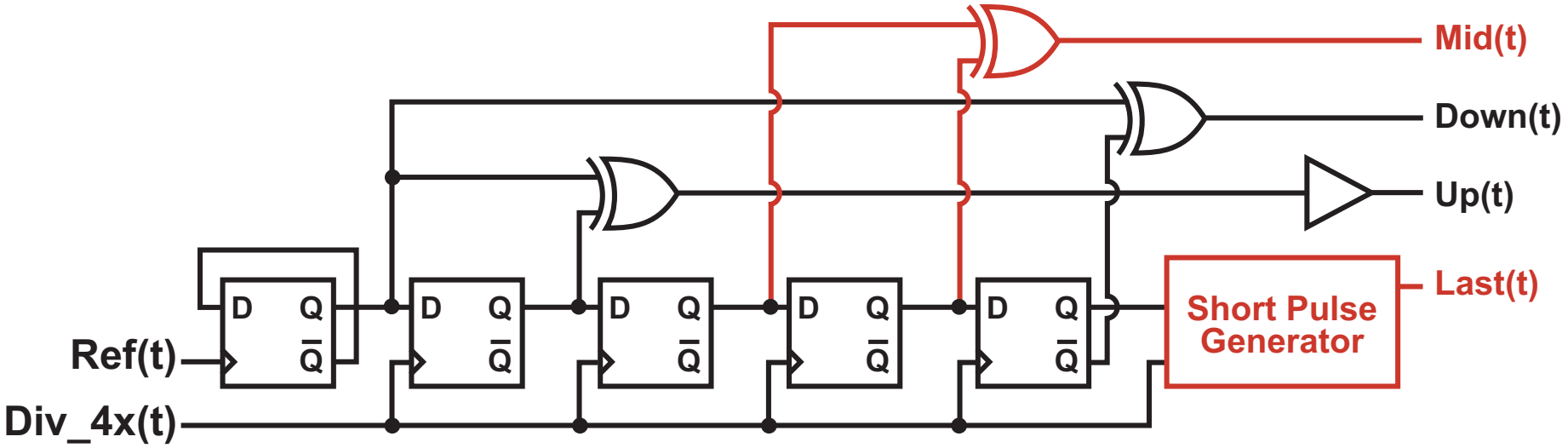
- Switching to voltage Supply/Gnd causes $V_{c1}(t)$ to reflect the average of the Up/Down pulses *within* the reduced PD range
  - PD gain is increased since full voltage range at V_{c1} achieved across a reduced phase error range

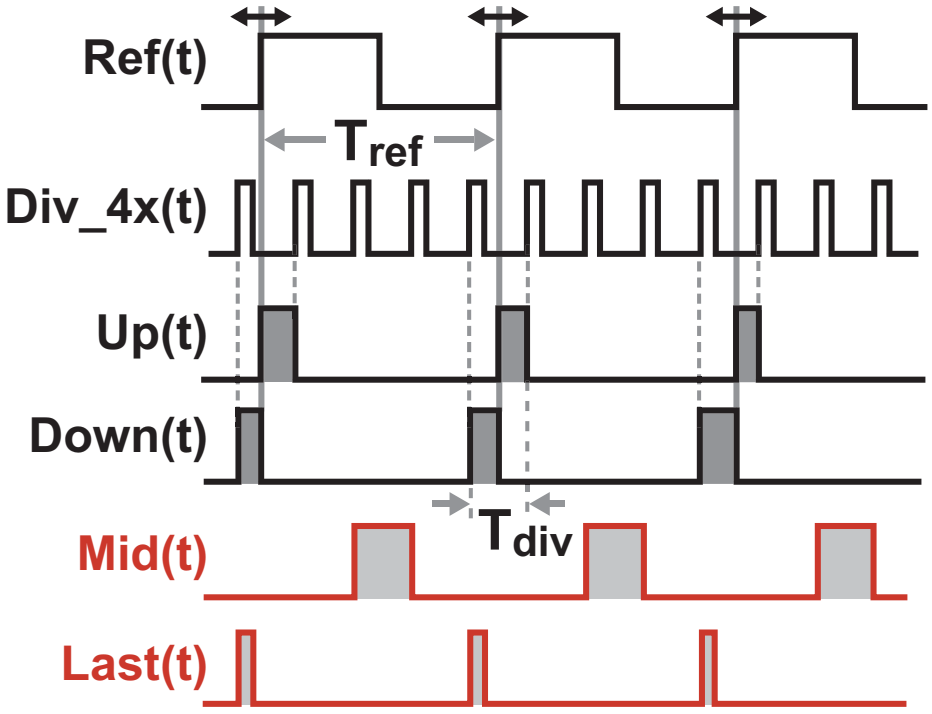
Implementation of High Gain Phase Detector



- Use 4X higher divider frequency
  - Simple digital implementation

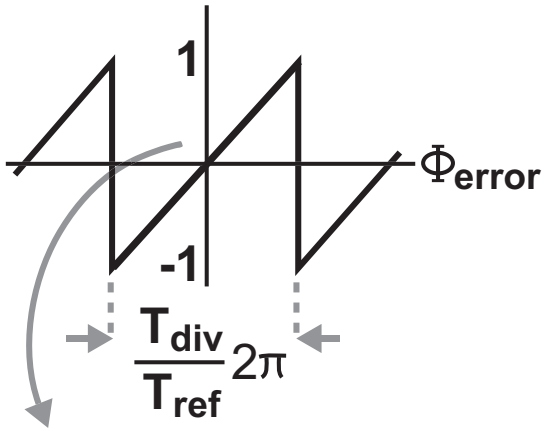
Multi-Phase Pulse Generation (We'll Use it Later…)





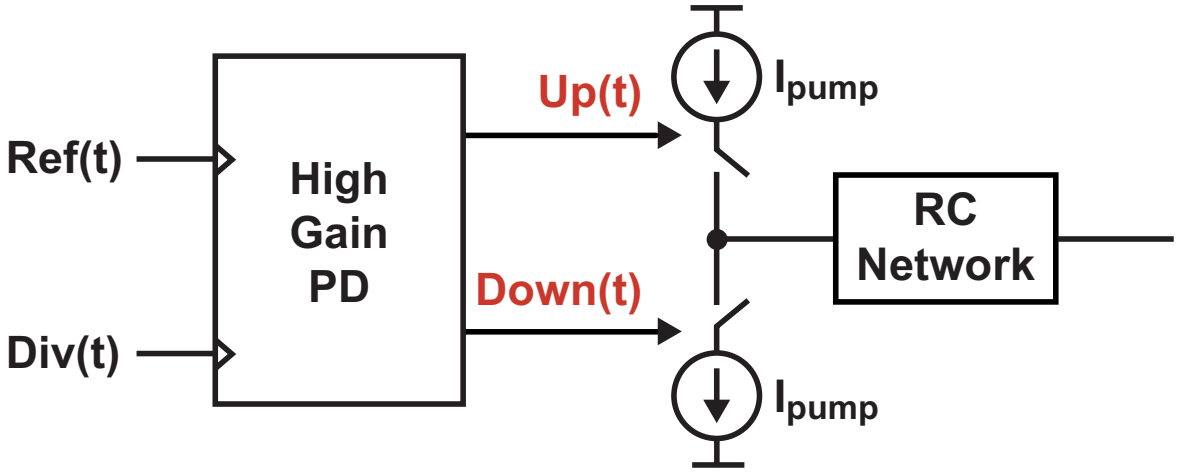
Phase Detector Characteristic

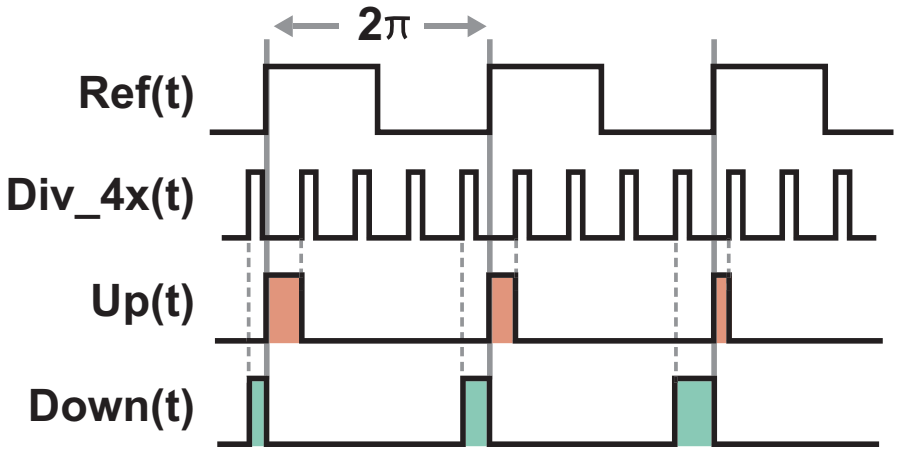
avg{Up(t) - Down(t)}

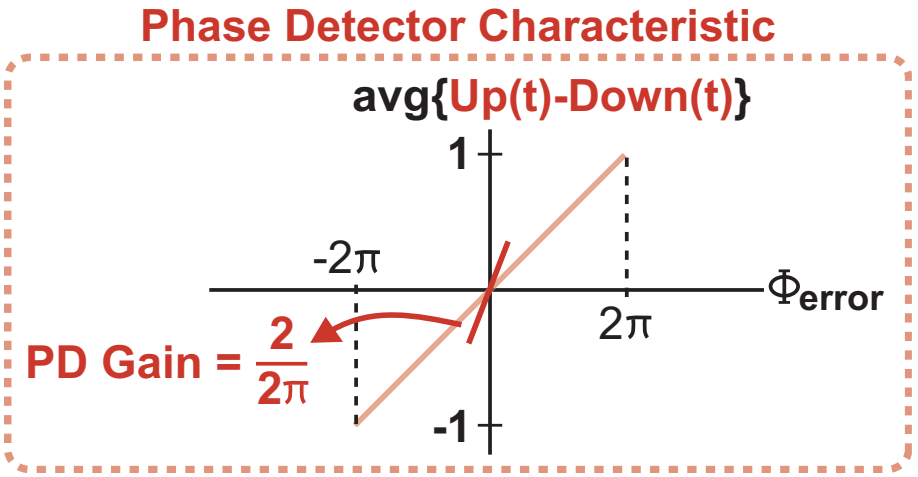


$$\text{PD Gain} = \frac{1}{2\pi}\frac{T_{ref}}{T_{div}}2 = \frac{8}{2\pi}$$

What If We Use A Charge Pump with the High Gain PD?

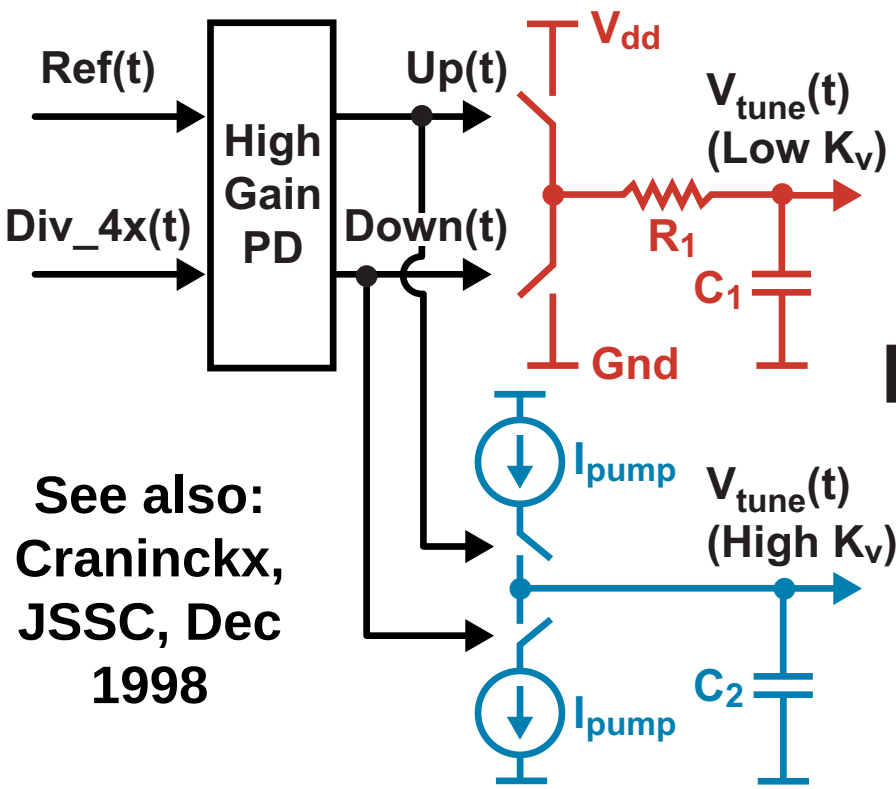




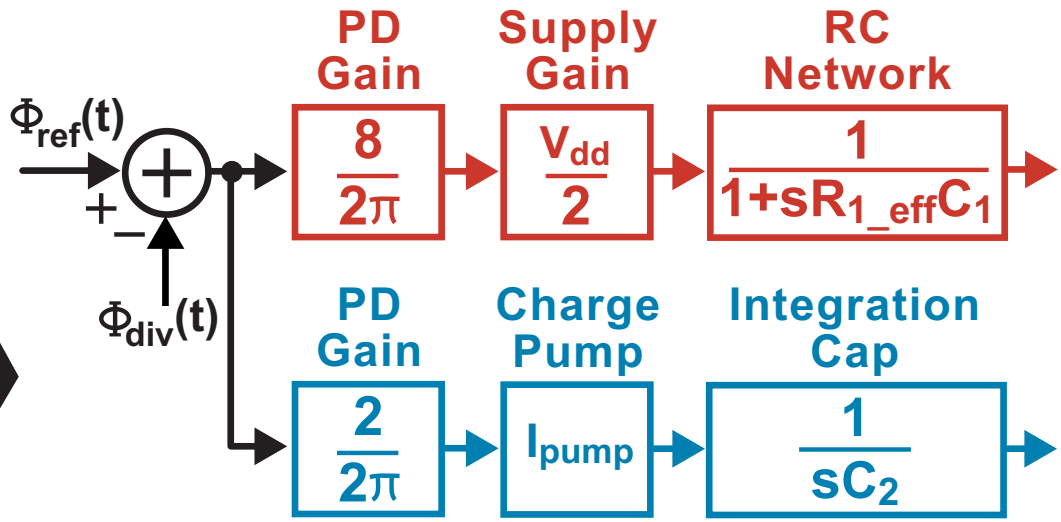


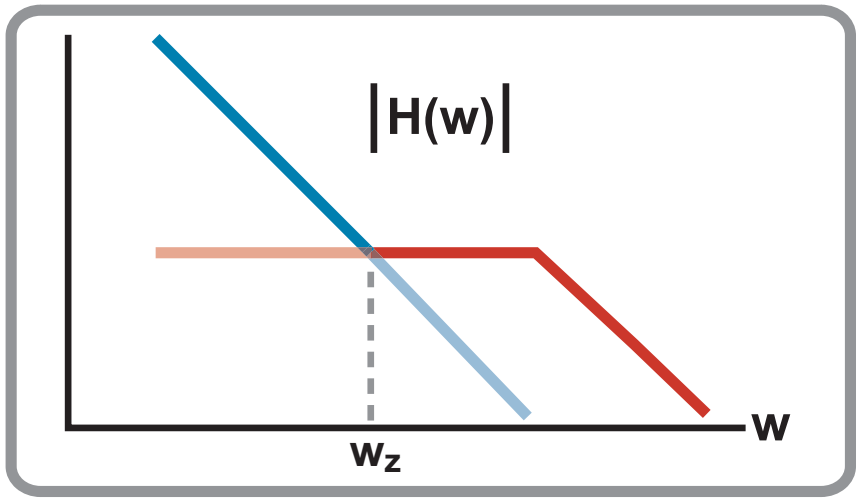
- PD Gain increased by 2 compared to tristate PFD
  - Reduced phase error range and max/min current occurs
- High linearity despite charge pump current mismatch
  - Similar to XOR PD, but noise is reduced

Increasing Feedforward Gain While Utilizing Charge Pump



See also: Craninckx, JSSC, Dec 1998

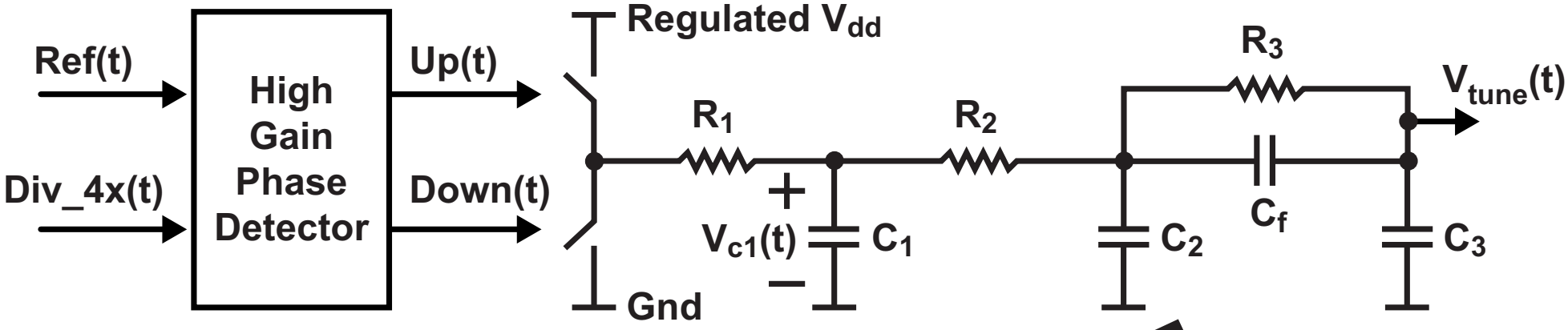


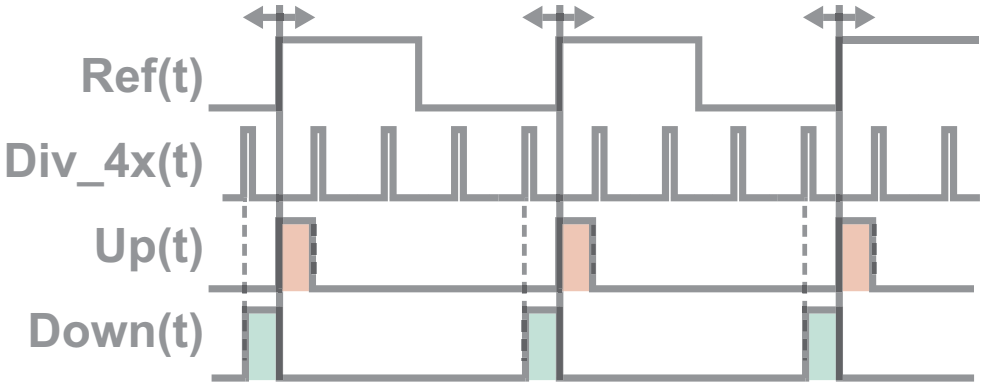


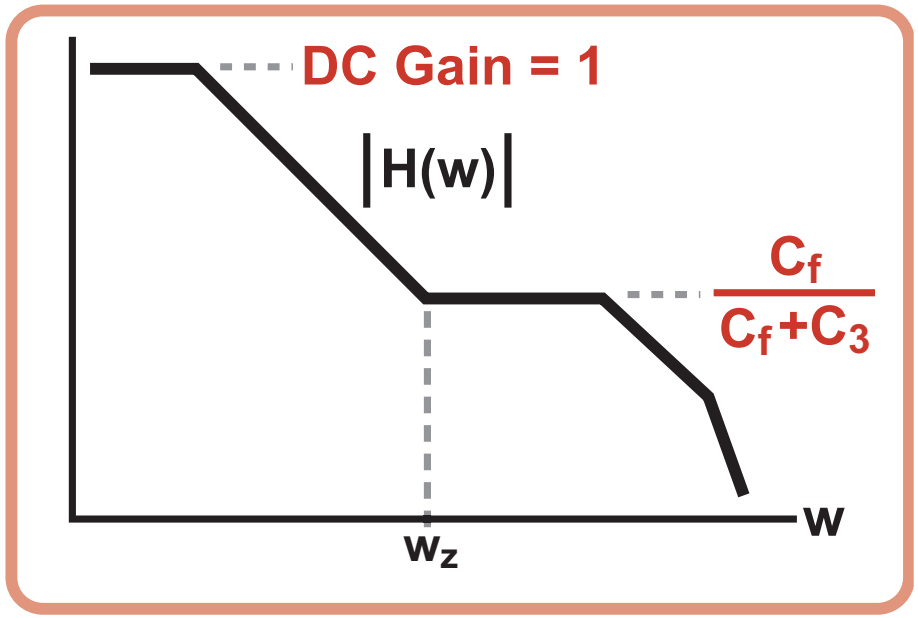
- We can use the high gain PD in a dual-path loop filter topology
  - But we want a simple design!

Can we remove the charge pump to reduce the analog design effort?

Passive RC Network Offers a Simpler Implementation

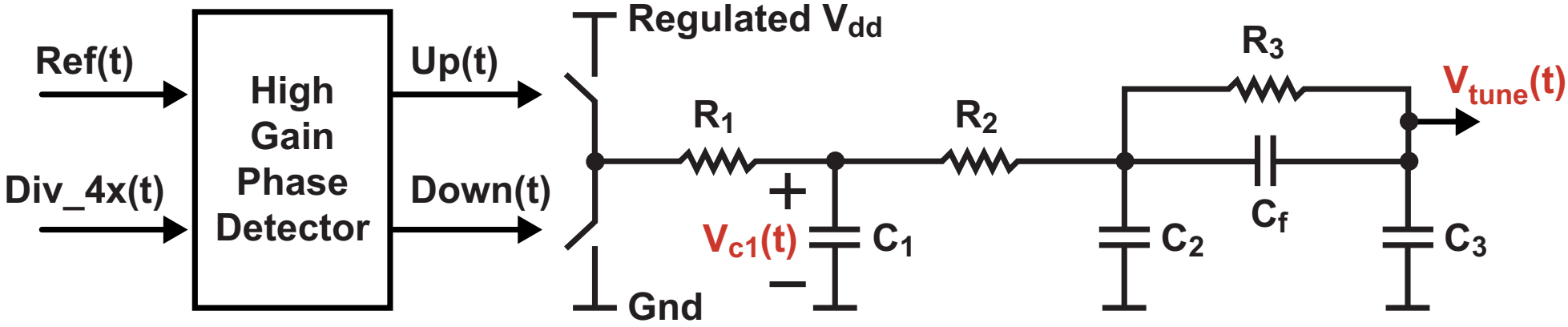


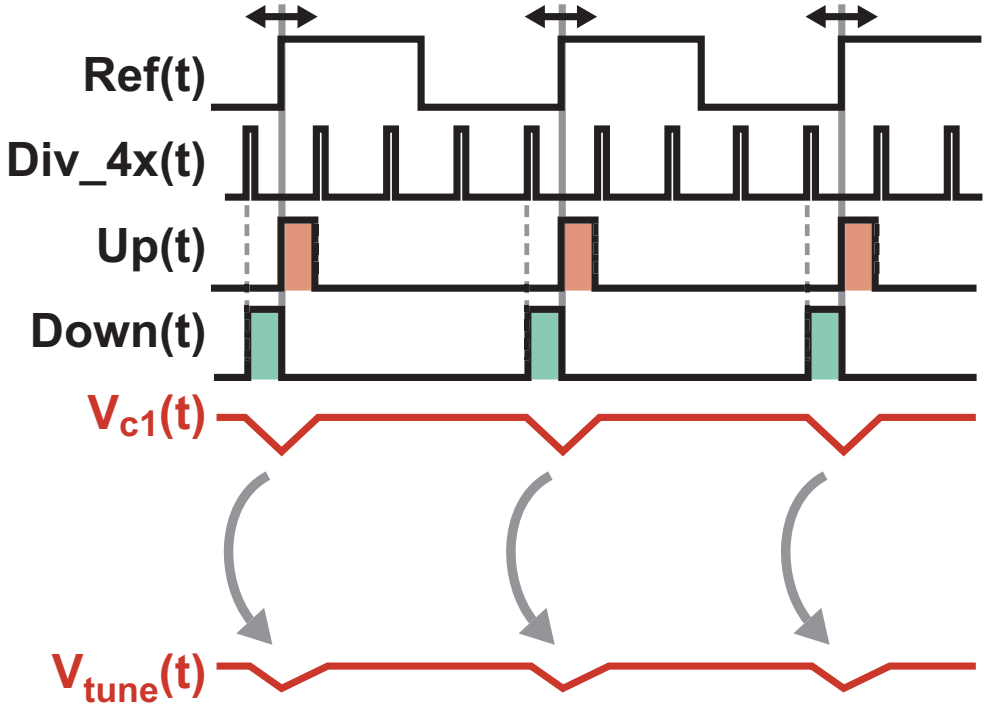




- Capacitive feedforward path provides stabilizing zero
- Design effort is simply choosing switch sizes and RC values

The Issue of Reference Spurs

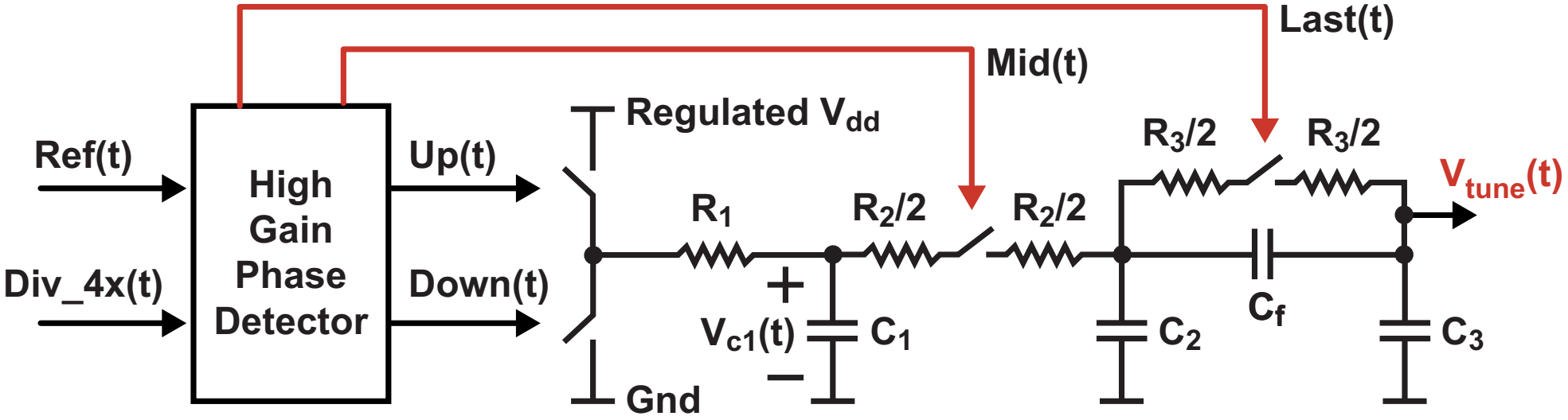


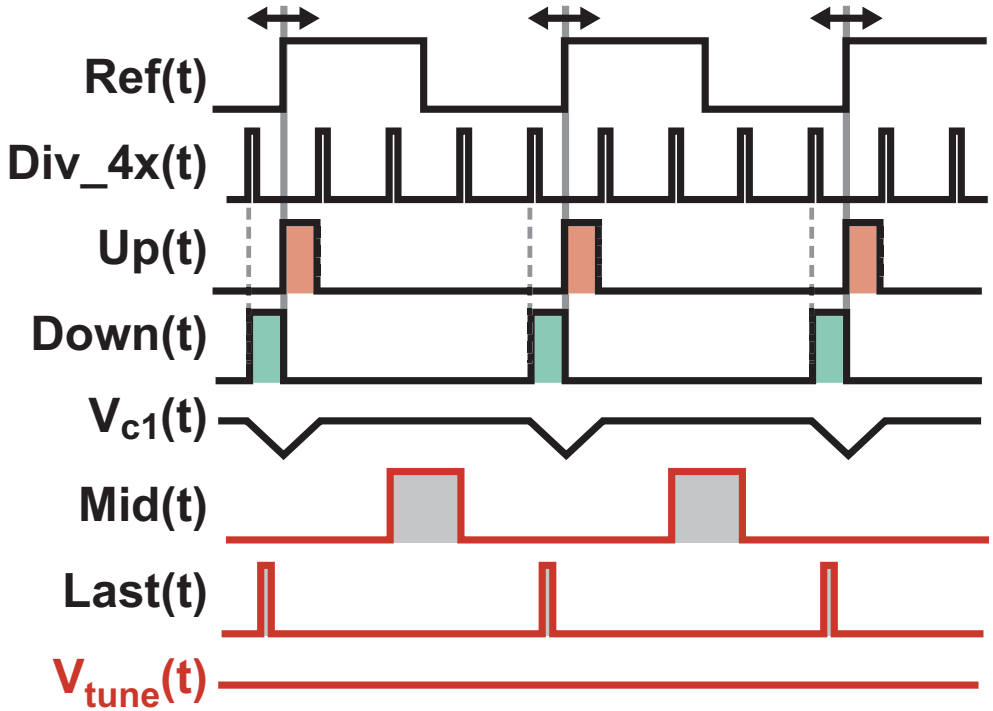


- Ripple from Up/Down pulses passes through to VCO tuning input

Is there an easy way to reduce reference spurs?

Leverage Multi-Phase Pulsing

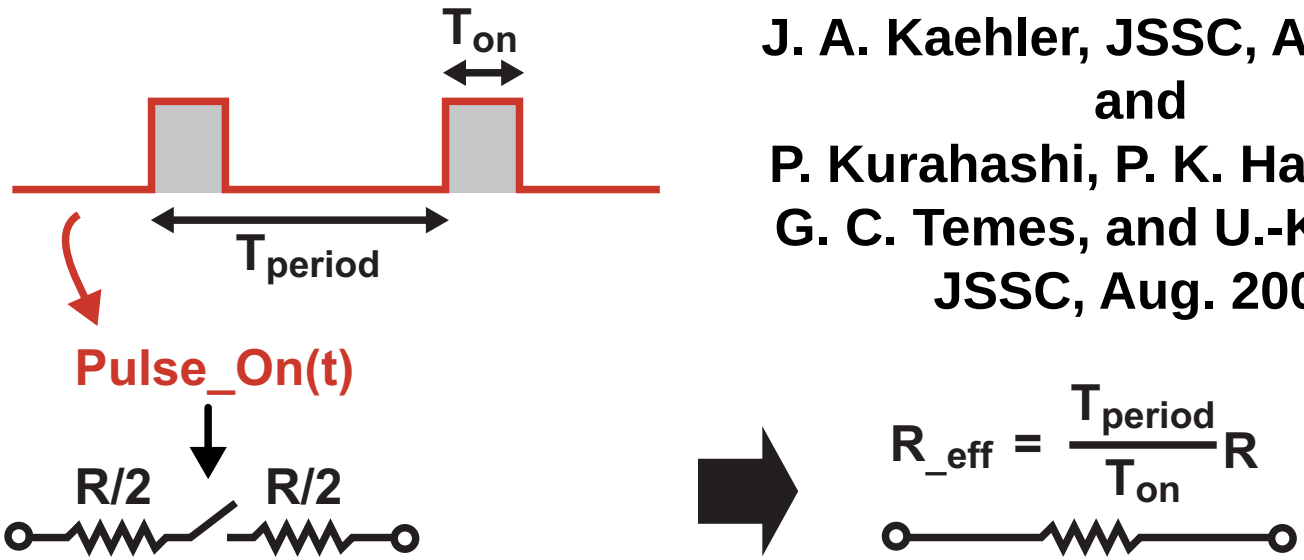




- Ripple from Up/Down pulses blocked before reaching VCO
  - Reference spurs reduced!
  - Similar to sample-and-hold technique (such as Zhang et. al., JSSC, 2003)

There is a nice side benefit to pulsing resistors…

Pulsing Resistor Multiplies Resistance!

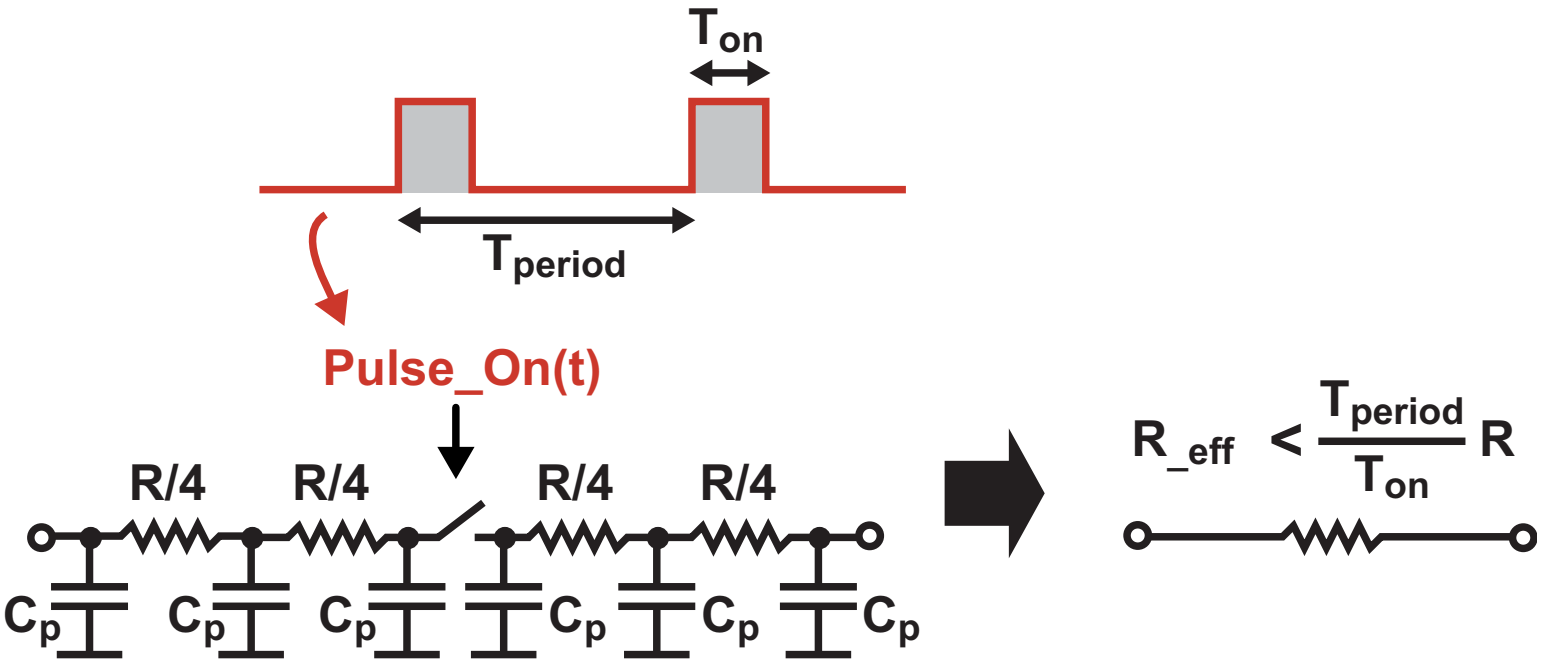


J. A. Kaehler, JSSC, Aug. 1969
and
P. Kurahashi, P. K. Hanumolu, G. C. Temes, and U.-K. Moon, JSSC, Aug. 2007

- **Resistor only passes current when pulsed on**
  - **Average current through resistance is reduced according to ratio of On time, T_{on}, versus pulsing Period, T_{period}**
  - ***Effective* resistance is actual resistance *multiplied* by ratio T_{period}/T_{on}**

Resistor multiplication allows a large RC time constant to be implemented with smaller area

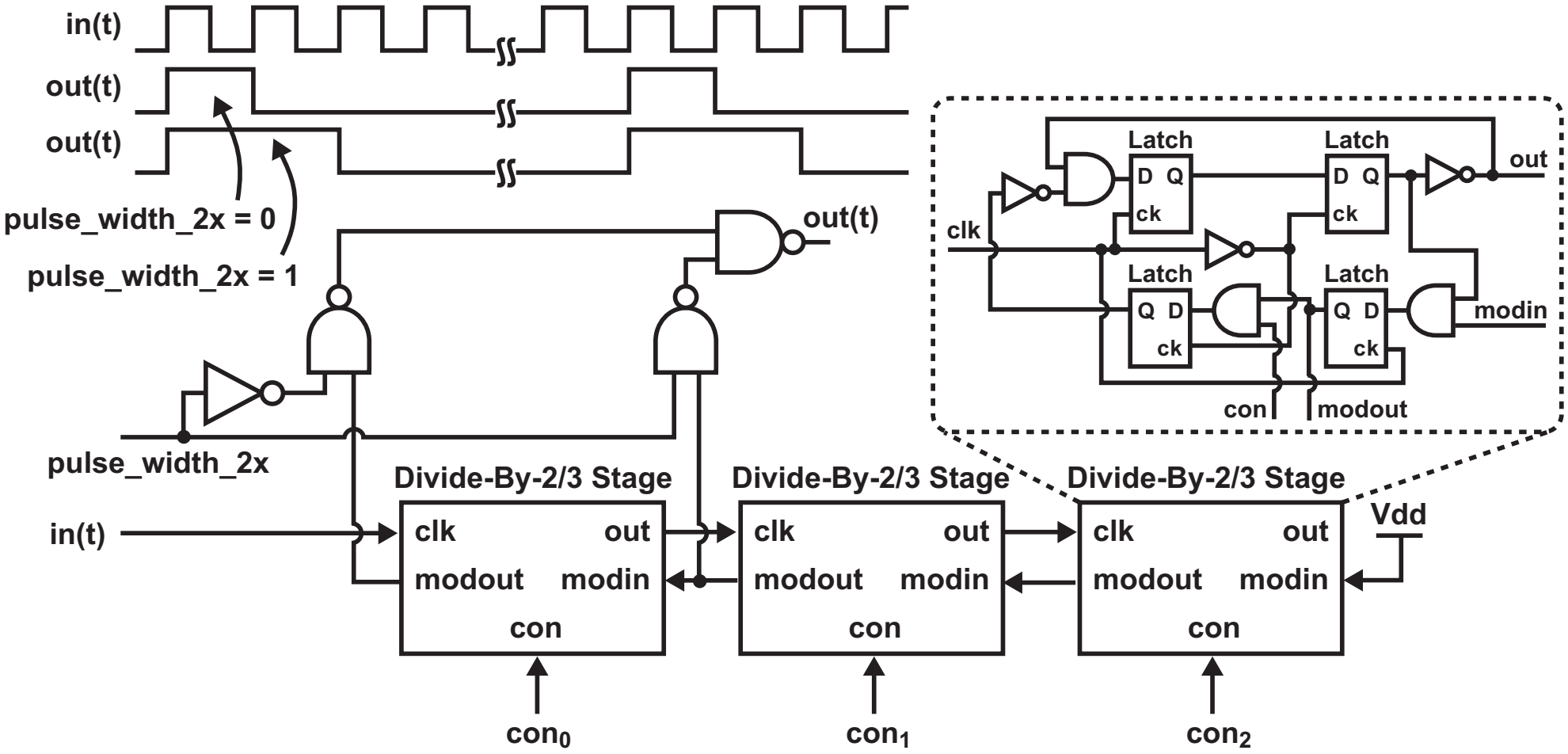
Parasitic Capacitance Reduces Effective Resistance



- Parasitic capacitance stores charge during the pulse "On" time
  - Leads to non-zero current through resistor during pulse Off time
  - Effective resistance reduced

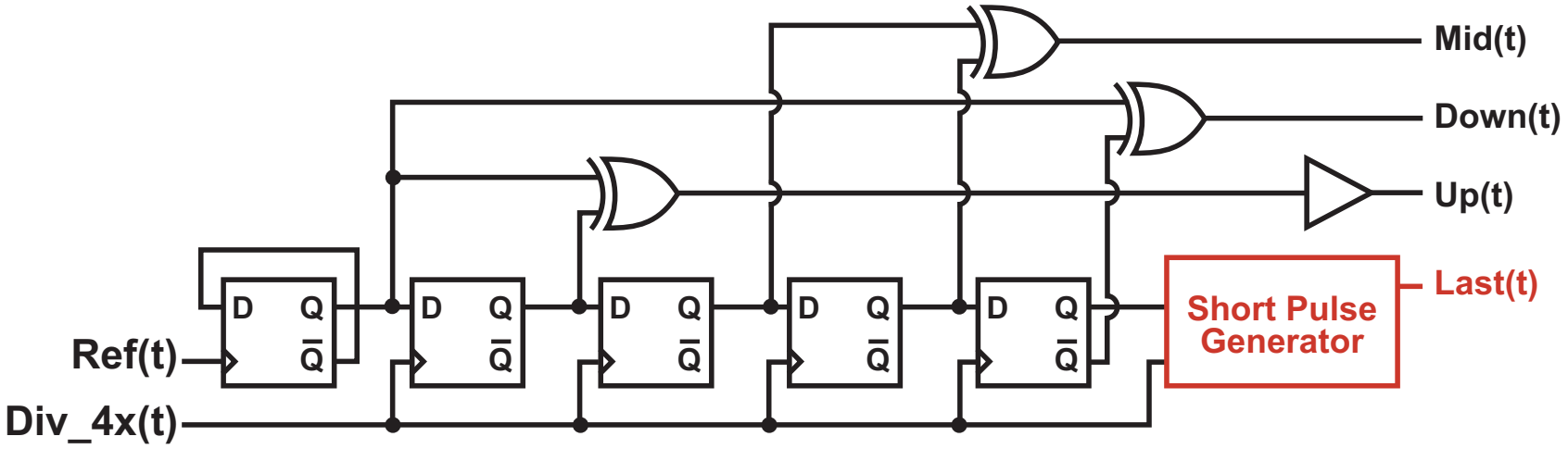
Spice simulation and measured results reveal that >10X resistor multiplication can easily be achieved

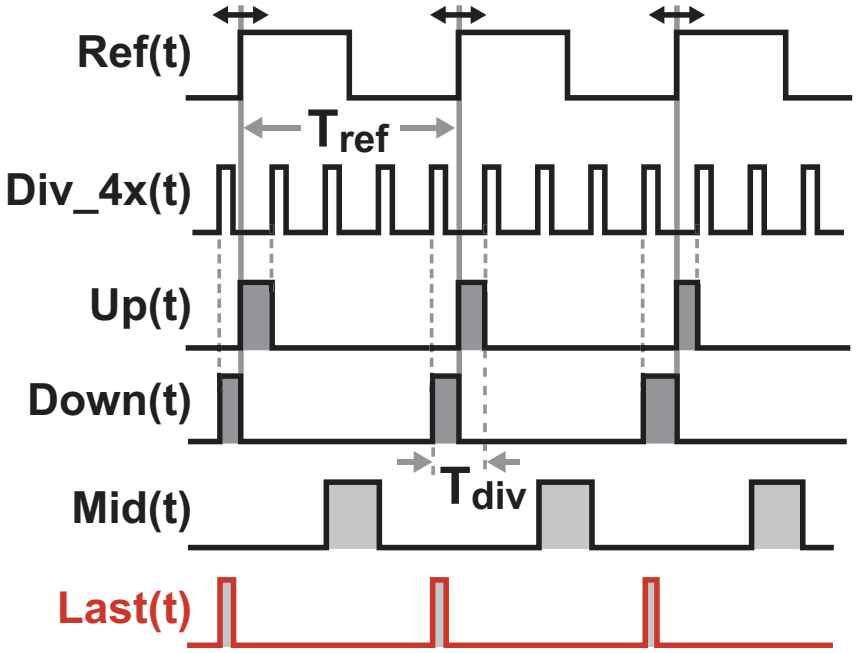
Multi-Modulus Divider Allows Short Pulse Generation



- Creates well controlled pulse widths corresponding to multiples of the period of its high speed input
  - Standard circuit used in many fractional-N PLL structures
  - Pulse width can be changed by tapping off different stages

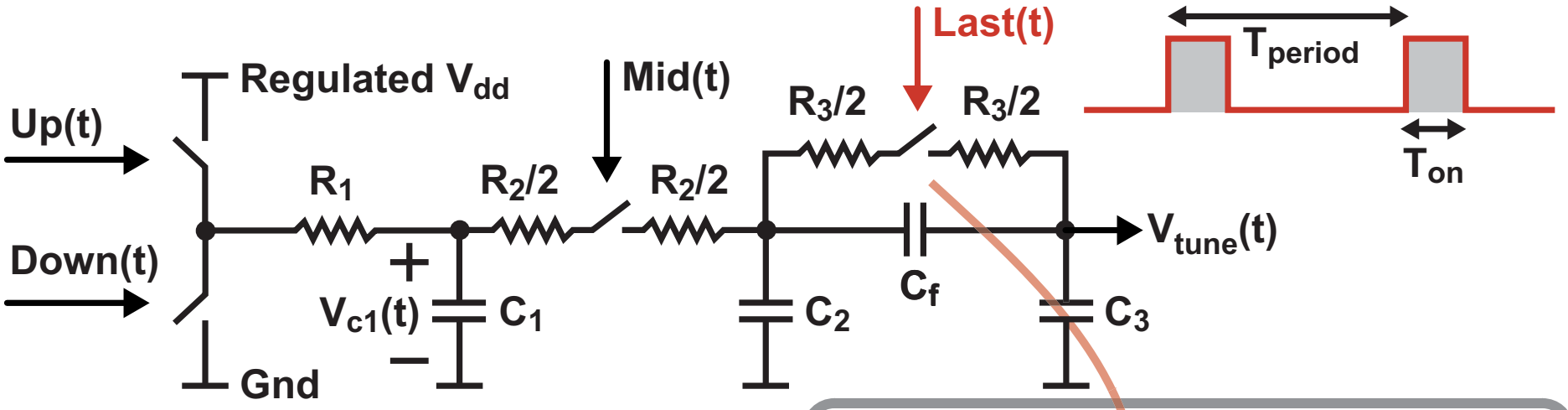
Utilize Short Pulses from Divider in the High Gain PD



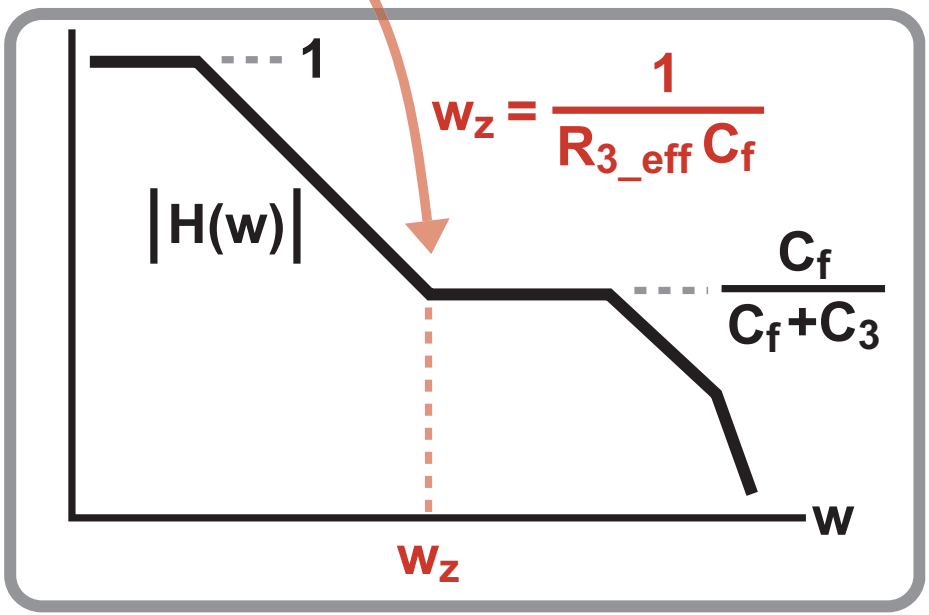


- Short pulses from divider output are used to clock the PD registers
- PD state is used to gate divider output every 4 cycles to form Last pulse
  - Lower pulse frequencies can also be implemented

Switched Resistor Achieves PLL Zero with Low Area

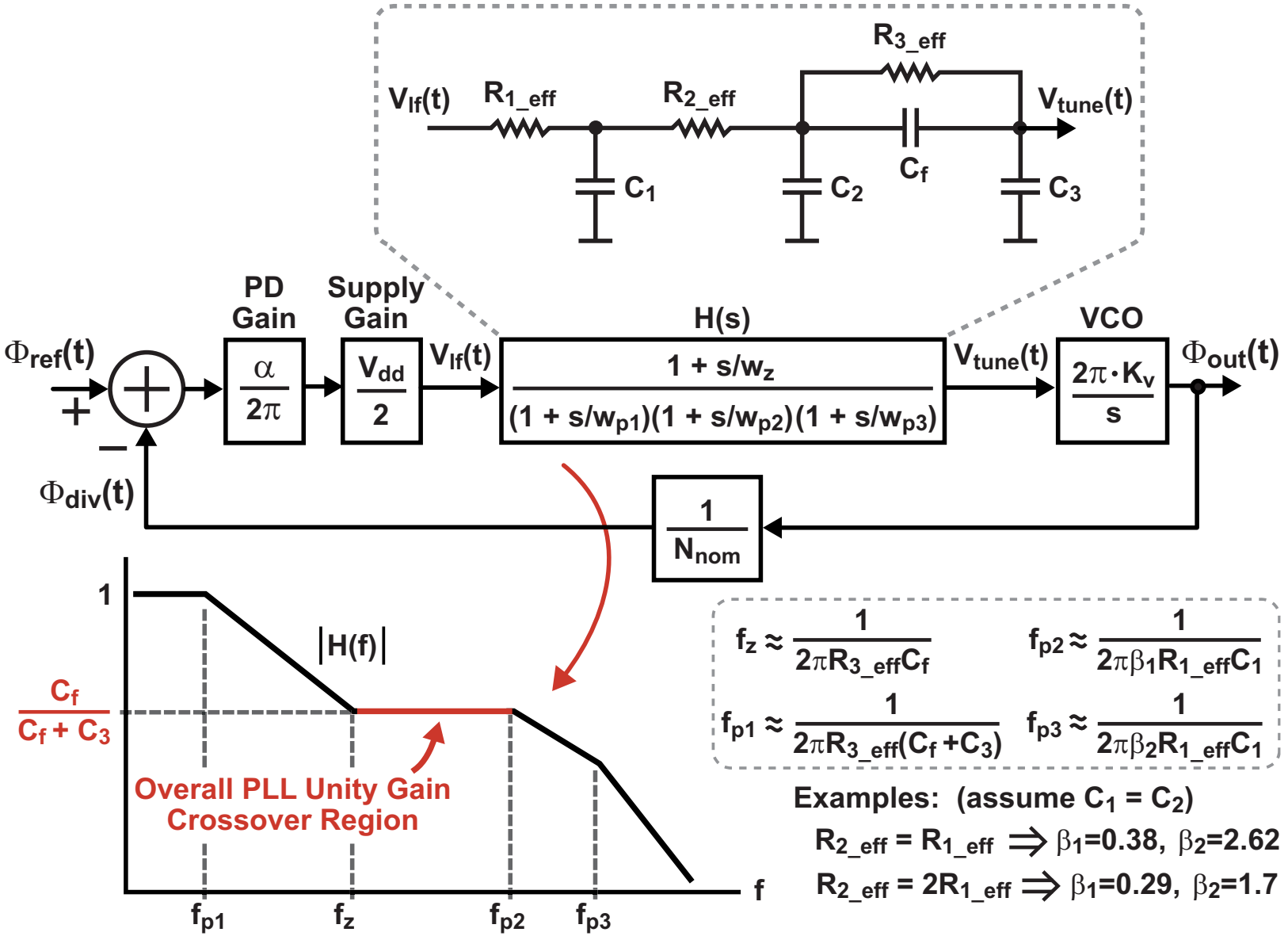


- For robust stability, PLL zero should be set << PLL BW
  - Example: PLL BW = 30kHz
  - Assume desired w_z = 4 kHz
  - Set C_f = 2.5pF (for low area)
  - Required R_{3_eff} = 16 MegaOhms
    - Large area



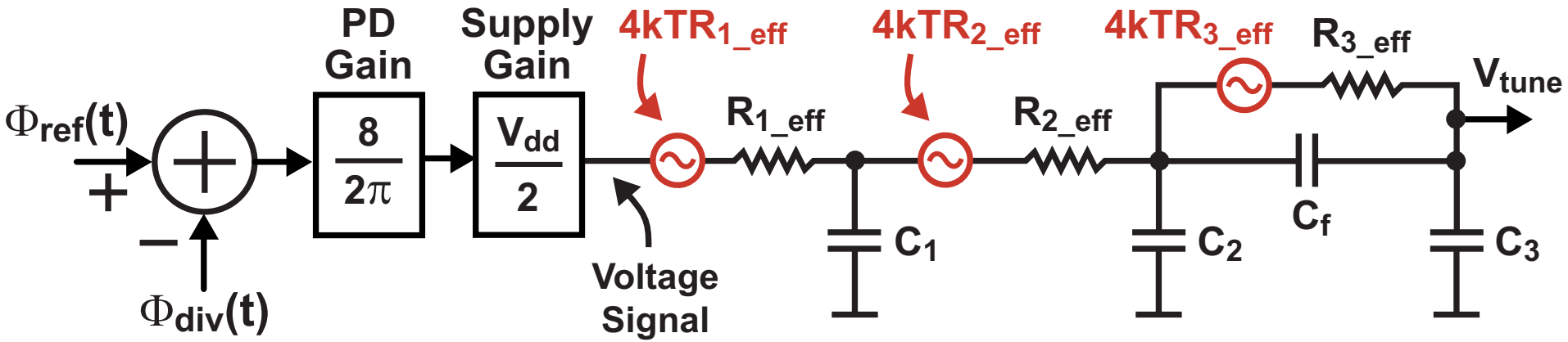
Example: Proper choice of T_{on} and T_{period} allows R_{3_eff} = 16 MegaOhms to be achieved with R_3 = 500 kOhms!

Overall Design of Loop Filter



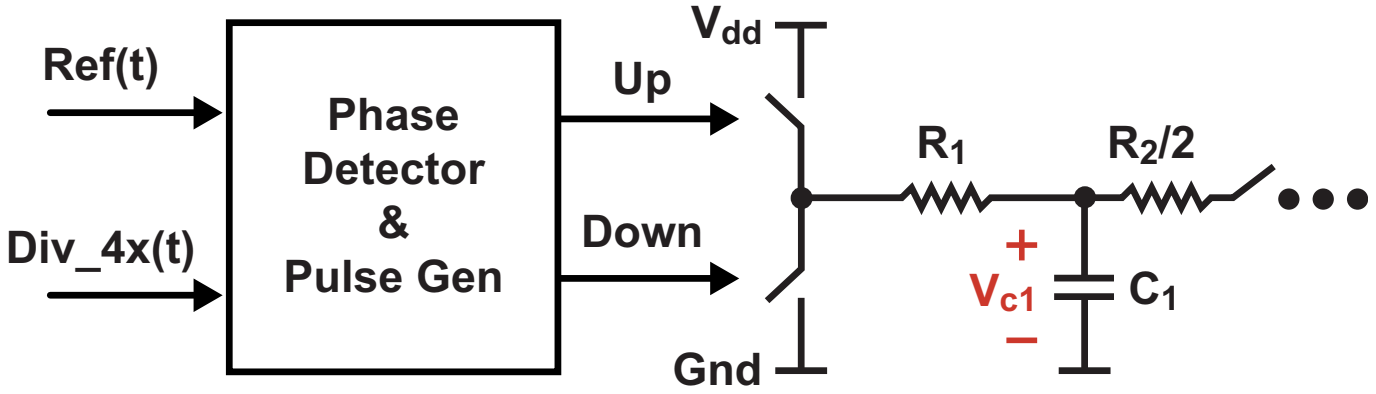
- Apply standard transfer function analysis to achieve desired PLL bandwidth and phase margin

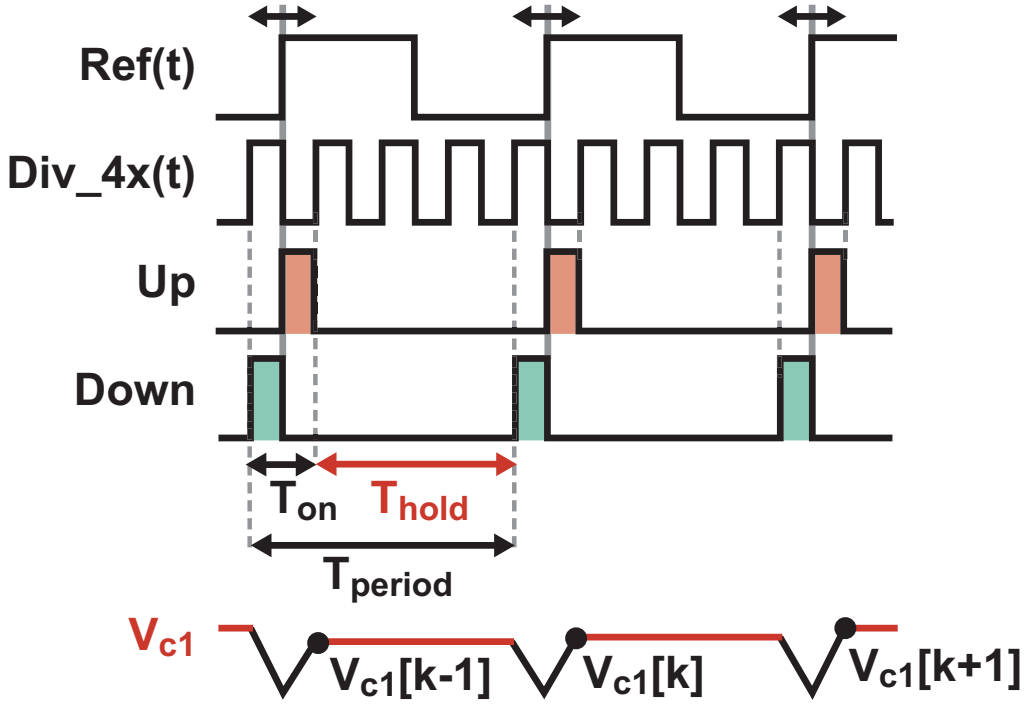
Noise Analysis (Ignore Parasitic Capacitance of Resistors)



- **Assumption: switched resistor time constants are much longer than "on time" of switches**
  - **Single-sided voltage noise contributed by each resistor is simply modeled as $4kTR_{eff}$ (same as for a resistor of the equivalent value)**
- **Note: if switched resistor time constants are shorter than "on time" of switches**
  - **Resistors contribute kT/C noise instead of $4kTR_{eff}$**
  - **We would not want to operate switched resistor filter in this domain since time constants would not be boosted**

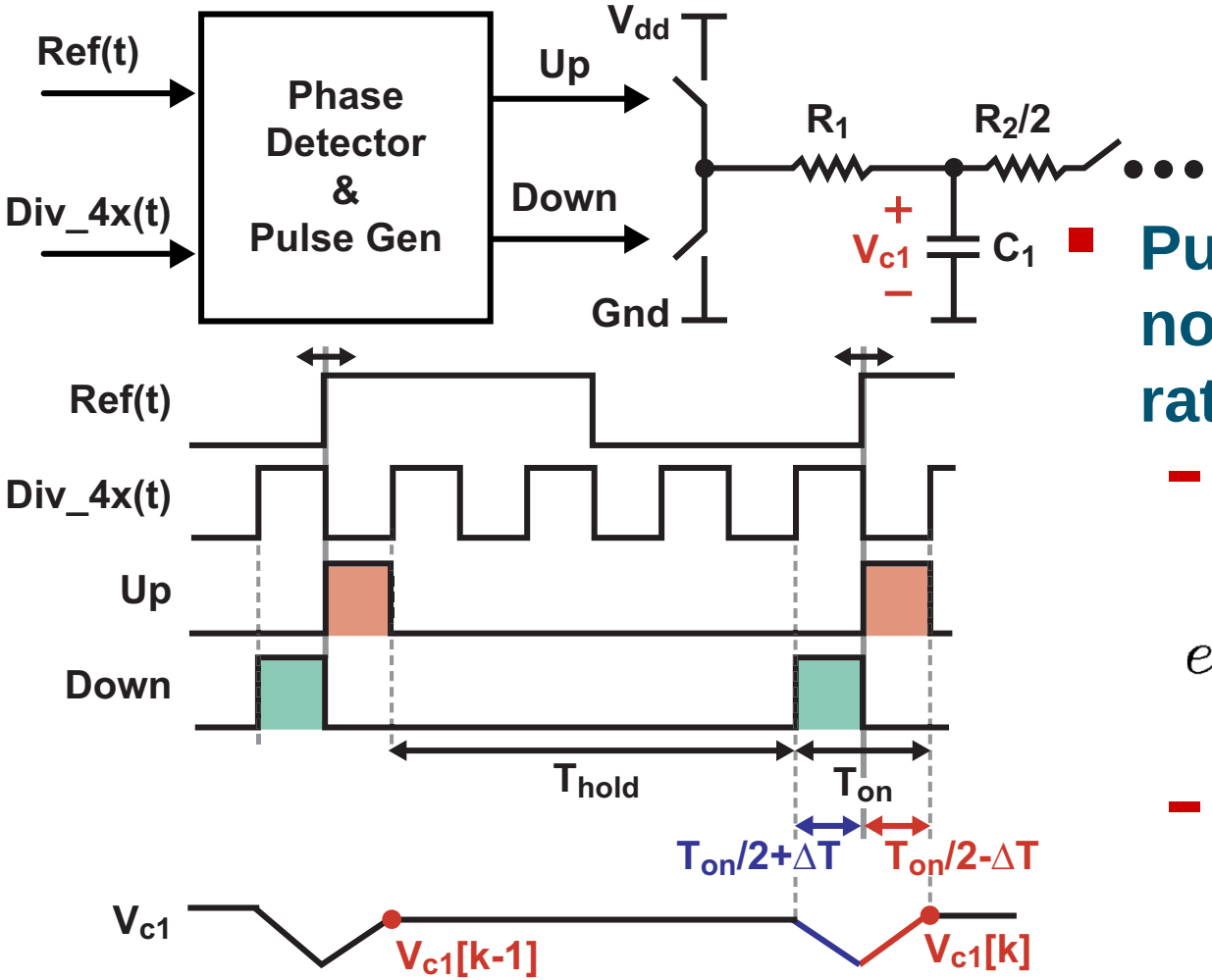
Issue: Nonlinearity in Switched Resistor Loop Filter





- Nonlinearity is caused by
  - Exponential response of RC filter to pulse width modulation
  - Variation of T_{hold} due to Sigma-Delta dithering of divide value
- Note: to avoid additional nonlinearity, design divide value control logic to keep T_{on} a constant value

Nonlinearity Due to Pulse Width Modulation



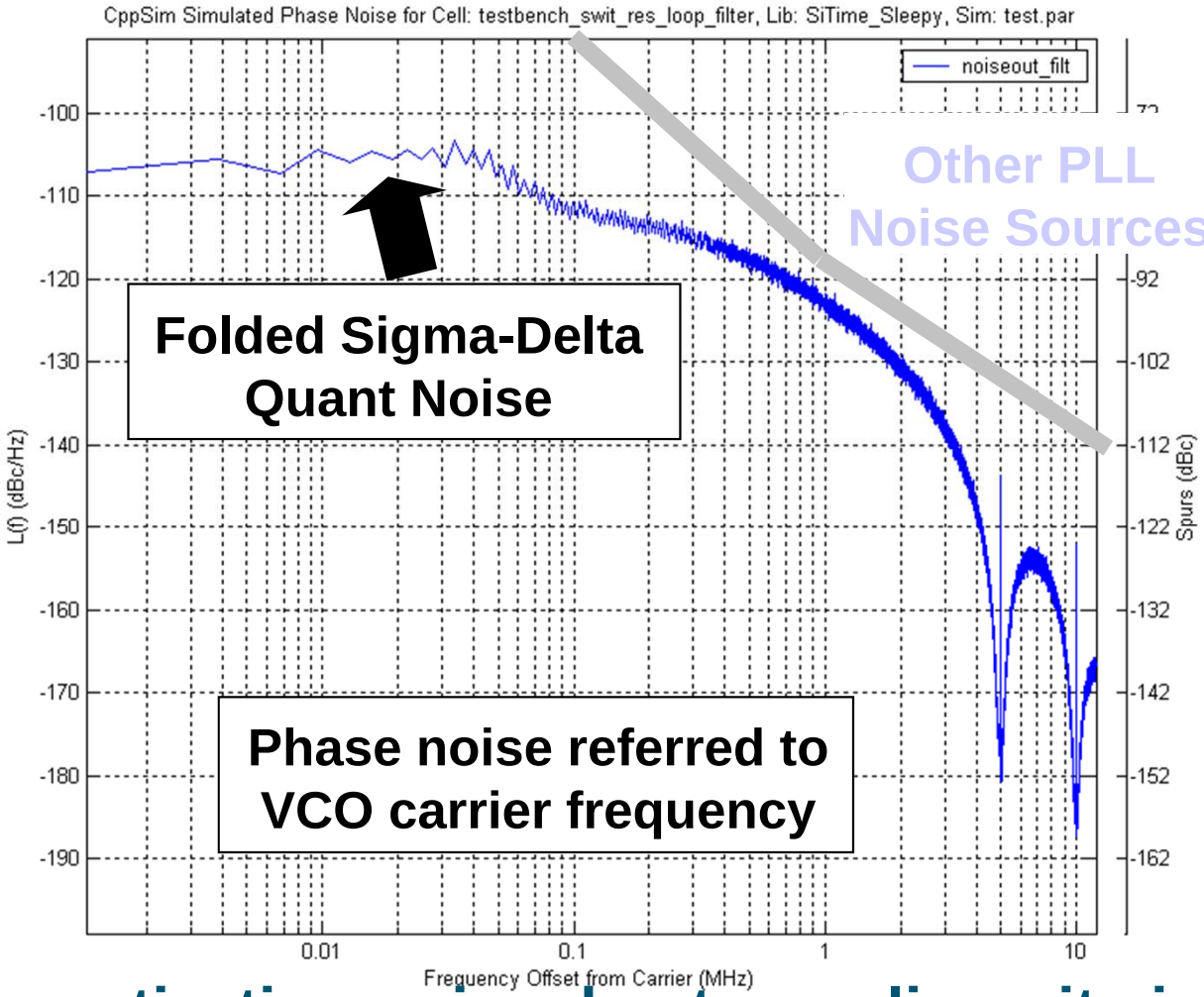
- **Pulse width modulation nonlinearity is reduced as ratio $\Delta T/(R_1C_1)$ is reduced**
  - **If $\Delta T/(R_1C_1)$ is small:**

$$e^{\frac{1}{R_1C_1}\Delta T} \approx 1 + \frac{\Delta T}{R_1C_1}$$

  - **This implies nonlinearity is reduced with lower PLL bandwidth**

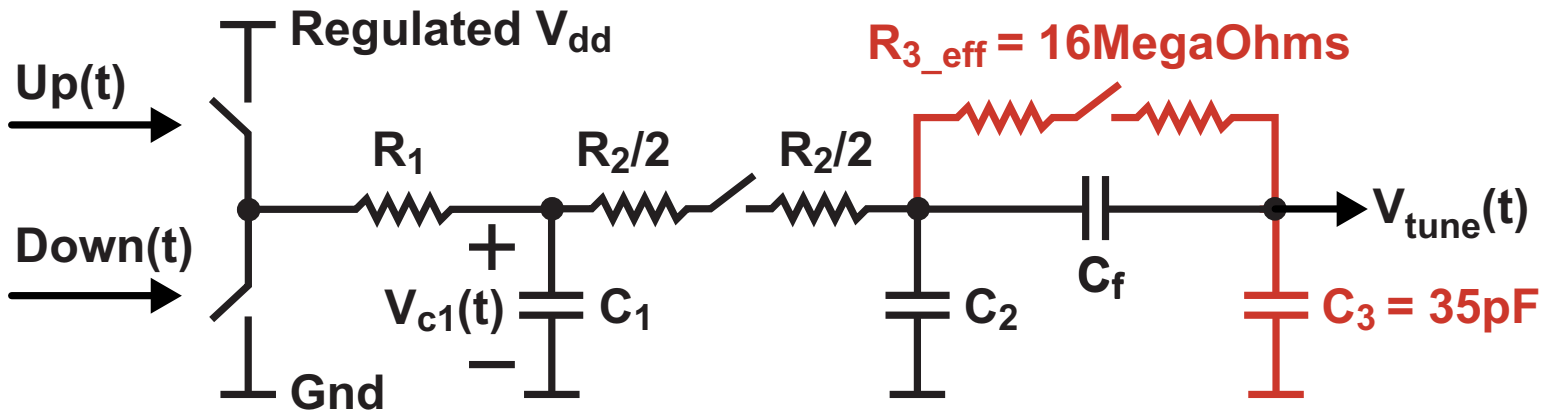
$$V_{c1}[k] = -V_{dd}e^{-\frac{1}{R_1C_1}\frac{T_{div}}{2}}e^{\frac{1}{R_1C_1}\Delta T} + e^{-\frac{T_{div}}{R_1C_1}}V_{c1}[k-1] + V_{dd}$$

Key Design Issue: Folded Noise versus Other Noise



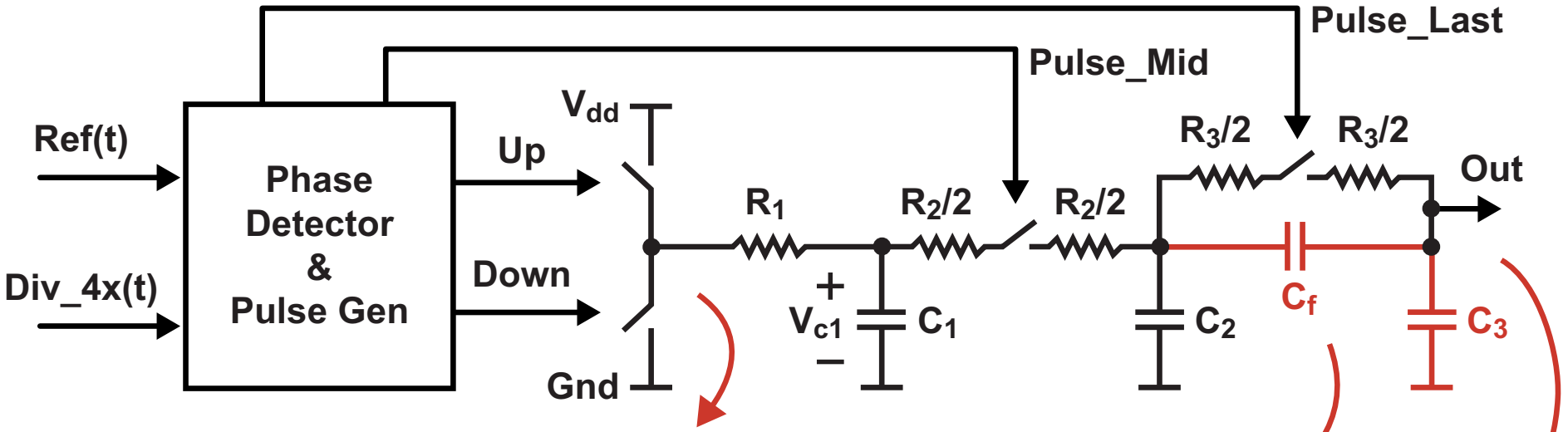
- Folded quantization noise due to nonlinearity is reasonably below other noise sources for this example
  - However, could be an issue for wide bandwidth PLLs
- Use (CppSim) behavioral simulation to evaluate this issue

The Issue of Initial Frequency Acquisition

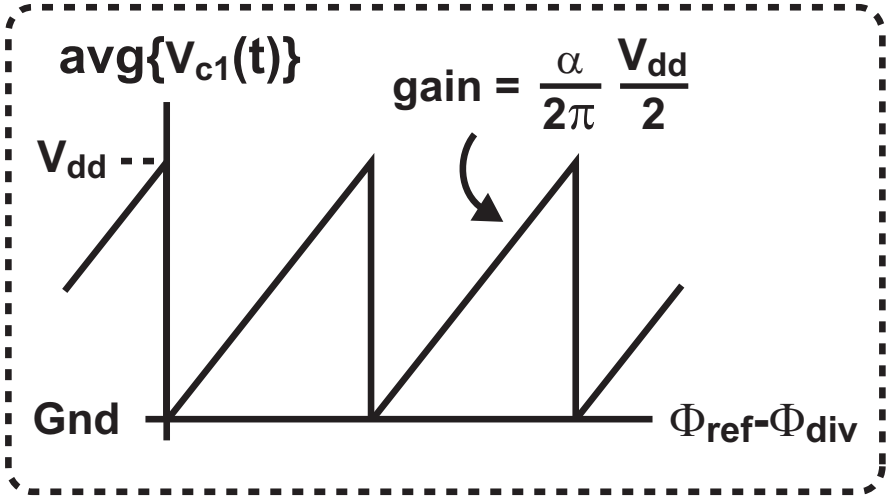


- During initial frequency acquisition, $V_{tune}(t)$ must be charged to proper bias point
  - Following through on previous example:
    - Large 16 MegaOhm resistance of R_{3_eff} prevents fast settling of the voltage across C_3

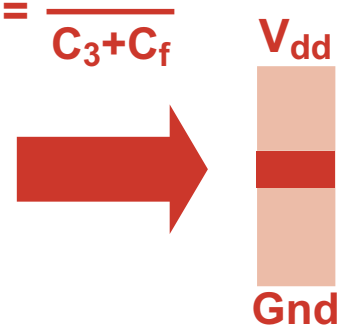
Capacitive Divider Sets Instantaneous Voltage Range



Phase Detector and Supply Gain Characteristic



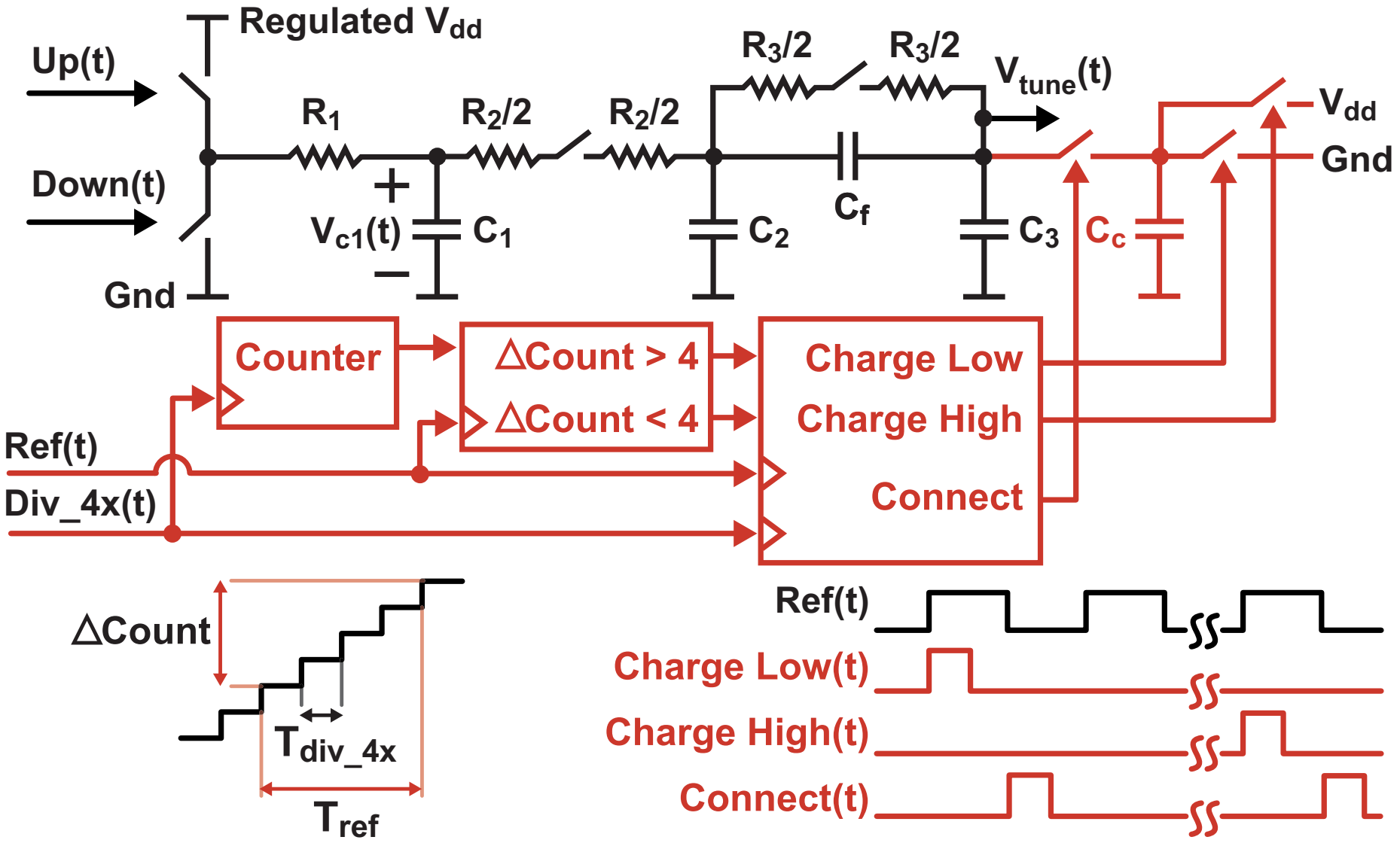
AC Gain $= \frac{C_f}{C_3+C_f}$



Instantaneous Out range $= V_{dd} \frac{C_f}{C_3+C_f}$

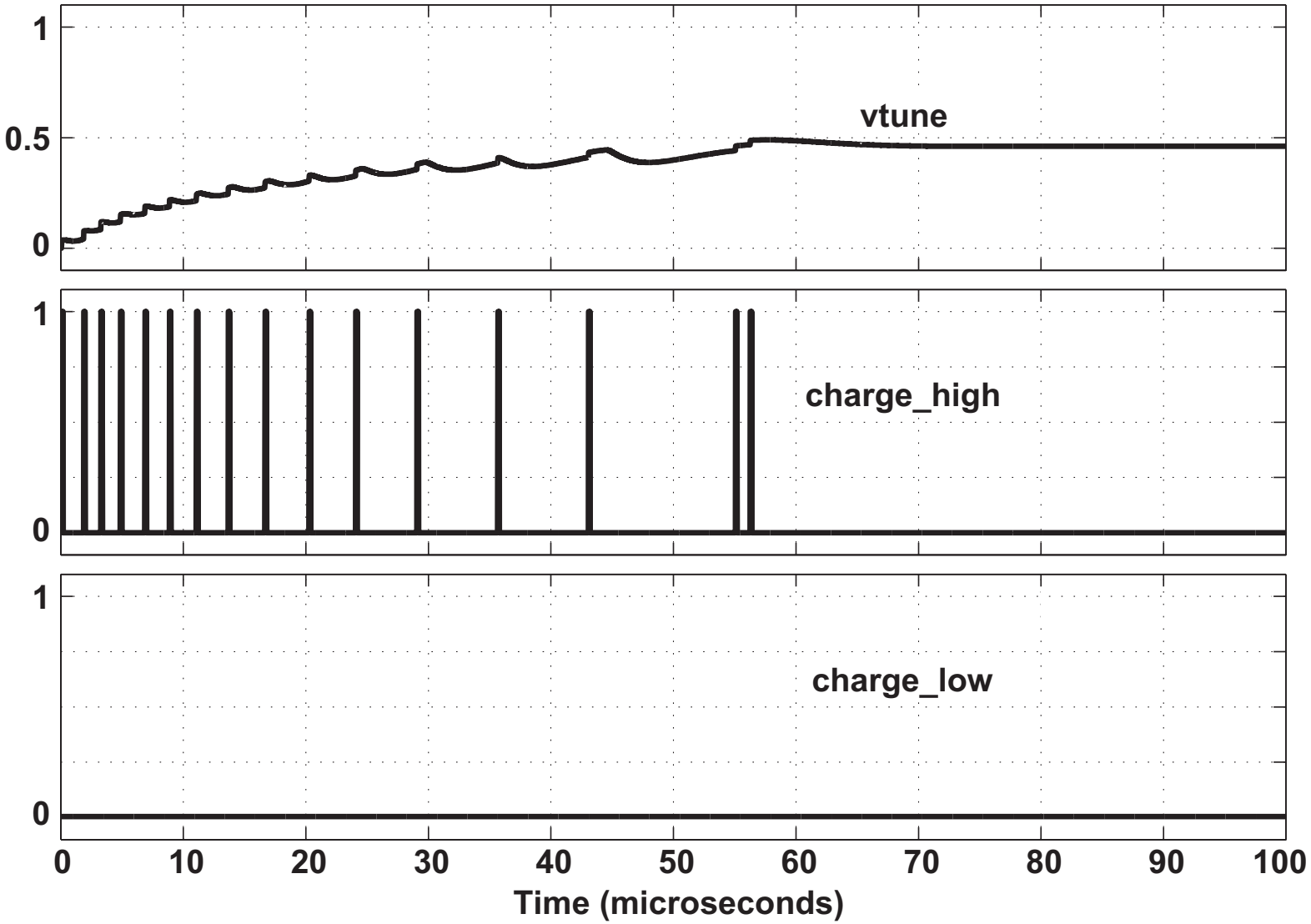
How do we quickly charge capacitor C_3 to its correct DC operating point during initial frequency acquisition?

Utilize Switched Capacitor Charging Technique



- Charge C_3 high or low only when frequency error is detected
  - No steady-state noise penalty, minimal power consumption

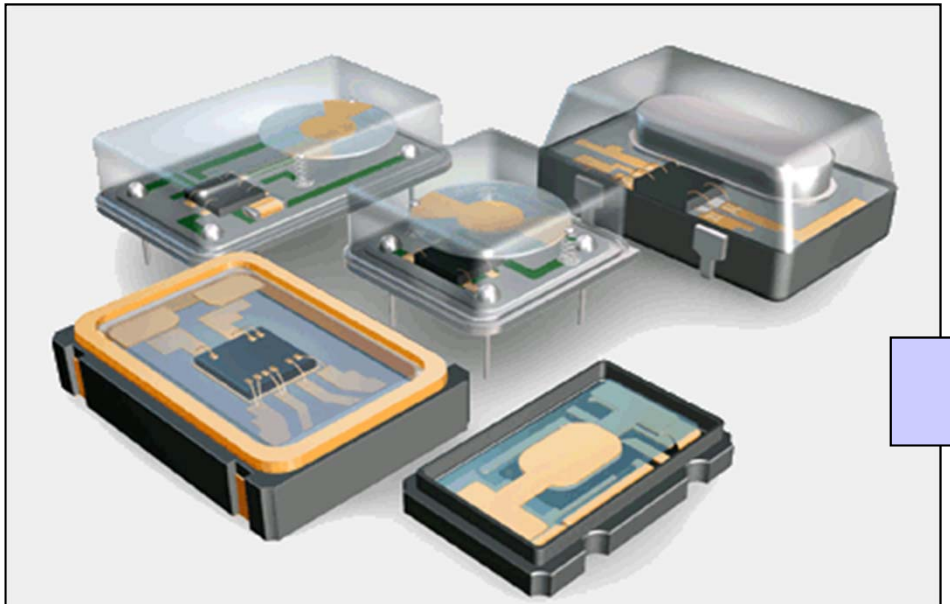
CppSim Behavioral Simulation of Frequency Locking



Switched capacitor technique allows relatively fast frequency locking

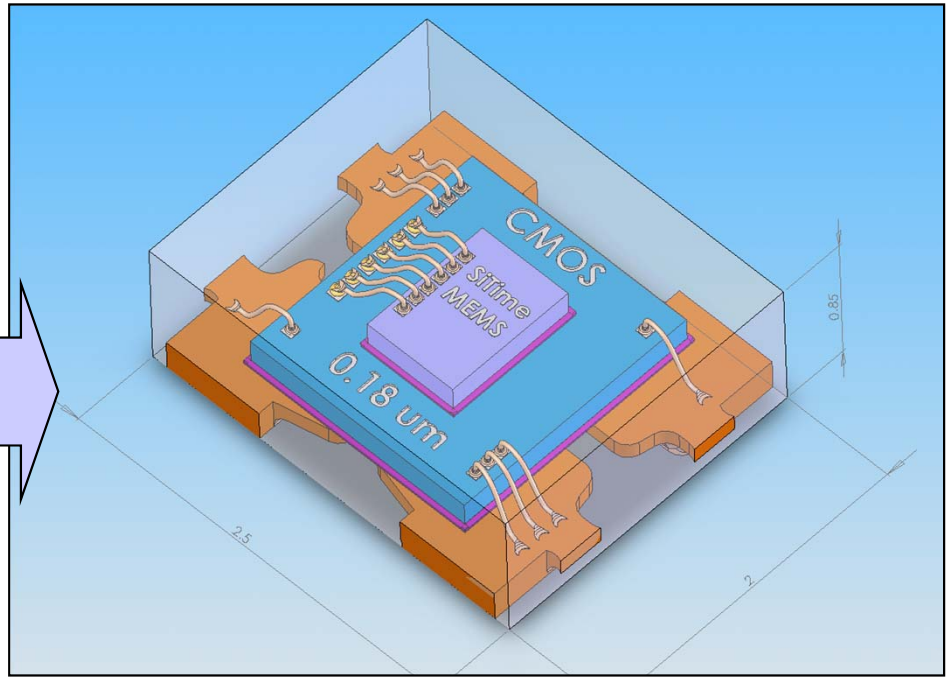
PLL Application: A MEMS-based Programmable Oscillator

Quartz Oscillators



source: www.ecliptek.com

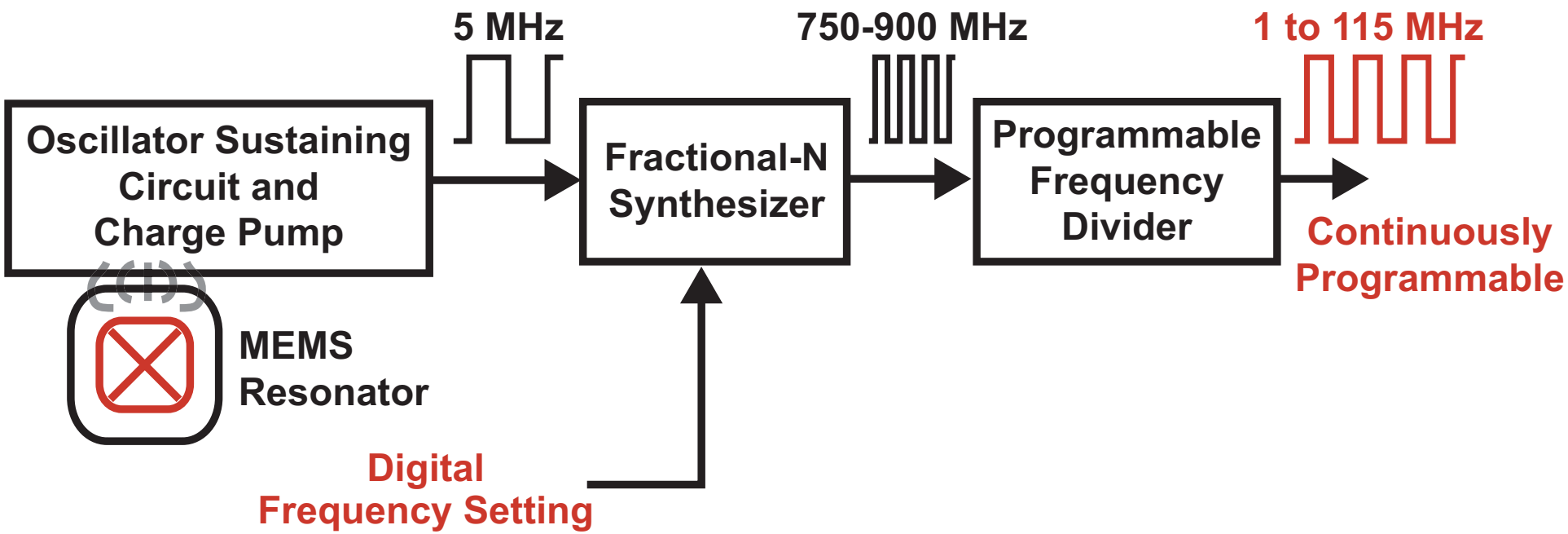
MEMS-based Oscillator



- A part for each frequency and non-plastic packaging
  - Non-typical frequencies require long lead times
- Same part for all frequencies and plastic packaging
  - Pick any frequency you want without extra lead time

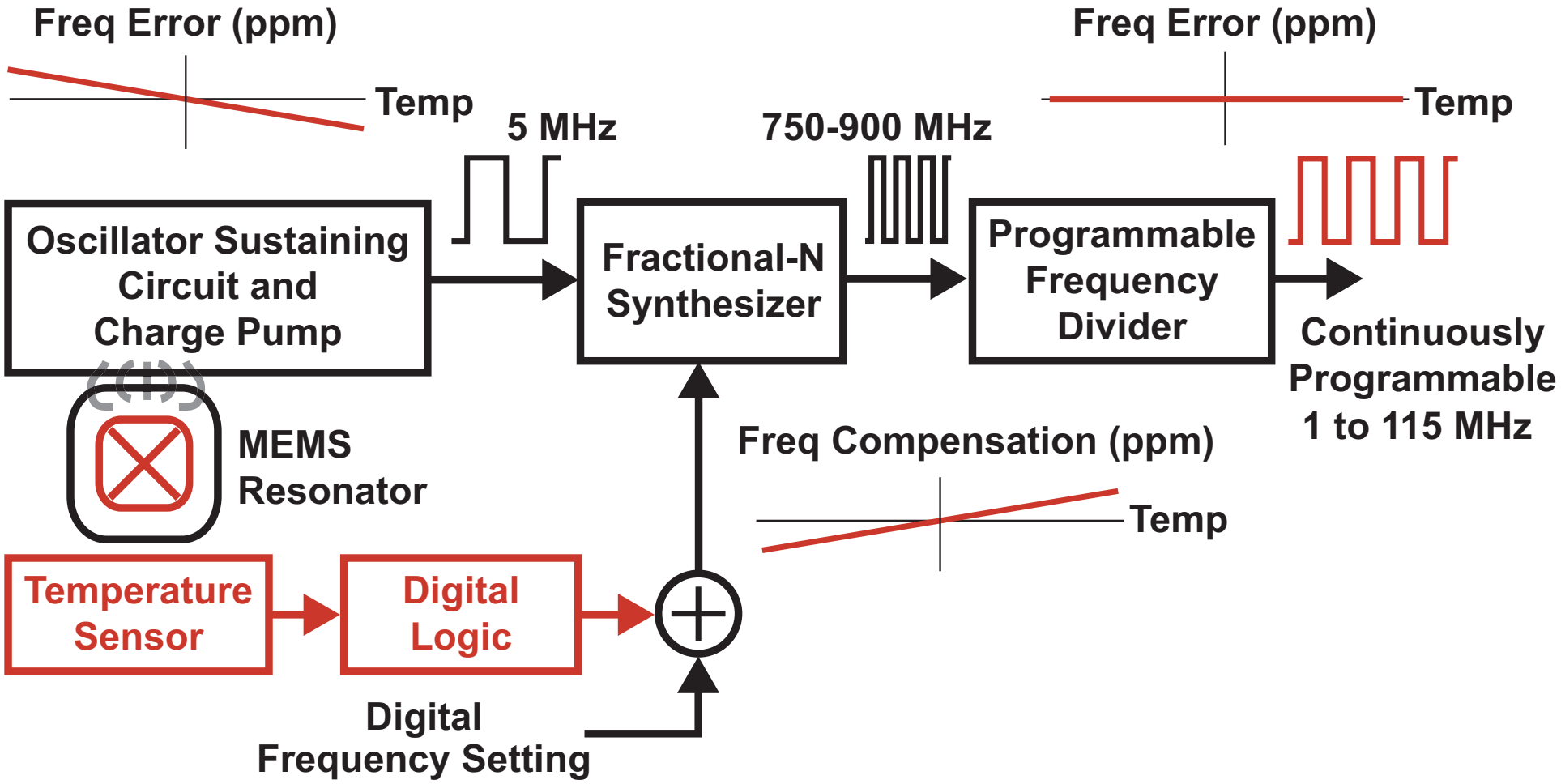
We can achieve high volumes at low cost using IC fabrication

Architecture of MEMS-Based Programmable Oscillator



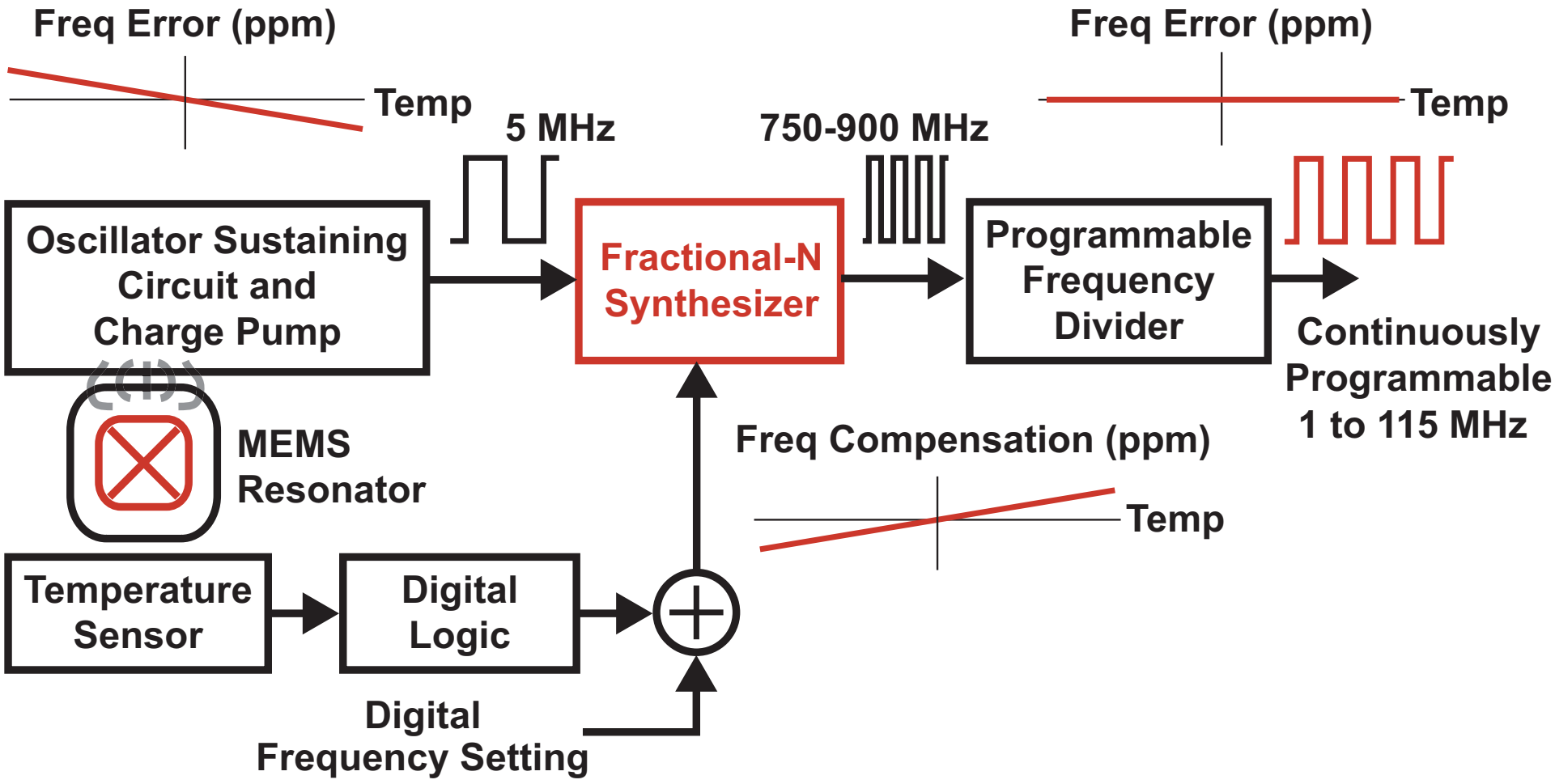
- MEMS device provides high Q resonance at 5 MHz
  - CMOS circuits provide DC bias and sustaining amplifier
- Fractional-N synthesizer multiplies 5 MHz MEMS reference to a programmable range of 750 to 900 MHz
- Programmable frequency divider enables 1 to 115 MHz output

Compensation of Temperature Variation



- High resolution control of fractional-N synthesizer allows simple method of compensating for MEMS frequency variation with temperature
  - Simply add temperature sensor and digital compensation logic

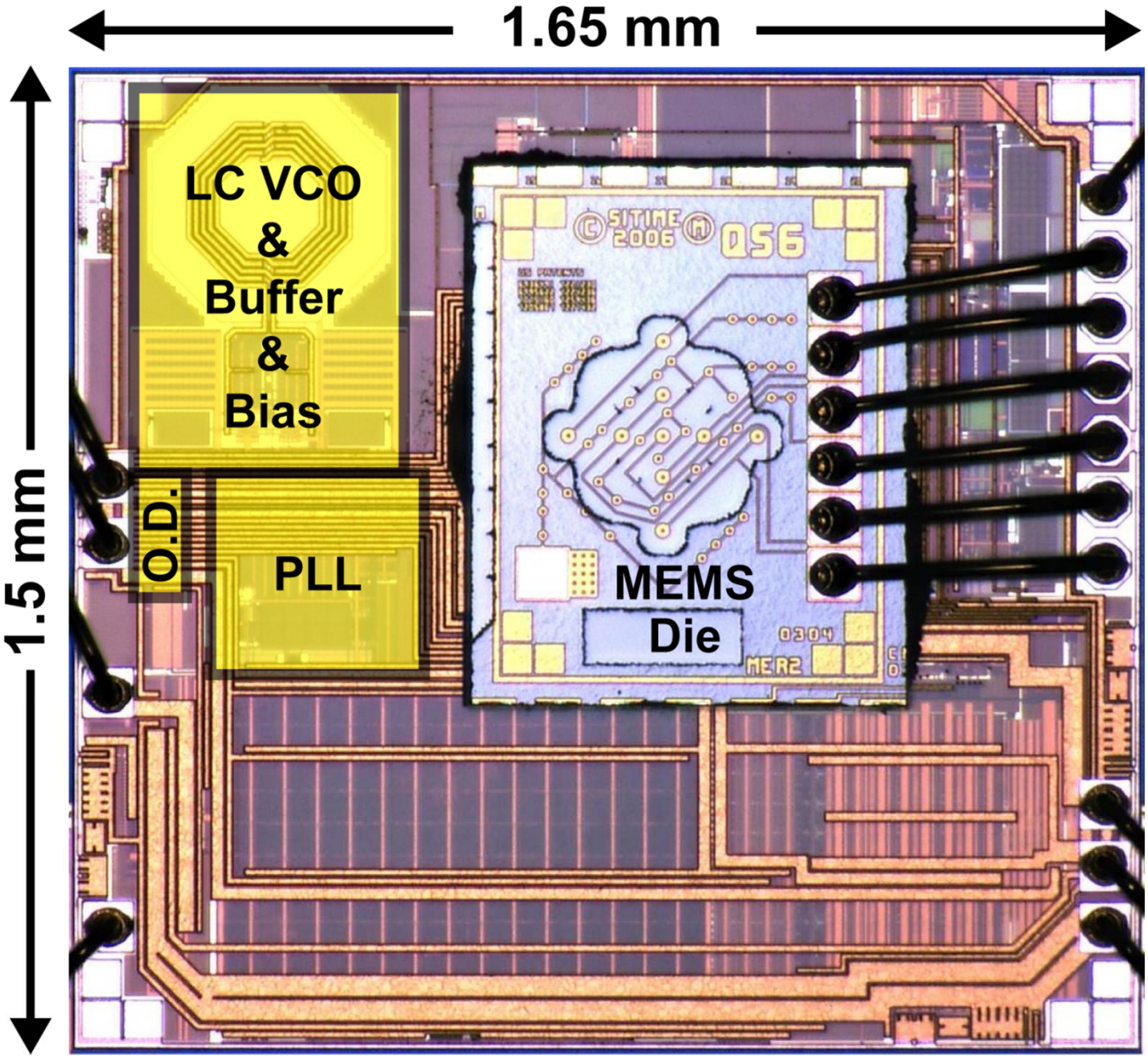
Why Use An Alternative Fractional-N PLL Structure?



Want to achieve low area, low power, and low design complexity

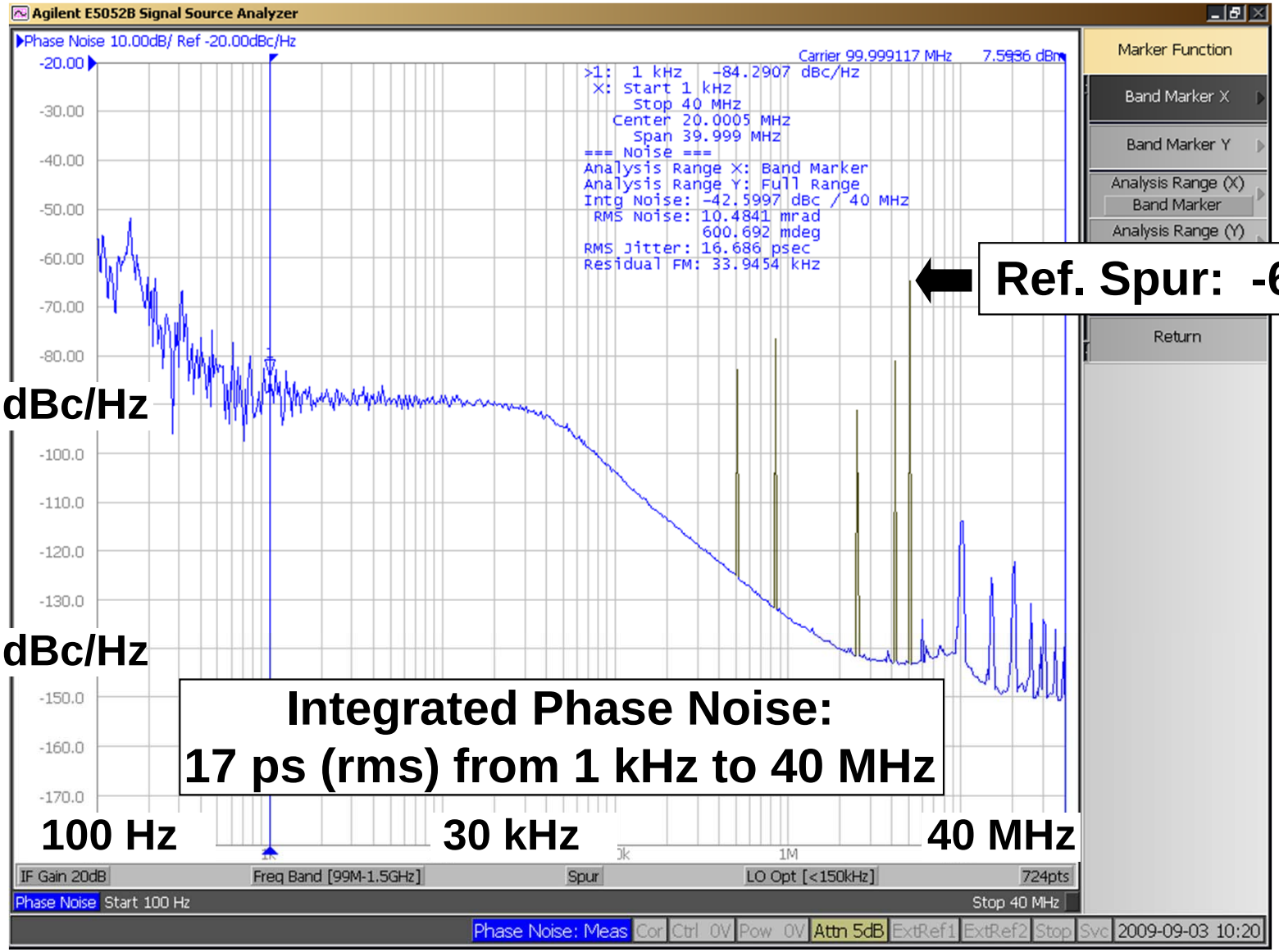
Switched resistor PLL provides a nice solution for this application space

CMOS and MEMS Die Photos Show Low Area of PLL



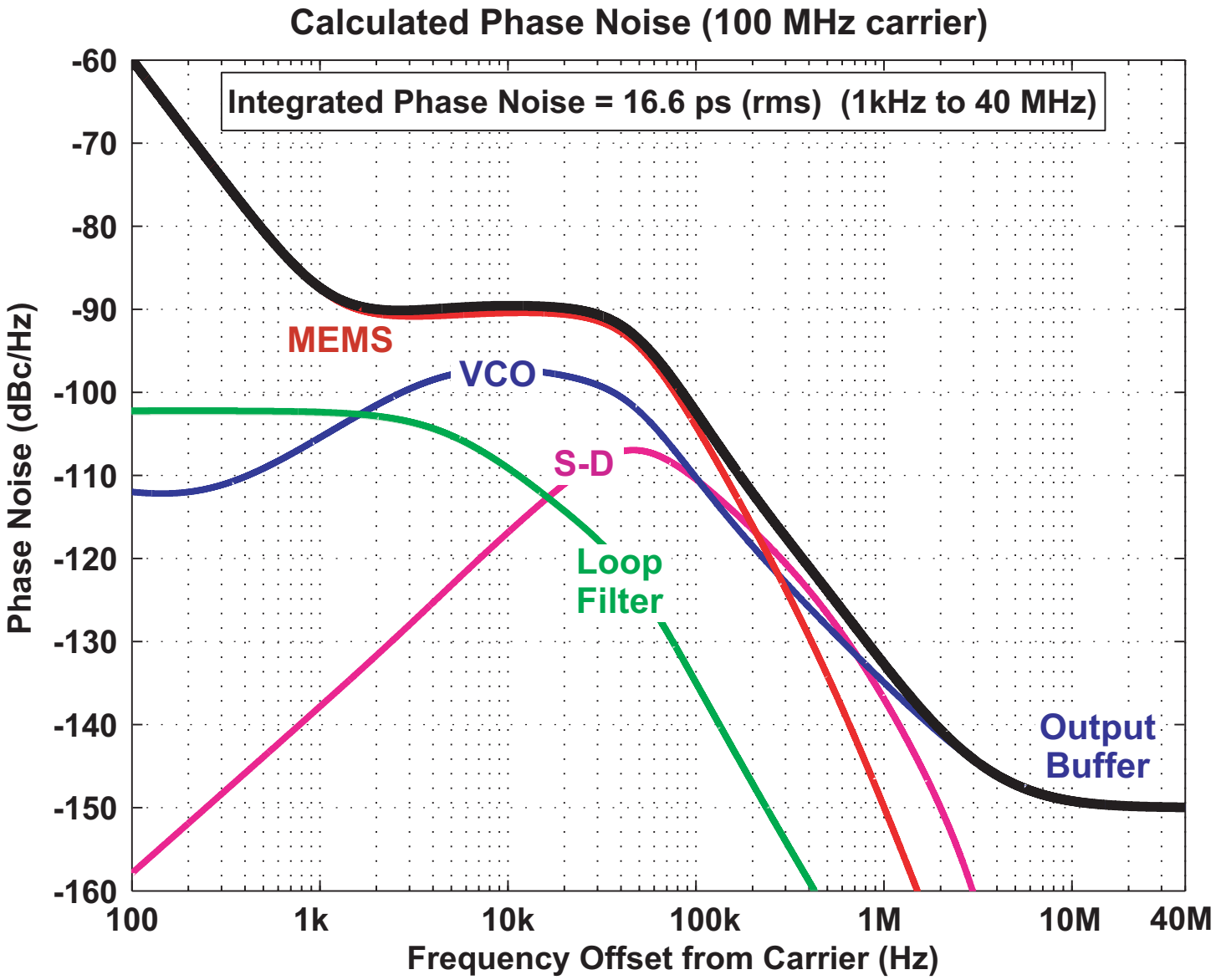
- Active area:
  - VCO & buffer & bias: 0.25mm^2
  - PLL (PFD, Loop Filter, divider): 0.09 mm^2
  - Output divider: 0.02 mm^2
- External supply
  - 1.8/3.3V
- Current (20 MHz output, no load)
  - ALL: 3.2/3.7mA
  - VCO: 1.3mA
  - PLL & Output Divider: 0.7mA

Measured Phase Noise (100 MHz output)



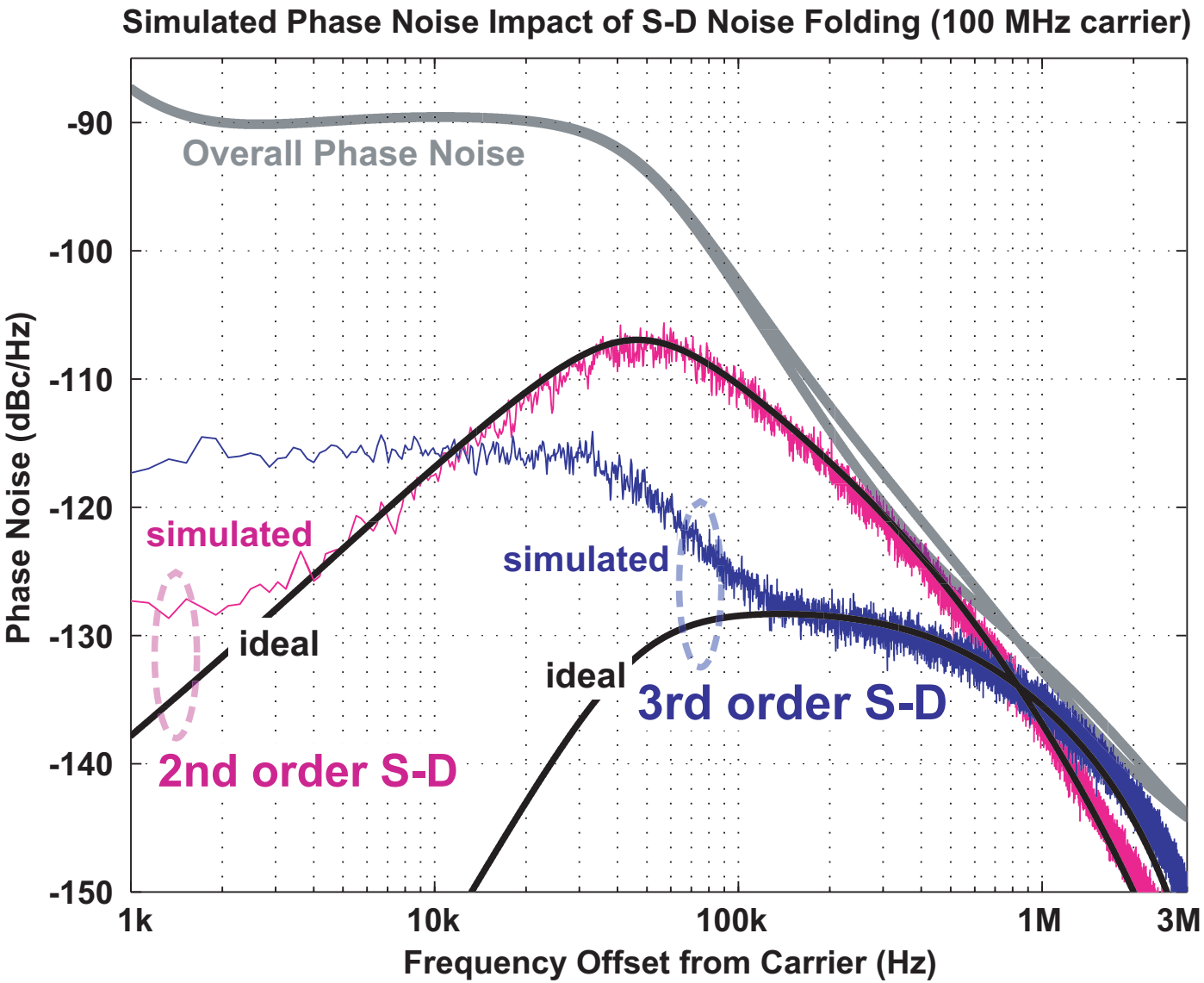
- Suitable for most serial applications, embedded systems and FPGAs, audio, USB 1.1 and 2.0, cameras, TVs, etc.

Calculated Phase Noise Profile of Overall PLL



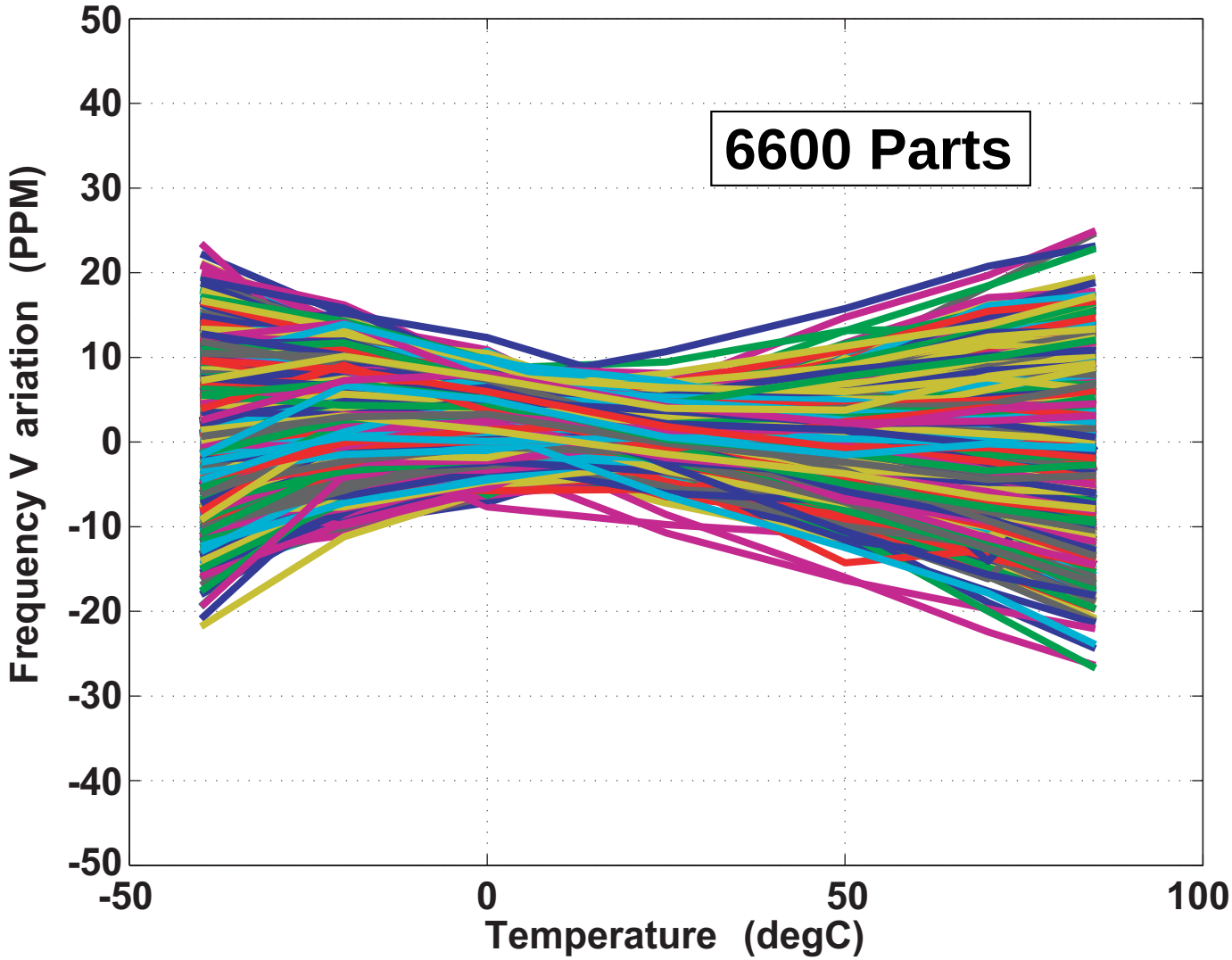
- Note that loop filter noise is well below other PLL noise sources

Simulated Impact of Switched Resistor Nonlinearity



- Noise folding below other PLL noise sources
  - More significant for third order Sigma-Delta

Frequency Variation After Single-Temperature Calibration



< +/-30 ppm across industrial temperature range with single-temperature calibration

Conclusion

- We took a closer look at the classical charge pump PLL
  - Very versatile structure
  - Requires a fair amount of analog design effort
- Alternative PLL structures can provide low area, low power, and reduced analog design effort
  - High gain phase detector lowers impact of loop filter noise
  - Switched resistor technique eliminates the charge pump and reduces area through resistor multiplication
  - Switched capacitor frequency detection enables reasonable frequency acquisition time with no noise penalty

Application specific PLL structures can provide worthwhile benefits over a classical analog PLL structure