11.6 A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator with Better Than ±0.5ppm Frequency Stability

Michael Perrott[1], Jim Salvia[2], Fred Lee[3], Aaron Partridge[2], Shouvik Mukherjee[2], Carl Arft[2], Jin-Tae Kim[2], Niveditha Arumugam[2], Pavan Gupta[2], Sassan Tabatabaei[2], Sudhakar Pamarti[4], Haechang Lee[2], Fari Assaderaghi[2]

[1]Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates,
[2]SiTime, Sunnyvale, CA
[3]Fairchild Semiconductor, San Jose, CA
[4]University of California, Los Angeles, Los Angeles, CA

MEMS-based programmable oscillators have emerged as a promising alternative to crystal-based frequency references, with previously reported work demonstrating sub-ps integrated jitter [1]. Here we show frequency stability better than ±0.5ppm from -40 to 85°C, along with Allan Deviation (i.e., long term jitter) better than 0.005 ppm for 0.1, 1, and 10 second strides. Since the MEMS resonator has a well-defined temperature dependence, the key to this performance is a stable and low-noise temperature-to-digital converter (TDC) that utilizes a thermistor on the same die as the MEMS resonator.

Figure 11.6.1 illustrates our programmable oscillator. It consists of a MEMS resonator die which is wire bonded to a 0.18µm CMOS die that includes an oscillator sustaining circuit, TDC, fractional-N synthesizer, and digital logic [1]. Placement of a thermistor on the MEMS die allows excellent tracking of temperature-induced fluctuations of the MEMS resonator frequency, F_{res}. Compensation of nonlinear temperature dependence of the thermistor resistance and F_{res} is achieved with on-chip digital 5th-order polynomial correction. Since F_{res} varies by approximately -31ppm/K, it is challenging to obtain ±0.5ppm frequency stability from -40 to 85°C. The current state of the art is ±10ppm frequency stability for temperature compensated (non-ovenized) MEMS oscillators [4]. Further, noise lower than 0.16mK (rms) in a 5Hz bandwidth (i.e., 10S/s) is required to achieve Allan Deviation less than 0.005ppm at 0.1 second stride – a challenging requirement given the current state of the art of 2mK at 1S/s [2], 15mK at 10 S/s [3] and 40mK at 32 S/s [4].

The TDC's front-end circuit, shown in Fig. 11.6.2, consists of a resistive bridge that is balanced by digitally tuning a reference resistor, R_{ref}, to match the thermistor's resistance, R_{MEMS}. Comparison of R_{ref} and R_{MEMS} is achieved by using a CMOS switch to periodically short them together at frequency f_{chop} (25kHz), and then amplifying the sum of the two voltages, $V_R(t)$ and $V_C(t)$, to yield an output voltage, $V_{amp}(t)$. As shown in Fig. 11.6.2, $V_R(t)$ and $V_C(t)$ move in opposite directions, and, regardless of the small resistance of the shorting switch, will have equal changes in magnitude only when R_{ref} and R_{MEMS} are equal in value (assuming well matched C_{ac} capacitors). As such, sampling the change in $V_{amp}(t)$ between each phase of f_{chop}, $V_{avg1}[k]$ -$V_{avg2}[k]$, provides an accurate error signal for tuning R_{ref} to match R_{MEMS}. An advantage of this CDS technique is that it rejects the 1/*f* noise and DC offset of the front-end amplifier. Further, the amplifier's DC input biasing can be done in an essentially noise free manner via a feedback resistor, R_f, which is periodically switched into the circuit for brief intervals outside the measurement window of $V_{avg1}[k]$ and $V_{avg2}[k]$.

Figure 11.6.3 reveals that $R_{ref} = T_{clk}/C_2$ is implemented with a switched-capacitor (SC) network, where $f_{clk} = 1/T_{clk}$ is the frequency, in the tens of MHz range, of the non-overlapping clocks $clk_{ph1}(t)$ and $clk_{ph2}(t)$. By digitally varying f_{clk}, the SC reference resistor can be tuned with high resolution. Voltage ripple due to the SC operation is reduced by the C_1 capacitors. Pseudo-differential implementation of the front-end is achieved with only one thermistor by using additional switches controlled by $clk_{chop}(t)$, which suppresses electromigration-induced drift since DC current through the thermistor is nearly zero.

Similar to the pulsed resistor biasing shown in Fig. 11.6.2, Fig. 11.6.3 reveals that a simple voltage regulator to reduce supply noise is achieved for the amplifier by pulse biasing the gate of a native NMOS device. A similar technique is also applied to the current bias source, with R_{bias} reducing the impact of charge injection and C_{bias} being large enough to adequately maintain the voltage bias between pulses. The measurement windows of $V_{amp\_p}(t)$ and $V_{amp\_m}(t)$ are chosen to avoid the intervals during which pulsed biasing occurs as well as the transients due to the transitions of $clk_{chop}(t)$.

A system-level view of the TDC is shown in Fig. 11.6.4. $R_{ref} = T_{clk}/C_2$ is digitally tuned using a fractional-N frequency divider whose nominal divide value, N_{nom}, is set by a 2nd-order digital ΔΣ modulator such that $R_{ref} = T_{clk480} \cdot N_{nom}/C_2$. T_{clk480} is set by an on-chip ring-oscillator clock multiplier that creates a 480MHz clock signal locked to the F_{res} frequency (48MHz). N_{nom} is adjusted by the feedback loop to achieve $V_{avg1}[k] - V_{avg2}[k] = 0$, implying $R_{ref} = R_{MEMS}$ under steady-state conditions. The overall TDC output at steady-state is $N_{nom} = R_{MEMS} \cdot C_2/T_{clk480}$. Since 5th-order polynomial correction is employed, temperature-induced variations in C_2 (implemented as a metal finger capacitor) and T_{clk480} (derived from F_{res}) are acceptable since they do not introduce significant higher-order curvature or cancellation of the temperature-induced variation in R_{MEMS}.

Details of the VCO-based quantizer are shown in Fig. 11.6.5. A pseudo-differential implementation is utilized [5,6] in which two ring oscillators are shifted in opposite directions in frequency as a function of the differential input voltage, $V_{in+} - V_{in-}$. The oscillators' biasing network keeps their total current consumption relatively constant in order to reduce impact on the supply voltage, and small bleeder currents maintain oscillation above 150MHz. In order to sample the phase of the ring oscillator outputs at a relatively low rate of 24MHz, 6b digital counters are inserted between the ring oscillators and the sampling register. The sampling register also includes digital logic to compensate for wrapping effects on the digital counters, and the 1st-order difference transforms the sampled phase of each oscillator into the difference of their frequencies while yielding 1st-order shaped quantization noise. Implementation of the measurement windows of $V_{avg1}[k]$ and $V_{avg2}[k]$ is achieved by the digital averaging block, which simply ignores the output of the VCO-based quantizer outside these measurement windows.

Figure 11.6.7 shows a die photo of the MEMS resonator die (with thermistor) wire-bonded to the 0.18µm CMOS die. Overall measured chip current (48MHz output with no load) is 33mA at 3.3V supply. Measured current consumption for the combined TDC and clock multiplier (including all analog and digital circuits) is 3.93mA, of which 2.8mA is estimated for the analog portion of the TDC and entire clock multiplier (which occupy 0.18mm² combined area), and the remainder for digital blocks. TDC noise in 5Hz bandwidth is <100µK (rms) at 25°C based on measurements taken from the TDC output. Figure 11.6.6(a) shows better than ±0.5ppm stability from -40 to 85°C with frequency compensation consisting solely of the on-chip TDC and digital 5th-order polynomial correction. Figure 11.6.6(b) displays measured output phase noise under several different conditions related to the TDC. Finally, Fig. 11.6.6(c) shows measured Allan Deviation <0.005ppm at room temperature at 0.1, 1, and 10-second strides.

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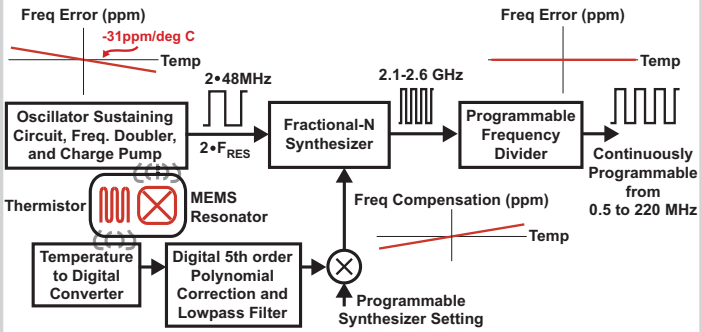

Figure 11.6.1: MEMS-based oscillator circuit consisting of a MEMS die with resonator and thermistor wire-bonded to a CMOS die with sustaining circuit, frequency doubler, fractional-N synthesizer, programmable frequency divider, and temperature compensation circuits.

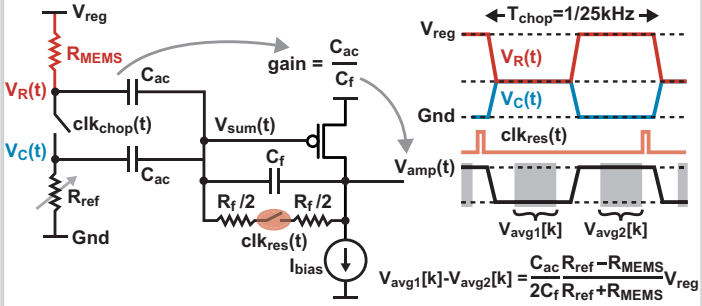

Figure 11.6.2: Simplified view of TDC frontend in which R_{ref} is matched to R_{MEMS} with error sensed using an amplifier with pulsed resistor feedback biasing for reduced noise.

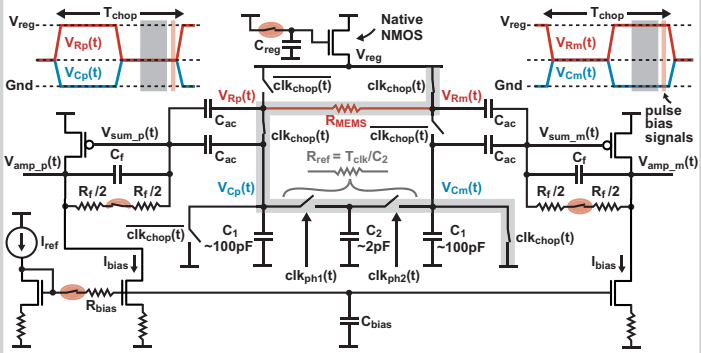

Figure 11.6.3: Detailed view of pseudo-differential TDC frontend showing the switched-capacitor implementation of R_{ref} and the pulsed bias current mirror and voltage regulator for reduced noise.

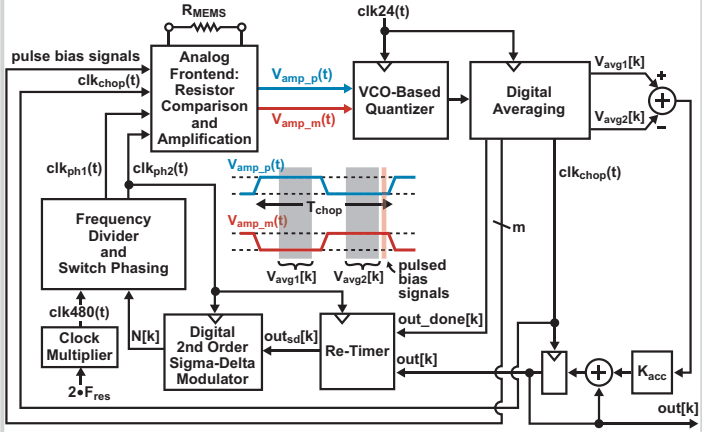

Figure 11.6.4: System-level view of TDC.

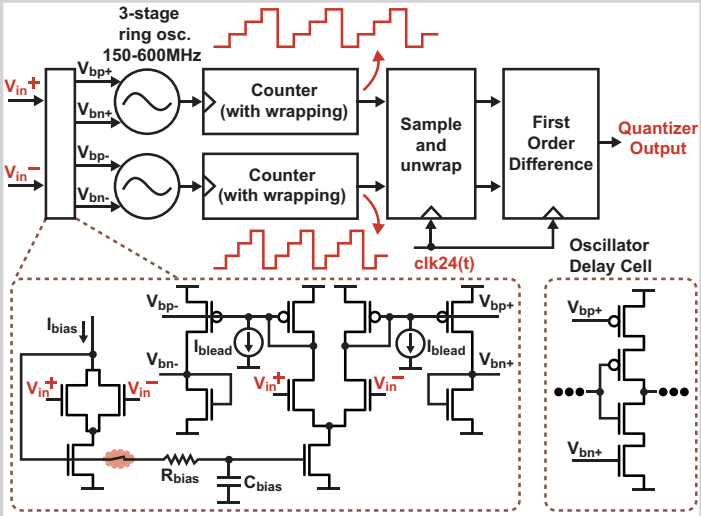

Figure 11.6.5: Pseudo-differential VCO-based quantizer in which counters are leveraged to lower the required sampling rate of the quantizer and pulsed current biasing for reduced noise.

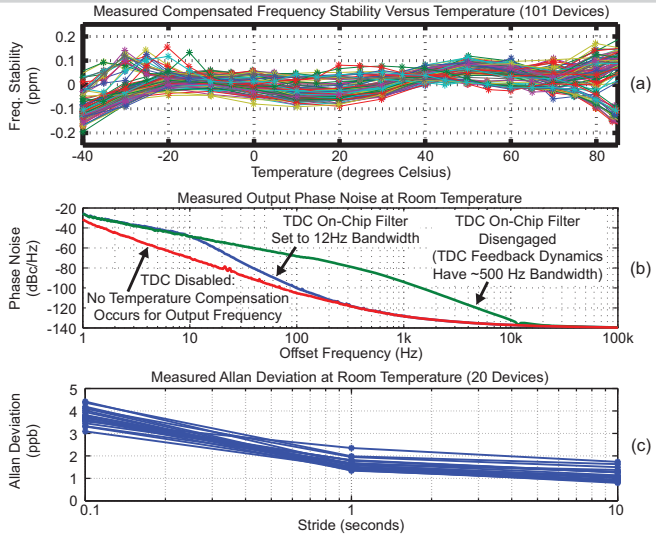

Figure 11.6.6: Measured results for (a) compensated frequency stability, (b) output phase noise at several TDC settings, and (c) Allan Deviation.

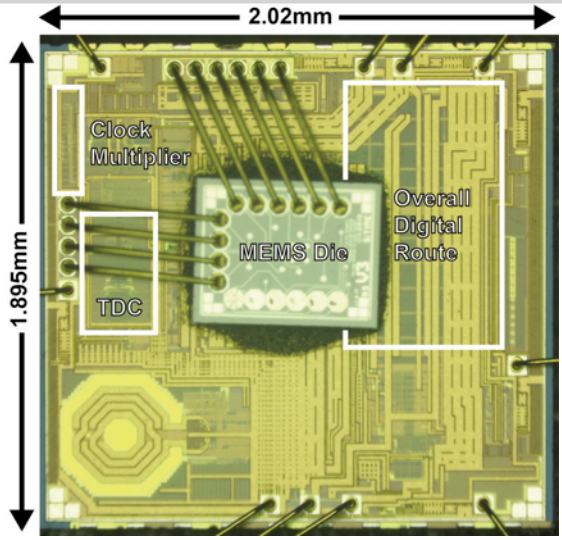

Figure 11.6.7: Micrograph of the 0.18µm CMOS die with MEMS die of the resonator and thermistor attached on top.

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