Short Course On
Phase-Locked Loops and Their Applications
Day 5, AM Lecture

Advanced PLL Examples (Part I)

Michael Perrott
August 15, 2008

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Outline

- Fast offset compensation for CDR limit amps
- Fractional-N based DLL
- Low-jitter multiplying DLL
- Sub-harmonic injection-locked oscillator
A 3.125 Gb/s Limit Amplifier in CMOS with 42 dB Gain and 1us Offset Compensation

Ethan A. Crain, Michael H. Perrott
Massachusetts Institute of Technology
A Fast Acquisition Limit Amp

- Acquisition time of CDR is limited by slow response of limit amp offset correction loop (typically milliseconds)
- Goal: improve speed of offset correction
**Motivation for Offset Compensation**

Without offset compensation the output of high gain amplifiers can saturate due to offset voltage alone.
Motivation for Offset Compensation

Offset compensation is required for high gain amplifiers to prevent the output from saturating due to offset.

Classical offset compensation methods suffer from long compensation times.
Why long settling times matter

Compensation only happens once in one-to-one links
Typical offset compensation time $\approx 1\text{ms}$
Why long settling times matter

The compensation time determines how quickly we can switch between channels
Outline

⇒ Proposed method
⇒ Peak detector design
⇒ System Details
⇒ Measured results
⇒ Conclusions
Proposed Method – Key Assumptions

- Assume that the data path is differential and the two data paths have approximately equal gains
- Assume that we are processing NRZ data
- The output-referred offset is equal to the difference in output common-mode levels
Proposed Method – Key Assumptions

\[ A \cdot V_{\text{offset}} = \max[V_+] - \max[V_-] \]
Traditional Peak Detector

Consider operation of traditional CMOS peak detector
Operation During Track Phase

\[
\frac{1}{\tau} \propto \sqrt{\frac{I_{bias}}{C_L}}
\]

Slew Rate \( \propto \frac{I_{bias}}{C_L} \)

Fast Offset Compensation \( \rightarrow \) Large \( I_{bias} \)
Operation During Hold Phase

\[ \text{Droop} = I_{\text{bias}} \cdot \frac{T_{\text{data}}}{C_L} \]

Droop proportional to both \( I_{\text{bias}} \) and \( T_{\text{data}} \)

Data dependent droop → Jitter (ISI)

Small Jitter → Small \( I_{\text{bias}} \)
Trade-Off for Traditional Peak Detector

Trade-off between settling time and jitter performance due to Inter-Symbol Interference!

Fast Settling $\rightarrow$ Large $I_{bias}$  Low Jitter $\rightarrow$ Small $I_{bias}$

Can we modify the design to improve the trade-off?
Add switch device that is controlled by the input
Proposed Solution – Track Phase

\[ \frac{1}{\tau} \propto \sqrt{\frac{I_{\text{bias}}}{C_L}} \]

Slew Rate \( \propto \frac{I_{\text{bias}}}{C_L} \)

Same operation as original peak detector circuit
Proposed Solution – Hold Phase

Droop is ideally independent of both $I_{bias}$ and $T_{data}$

Can achieve small jitter with a large $I_{bias}$
Proposed Solution – Differential Design

Use inputs to switch $I_{bias}$ between the two source-follower circuits.
Proposed Solution – Operation

Incomplete switching causes non-zero droop
Proposed Solution – Operation

Incomplete switching causes non-zero droop

Simultaneously achieve fast offset compensation and low droop
Dynamic multi-tap control loops are required
Peak detector at each amplifier output
All loops have matched gain
Test System – Die Micrograph

- 3.125Gb/s limit-amp.
  42dB gain
  5GHz BW
- Compensation
time $< 1\mu s$
- Meet OC48 jitter specs.
  $< 4ps_{RMS}$ @ 2.5Gb/s
- Total area: 1$mm^2$
- Active area: 0.5$mm^2$
- Supply Voltage: 1.8V
- Total Power: 338mW
- Power of LA & Offset Compensetion: 113mW

Fabricated in National Semiconductor’s
0.18$\mu m$ CMOS process
Test System – Measured Results

Eye diagrams with $2.5mV_{pp}$ PRBS $2^{31} – 1$ input

Offset Compensation Settling time $\approx 1\mu s$

$2.5Gb/s \rightarrow Jitter = 3.71\text{ps RMS}$

$3.125Gb/s \rightarrow Jitter = 5.90\text{ps RMS}$

Horizontal Scale: 100ps/div  Vertical Scale: 50mV/div

$V_{control}$

$V_{offset}$

$V_{in}$

$A(s)$

$V_{out}$

$-\rightarrow +$

Offset Comp.
Test System – Measured Results

Offset Compensation Settling time $\approx 1\mu s$

<table>
<thead>
<tr>
<th>Input Amp</th>
<th>1.0Gb/s</th>
<th>2.5Gb/s</th>
<th>3.125Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5mVpp</td>
<td>3.94</td>
<td>3.71</td>
<td>5.90</td>
</tr>
<tr>
<td>10mVpp</td>
<td>2.65</td>
<td>2.86</td>
<td>6.30</td>
</tr>
<tr>
<td>50mVpp</td>
<td>1.13</td>
<td>2.52</td>
<td>7.98</td>
</tr>
</tbody>
</table>

Meets OC-48 Jitter Spec ($< 4.0\text{ps RMS}$) down to $V_{in,pp} = 2.5mV$
**Test System – Measured Results**

Control voltage step-response with a $5.0mV_{pp}$ PRBS $2^{31} - 1$ input

- Compensation Settling time goal $\approx 1\mu s$
- $3.125Gb/s \rightarrow Jitter = 5.75ps$ RMS

- Compensation Settling time goal $\approx 0.33\mu s$
- $3.125Gb/s \rightarrow Jitter = 5.90ps$ RMS

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**Diagram:**

- $V_{control}$
- $V_{offset}$
- $A(s)$
- $V_{in}$
- $V_{out}$
- OffsetComp.
Summary

- Proposed peak detector design enables a 1000x improvement in the trade-off between settling time and output jitter by changing relationship between peak detector bandwidth and output droop.

- Implemented and tested system with proposed offset compensation method that has 2.5mVpp input sensitivity and that meets OC48 jitter specifications (< 4ps RMS @ 2.5Gb/s).

- Behavior model download:
  - [http://www.cppsim.com](http://www.cppsim.com)
A Delay-Locked Loop using a Synthesizer-based Phase Shifter for 3.2 Gb/s Chip-to-Chip Communication

Chun-Ming Hsu, Charlotte Y. Lau, Michael H. Perrott
Massachusetts Institute of Technology
In some applications, a reference clock that is perfectly matched in frequency to data sequence is available

- Phase mismatch is present due to different propagation delays between clock and data on the PC board

A delay-locked loop limits adjustment to phase (as opposed to phase and frequency)

- Faster, and much simpler to design than PLL structure
Delay-Locked Loop using Phase-Interpolator

- Infinite delay range and good jitter performance
- Issue:

Good matching needed for accurate phase control, but future processes promise high variation …
Can we eliminate the need for good matching?
Proposed DLL

- Use $\Sigma$-$\Delta$ frequency synthesizer as a phase shifter
**VCO-based Phase Shifter**

- VCO output phase increases or decreases by a step when a pulse is fed into it
- Fine phase resolution and infinite range are achieved

**Issue1:** How to control the VCO frequency accurately?

**Issue2:** How to control the phase step accurately?
Solution: Synthesizer-based Phase Shifter

- Use a PLL to lock VCO frequency to received clock
- Use Σ-Δ technique in digital domain to control the VCO phase
Most Synthesizer Applications Look at **Frequency**

Fractional output frequency is provided by a fractional-N frequency synthesizer.
Here We Will Look at Phase ....

- Phase step decreases together with pulse height

Phase step is determined only by the number of bits of the Σ-Δ modulator → No process, voltage, and temperature (PVT) variations
Design Consideration of the Phase Shifter

- Wait enough time before feeding next pulse to allow proper settling of VCO phase $\rightarrow T_d > 1/$bandwidth

- How to implement a simple $\Sigma$-$\Delta$ modulator?
Phase Shifter Guided by Staircase Input

Use a differentiator to generate the pulses from a staircase input
Phase Shifter Guided by Up/Down Counter

- VCO phase shifts according to Up/Down counter
Phase Shifter Guided by Up/Down Counter (cont’d)

- VCO phase shifts according to Up/Down counter
Phase Shifter Guided by Up/Down Counter (cont’d)

- Phase resolution improves by increasing number of bits in the hardware
Problem: Up/Down Counter Overflows

- Large negative pulse caused by overflow rotates VCO phase by a large step in the wrong direction
- Phase shifter provides a phase range of only $2\pi$
Solution: Add Overflow Signal to Output

- Generate a +1 pulse to cancel the undesired -15/16 pulse
- Phase shifter provides an infinite phase range
Quantization Noise of Phase Shifter

- Second-order quantization noise exists
- Transfer function of a differentiator is the same as noise transfer of a first-order Σ-Δ modulator
Quantization Noise of Phase Shifter (cont’d)

- Change the order of differentiator and modulator
- Same quantization noise obtained with a first-order Σ-Δ modulator → Less circuit complexity
Proposed $\Sigma$-$\Delta$ Modulator

- Output is three-value $(1,0,-1)$
- Divider with three division ratios $(N-1, N, N+1)$ is necessary
Proposed Σ-Δ Modulator (cont’d)

- Multiple first-order Σ-Δ Modulators are used
  - Bit number decreases as operating frequency increases
  - Metastability and synchronization problems are avoided

Easy Design and low power
Proposed Σ-Δ Modulator (cont’d)

Blue: 533-MHz Modulator
Green: 267-MHz Modulator
Red: 33-MHz Modulator
Overflow signals are realigned to main signals in each domain
Output is still three-value even with the extra adder
Use Bang-Bang detector for phase comparison
Proposed Bang-Bang Architecture

- An analog integrator, whose output is saturated to VDD or GND, is used to accumulate bang-bang detector output
**DLL Prototype Chip for 3.2 Gb/s Communication**

- 8-bit Σ-Δ modulator → 1.4° phase resolution
- Simple analog components without need of good matching
Chip Microphotograph

- Implemented by 0.18um CMOS Process
- Core Area: 600um X 700 um
- 1.8 V, 55 mA (excluding I/O buffer)
DLL Measured Jitter

- **Left:** 3.2Gb/s PRBS $2^{31}-1$
  - Single-ended clock jitter < 4.8ps
  - Single-ended data jitter < 30.5ps

- **Right:** 3.2Gb/s PRBS $2^{31}-1$
  - Differential clock Jitter < 3.7ps

- BER < $10^{-12}$
Non-ISI-limited DLL Jitter

- 1.6Gb/s PRBS $2^7-1$
  - Single-ended clock Jitter < 4.7ps
  - Single-ended data jitter < 5.2ps
- BER < $10^{-12}$
Conclusion

- A DLL architecture is proposed
  - Σ-Δ synthesizer is used as the phase shifter
  - A compact and low-power Σ-Δ modulator
  - Simple Bang-bang detector is used for phase detection
- Prototype is implemented for 3.2 Gb/s chip-to-chip communication
- The DLL provides a digitally-controlled phase adjustment with fine-resolution and infinite-range that is not sensitive to PVT variations
- The overall architecture is insensitive to mismatch
  - Well suited for more advanced CMOS processes with high variability
Low Jitter, Highly Digital, MDLL-based Clock Multiplier

Belal M. Helal, Matthew Z. Straayer, Gu-Yeon Wei* and Michael H. Perrott
Motivation

- **Issue:** Clock multiplication using phase-locked loops complicates the design of digital chips.

- **Goal:** Achieve a highly digital clock multiplier that can be easily ported across different CMOS processes.
  - Do not compromise on jitter performance

We will present a non-PLL based clock multipliers that achieves sub-ps jitter performance.
PLL: Typical Architecture for Clock Multiplication

- Application determines VCO type
  - Lowest noise → LC oscillator
  - Smallest area → Ring oscillator

- How to reject the high phase noise of a ring oscillator?
Rejection of High Phase Noise in Ring Oscillators

- Phase noise contributors: VCO and PFD noise
  - Affected differently by PLL bandwidth, $f_0$
- VCO noise: high-pass filtered, PFD noise: low-pass filtered
  - Tradeoff: bandwidth $\uparrow \rightarrow$ VCO noise $\downarrow$, PFD noise $\uparrow$
- Can we suppress VCO noise without large bandwidth?
**Time Domain View: Reducing VCO Jitter**

- **Problem:** Jitter accumulates with time according to loop dynamics to a steady state level, $\sigma_{ss}$

- **Solution:** reset jitter at a rate faster than the loop BW
  - How?

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McNeill, JSSC, June 1997
**Multiplying DLL Concept**

- **Goal:** Create a higher frequency clock from an input reference signal

- **Replace jittery edge with clean Reference edge**
  - Accumulated jitter is periodically removed
The Benefit of the MDLL Approach

- Phase noise of ring oscillator is suppressed by the periodic multiplexing of reference edge
- Transfer function approximates a 1\textsuperscript{st} order high pass filter
  - \( f_{\text{hpf}} \approx \frac{f_{\text{Ref}}}{4} \)

High bandwidth suppression of phase noise independent of loop bandwidth
**Deterministic Jitter in MDLLs**

- **Key issue:** Need to precisely tune ring oscillator frequency
- **Offset in frequency results in inconsistent period**
  → deterministic jitter

**Goal:** Reduce deterministic jitter to the level of random jitter
**Deterministic Jitter Observed in Output Spectrum**

- Deterministic jitter shows up as reference spurs

- Relationship by Fourier analysis

\[ \Delta \approx T_{\text{out}} \times 10^{\text{Spur}(\text{dBc})/20} \]

Deterministic Jitter can be estimated from reference spurs
**Classical Analog Approach**

- **Key idea:** Compare edges of MDLL output and reference to detect error ($\Delta$)
  - Integrate error to adjust $V_{\text{tune}}$
- **The problem:** Mismatches and offsets in the phase detector and integrator limit reduction of $\Delta$

**Low deterministic jitter is challenging to achieve**

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Proposed Detection Approach

- Compare cycle periods of MDLL output
- Infer error (Δ) from difference between cycle periods of the MDLL output

Comparison of same signal eliminates path mismatch
Detection of the Output Period

- Need an accurate period detector
  - Error removal is limited by the effective resolution of the detector
- A digital detector has many advantages
  - Time-to-digital converter (TDC)
Gated Ring Oscillator (GRO) is ON during the measured period

Raw resolution is one inverter delay

Quantization noise is scrambled (and first order noise shaped)

Effective resolution improved by averaging
Using the GRO in the proposed MDLL Architecture

- **Div\(_{2x}\)** selects two output periods per reference cycle
- Sub-picosecond effective resolution is possible
  - \(T_{\text{gro}} = 50\) ps, \(F_s = 100\) MHz, \(BW = 10\) KHz \(\Rightarrow\) Eff. Res. \(\approx 0.7\) ps

**GRO Detects the Output Period Accurately**
Digital Correlator Extracts the Error

- Digital version of correlated double-sampling technique
Close the Loop

- Digital accumulator
  - Infinite DC gain
  - No DC offsets
  - Allows low bandwidth without leakage or large area
- $V_{\text{tune}}$ adjustment only needs to track thermal variations
MDLL Prototype

- Two custom 0.13μm CMOS ICs
  - GRO (Matt Straayer) and core MDLL structures
- FPGA
  - Digital Correlator, Accumulator and digital ΣΔ-modulator
- Discrete 16-bit DAC and RC lowpass filter (3 MHz pole)
  - DAC using 8 effective bits (by using the ΣΔ-modulator)
Power Consumption and Area

- **Core MDLL**
  - Area: 0.04 mm²
  - Power: 3.9 mW

- **GRO-based TDC**
  - Area: 0.02 mm²
  - Power: 1.2 mW
Circuit Details
**Multiplexed Ring Oscillator**

- **Balanced differential loading**
  - Better PSRR and 1/f noise
- **Five delay stages, no external connections to multiplexer**
  - Faster edges → better multiplexing

Similar to: Dai, Harjani, ASIC-SOC, Sep. 2001
Select Logic and Enable Logic

- **Select Logic**
  - Mostly standard cells
  - Relaxed timing
  - Sel at middle of output transition
    → better multiplexing

- **Enable Logic**
  - Simple implementation
  - Single path detection
**Measured Overall Jitter**

- Measured overall jitter:
  - 928 fs (rms)
  - 11.1 ps (peak-to-peak)

**Sub-picosecond jitter**
Jitter Estimation from Measured Ref. Spur and Ph. Noise

- Reference spur: -58.3 dBc
  - Deterministic jitter: $\approx 760$ fs (peak-to-peak)
- Random jitter: 679 fs (rms)
  - From integrated phase noise (1 kHz to 40 MHz)

Sub-picosecond of estimated random and deterministic jitter
## Performance Comparison

<table>
<thead>
<tr>
<th></th>
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<td>Output Frequency (GHz)</td>
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<td>0.176</td>
<td>1.6</td>
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<td>Reference Frequency (MHz)</td>
<td>250</td>
<td>64</td>
<td>8</td>
<td>50</td>
</tr>
<tr>
<td>Reference Spur (dBc)</td>
<td>-37</td>
<td>-46.5</td>
<td>-70 (estimated)</td>
<td>-58.3</td>
</tr>
<tr>
<td>Deterministic Jitter (ps pp) estimated from meas. Spurs (Figure-of-merit)</td>
<td>7.06</td>
<td>3.89</td>
<td>1.80</td>
<td>0.76</td>
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<td>1.80</td>
<td>0.76</td>
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<td>Random Jitter (ps rms)</td>
<td>N/A</td>
<td>N/A</td>
<td>5 (1.8 simulated) (1 kHz to 10 MHz)</td>
<td>0.68 (1 kHz to 40 MHz)</td>
</tr>
<tr>
<td>Overall Jitter</td>
<td>1.62 ps (rms)</td>
<td>(@2.16 GHz)</td>
<td>1.6 ps (rms)</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>13.11 ps (p-p)</td>
<td>12.9 ps (p-p)</td>
<td>12.2 ps (p-p)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25 khits</td>
<td>25 khits</td>
<td>12.2 khits</td>
<td></td>
</tr>
<tr>
<td>Technology (CMOS)</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>0.13 μm</td>
</tr>
</tbody>
</table>
Conclusion

- **Digital Period Correlator**
  - Detects tuning error without path mismatch
  - Enables a digital loop filter

- **Highly-digital tuning technique**
  - Avoids analog non-idealities
  - Enables low bandwidth without leakage or large area

- **Highly digital MDLL**
  - 1.6 GHz from 50 MHz reference
  - Significantly-reduced deterministic jitter
  - Sub-picosecond jitter
A Low Noise Programmable Clock Multiplier based on a Pulse Injection-Locked Oscillator with a Highly-Digital Tuning Loop

Belal M. Helal, Chun-Ming Hsu, Kerwin Johnson, and Michael H. Perrott
Motivation

- **Goal:** clock multiplication of a clean reference source
  - Applications: high performance data links, ADCs, processors, etc.
- **Our approach:** sub-harmonic injection-locking of an LC oscillator

How do we achieve very low jitter levels?
Sub-Harmonic Injection-Locking of an LC Oscillator

- Sub-harmonic injection locking can be achieved with current pulses
  - Pulses have rich harmonic content to lock to
  - Oscillator locks its voltage peaks to the pulses
  - Locking bandwidth proportional to the injected charge

[Ref. Razavi, JSSC 2004]
[Ref. Toso et al., ISSCC 2008]
Problems with Current Pulse Injection Locking

- Asymmetric injections in differential oscillators
  → large reference spurs
- Current pulses have constant level even at ideal tuning
  → Oscillator amplitude is disturbed periodically
  → increased reference spurs

[Toso et al., ISSSC 2008]
Proposed Pulse Injection-Locked Oscillator (PILO)

- Injection lock by shorting the tank instead of using constant current pulses
- Injected pulse shifts phase towards zero crossing
- Minimal disturbance to oscillator amplitude when injected with narrow pulses and properly tuned
The Need for Continuous Tuning

Injected pulse

\[ I_{osc} \]
\[ V_{osc} \]

Ref

Injected pulse

\[ V_{tune} \]

too high

too low

ideal
How do we achieve continuous tuning?
Leverage a tuning technique originally developed for Multiplying Delay-Locked Loops (MDLLs)
- See Helal et al., JSSC, April 2008
Output Period Detection

- Compare cycle periods of PILO output
- Infer error ($\Delta$) from difference between cycle periods of the PILO output
- Use this information to control $V_{\text{tune}}$

Comparison of same signal eliminates path mismatch
Detection of the Output Period

- Need an accurate period detector
  - Error removal is limited by the effective resolution of the detector
- A digital detector has many advantages
  - Time-to-digital converter (TDC)
Scrambling TDC

- Gated Ring Oscillator (GRO) is ON during the measured period
- Quantization noise is scrambled (and first order noise shaped)
  - Effective resolution improved by averaging
- We are using a new version of the GRO
  - Details in Straayer, et al., VLSI 2008
Using the GRO in the proposed PILO Architecture

- Oversampling improves the effective resolution significantly
  - $T_{gro} = 20$ ps, $F_s = 100$ MHz, $BW = 1$ kHz
  - Effective resolution $\approx 90$ fs

GRO detects the output period accurately
Digital Correlator Extracts the Error

- Digital version of correlated double-sampling technique
Close the Loop

- **Digital accumulator**
  - Infinite DC gain
  - No DC offsets
  - Allows low bandwidth without leakage or large area

- \( V_{\text{tune}} \) adjustment only needs to track thermal variations
**PILO Prototype**

- **Custom 0.13μm CMOS IC**
  - Active area: 0.4 mm$^2$
  - Active Power: 28.6 mW

- **FPGA**
  - Accumulator and digital $\Sigma\Delta$-modulator

- **Discrete 16-bit DAC and RC lowpass filter (500 kHz pole)**
  - DAC using 8 effective bits (by using the $\Sigma\Delta$-modulator)
Circuit Details
Proposed PILO Implementation

- **Differential Injection by shorting**
  - Minimizes deterministic jitter by preserving injection symmetry
- **Narrow pulses minimize effect on Q of the tank**
  - Minimal residual effect when tuned
Enable Logic

- Asynchronous Modular divider
- Pulse width of $\mod_x \approx$ multiples of VCO periods
  → Enable signal from any mod output (with reasonable width)
- Simple implementation and low power consumption

[similar to Voucher, et al, JSSC 2000]
Enable Logic: Divider Step Control

- **GRO TDC must capture periods that includes the injected pulse**
  → Divider stepped until Ref rises during Enable
Measured Results
**Measured Phase Noise (Open-loop tuned PILO)**

- **Random jitter:** 91 fs (rms)
  - From integrated phase noise (1 kHz to 20 MHz)
**Measured Phase Noise (close-loop tuned PILO)**

- **Random jitter:** 134 fs (rms)
  - From integrated phase noise (1 kHz to 40 MHz)
**Measured Reference Spurs and Est. Deterministic Jitter**

- Reference Spur: -63.4 dBc

- From Fourier analysis: $\Delta \approx T_{out} \times 10^{Spur(dBC)/20}$

  → Estimated deterministic jitter $\approx 211$ fs (peak-to-peak)
Performance Summary

<p>| | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>Process</strong></td>
<td>0.13 μm CMOS</td>
</tr>
<tr>
<td><strong>Core Area</strong></td>
<td>0.4 mm²</td>
</tr>
<tr>
<td><strong>Core Power</strong></td>
<td>28.6 mW</td>
</tr>
<tr>
<td><strong>Output Frequency</strong></td>
<td>3.2 GHz (up to 4 GHz)</td>
</tr>
<tr>
<td><strong>Reference Frequency</strong></td>
<td>50 MHz</td>
</tr>
<tr>
<td><strong>Reference Spur</strong></td>
<td>-63.4 dBc</td>
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<td><strong>Deterministic Jitter</strong></td>
<td>211 fs (peak-to-peak), estimated from measured reference spurs</td>
</tr>
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<td>134 fs (rms), from integrated phase noise (1 kHz to 40 MHz)</td>
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</table>
**Future Research Area: Optical PILO**

- RF output from an optical reference input
- Leverage Mode-Locked lasers
  - Train of very short optical pulses
  - Ultra-low jitter in the range of 10’s fs to sub-fs
Conclusions

- Clock multiplication by injection locking
  - Lower jitter than typical PLLs
  - Achieved continuous tuning

- Pulse Injection-Locked Oscillator (PILO)
  - Injection by shorting minimizes deterministic jitter when tuned

- PILO-based clock multiplier with highly-digital tuning
  - 3.2 GHz from 50 MHz reference
  - Random jitter: 134 fs (rms)
  - Deterministic jitter: 211 fs (peak-to-peak)
  - Avoids analog non-idealities
  - Enables low bandwidth without leakage or large area