Short Course On
Phase-Locked Loops and Their Applications
Day 1, AM Lecture

Integer-N Frequency Synthesizers

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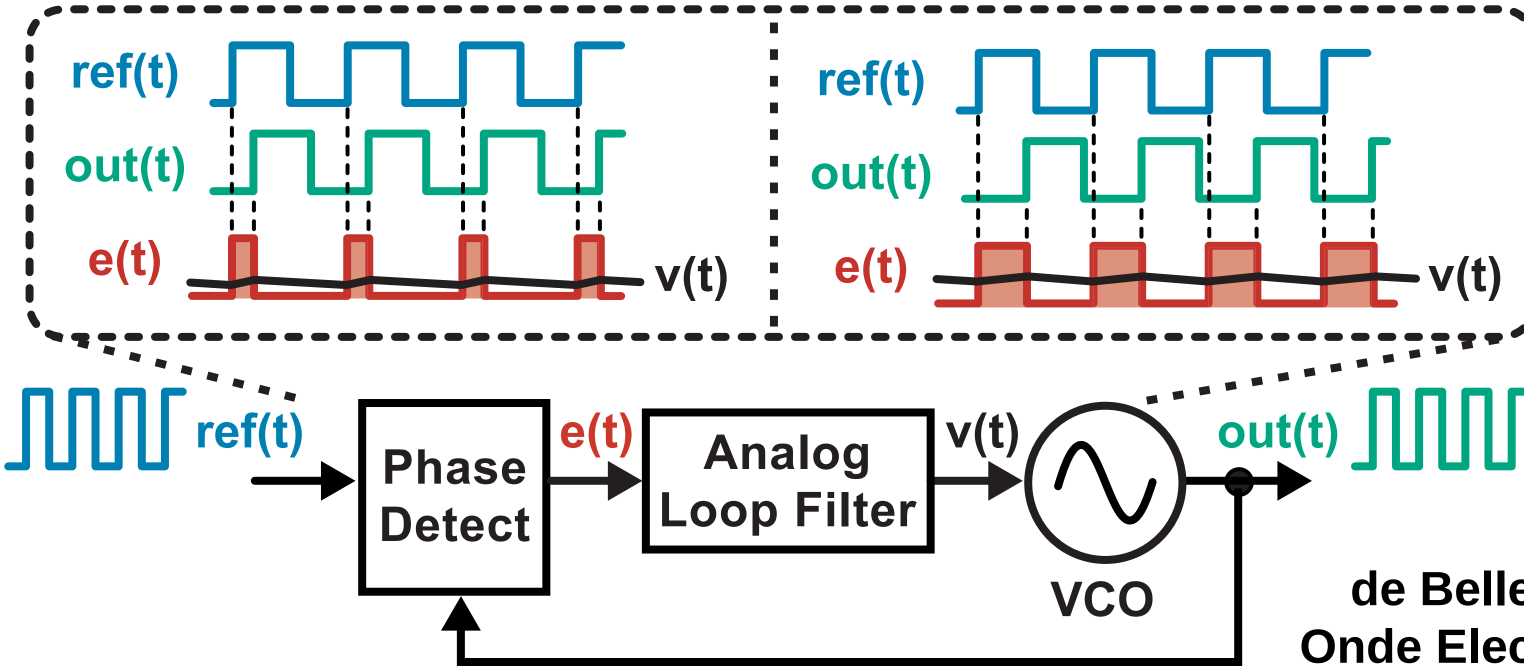
August 11, 2008

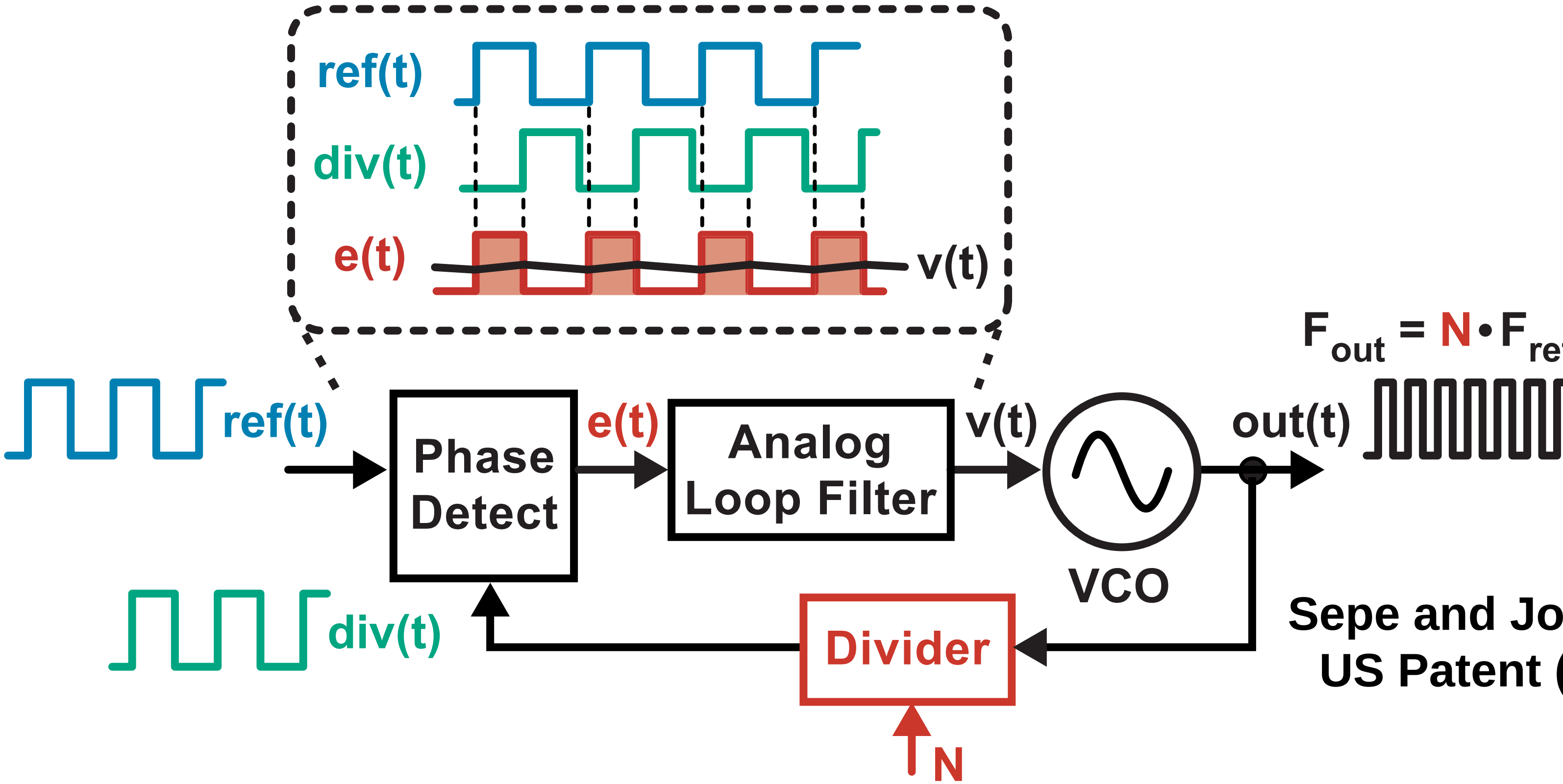
What is a Phase-Locked Loop (PLL)?



de Bellescize
Onde Electr, 1932

- **VCO efficiently provides oscillating waveform with variable frequency**
- **PLL synchronizes VCO frequency to input reference frequency through feedback**
  - **Key block is phase detector**
    - Realized as digital gates that create pulsed signals

Integer-N Frequency Synthesizers

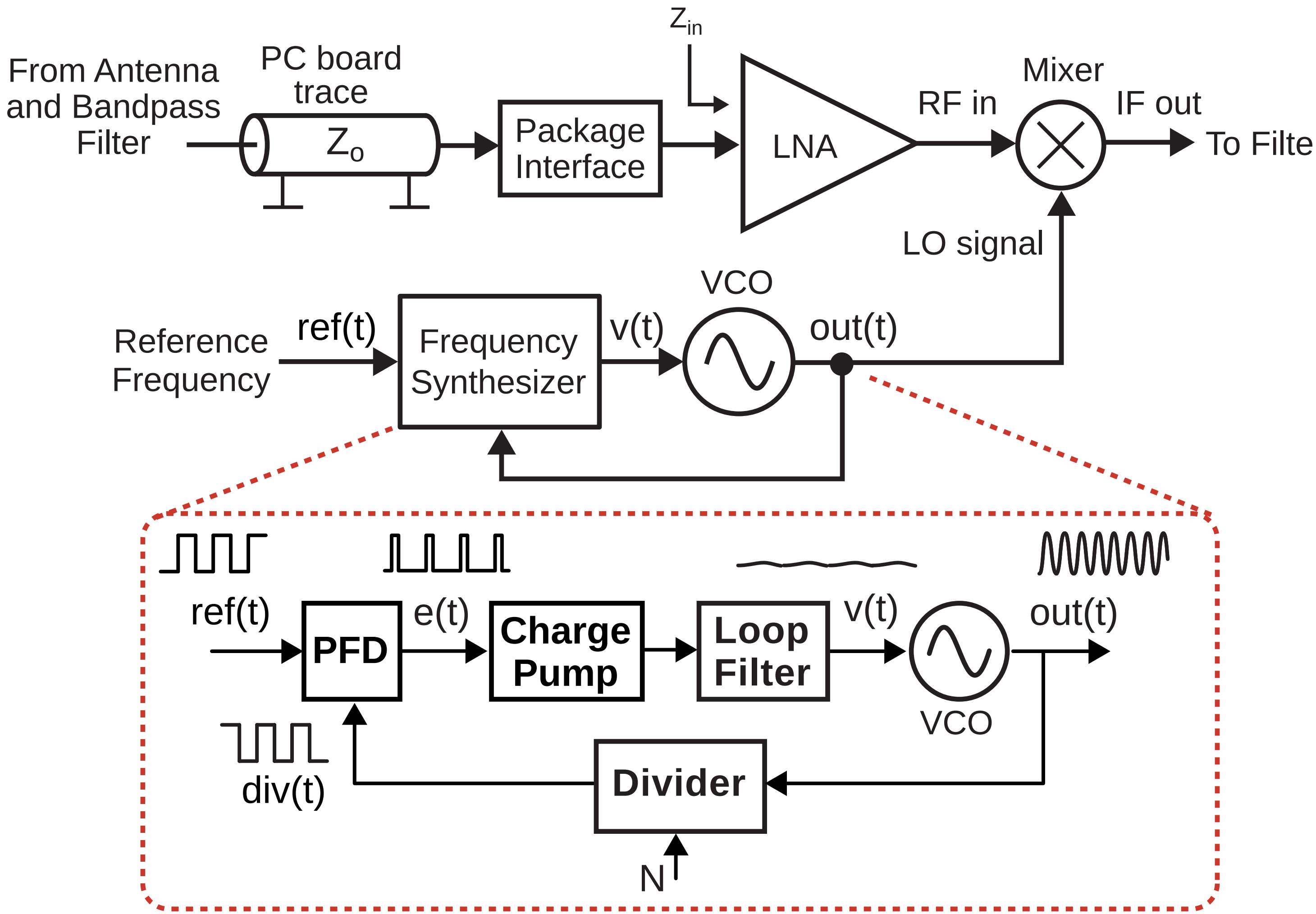


Sepe and Johnston US Patent (1968)

- Use digital counter structure to divide VCO frequency
  - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

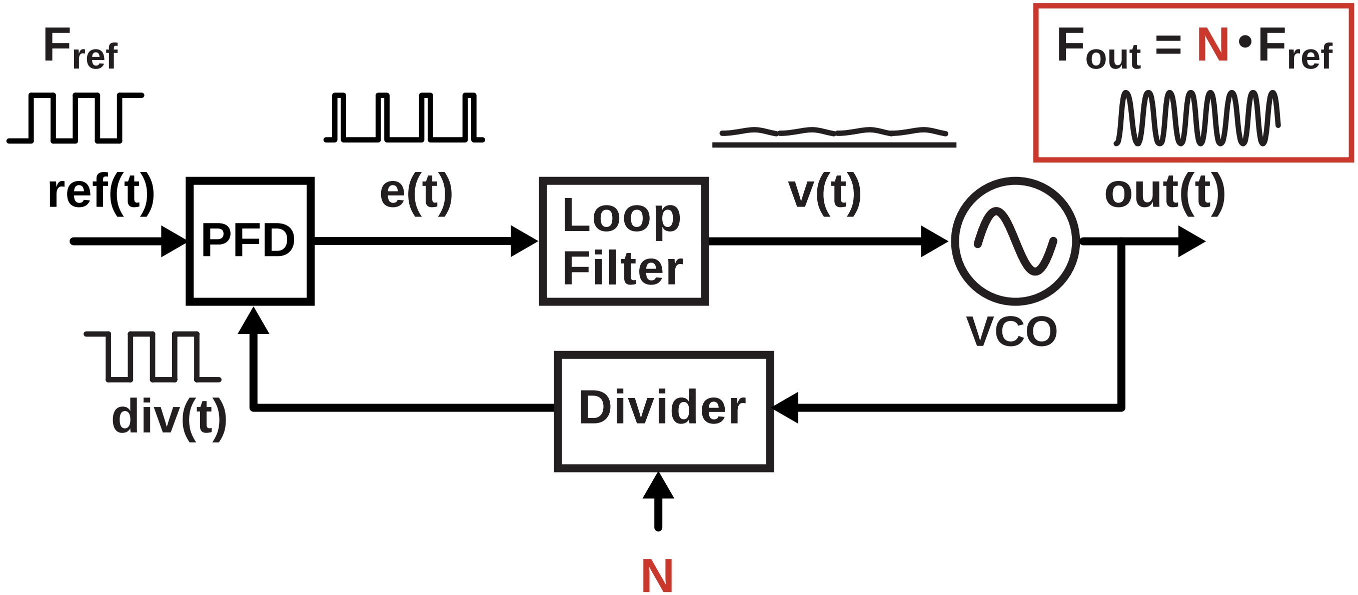
Output frequency is digitally controlled

Integer-N Frequency Synthesizers in Wireless Systems



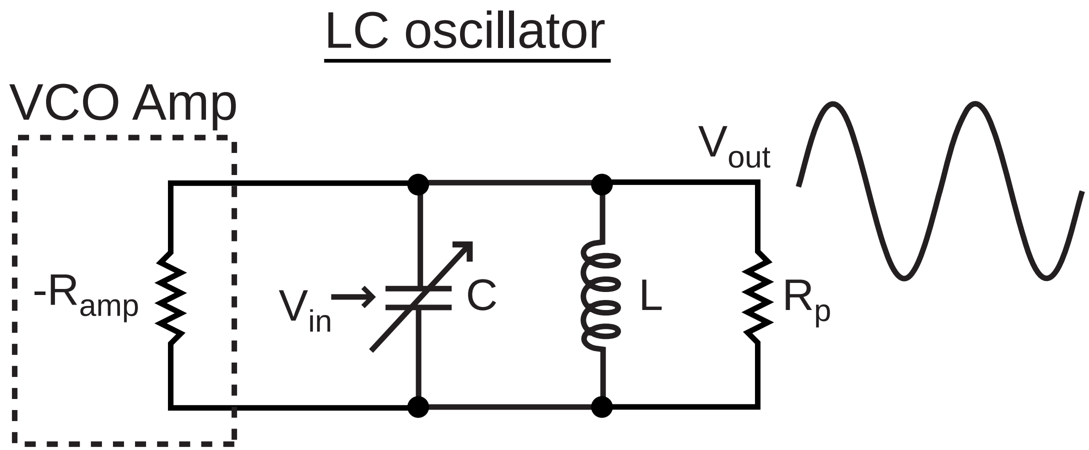
- Design Issues: low noise, fast settling time, low power

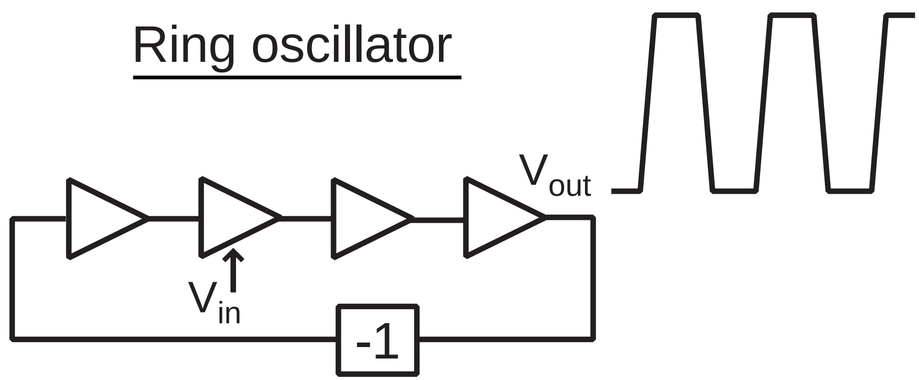
Outline of Integer-N Frequency Synthesizer Talk



- Overview of PLL Blocks
- System Level Modeling
  - Transfer function analysis
  - Nonlinear behavior
  - Type I versus Type II systems
- Noise Analysis

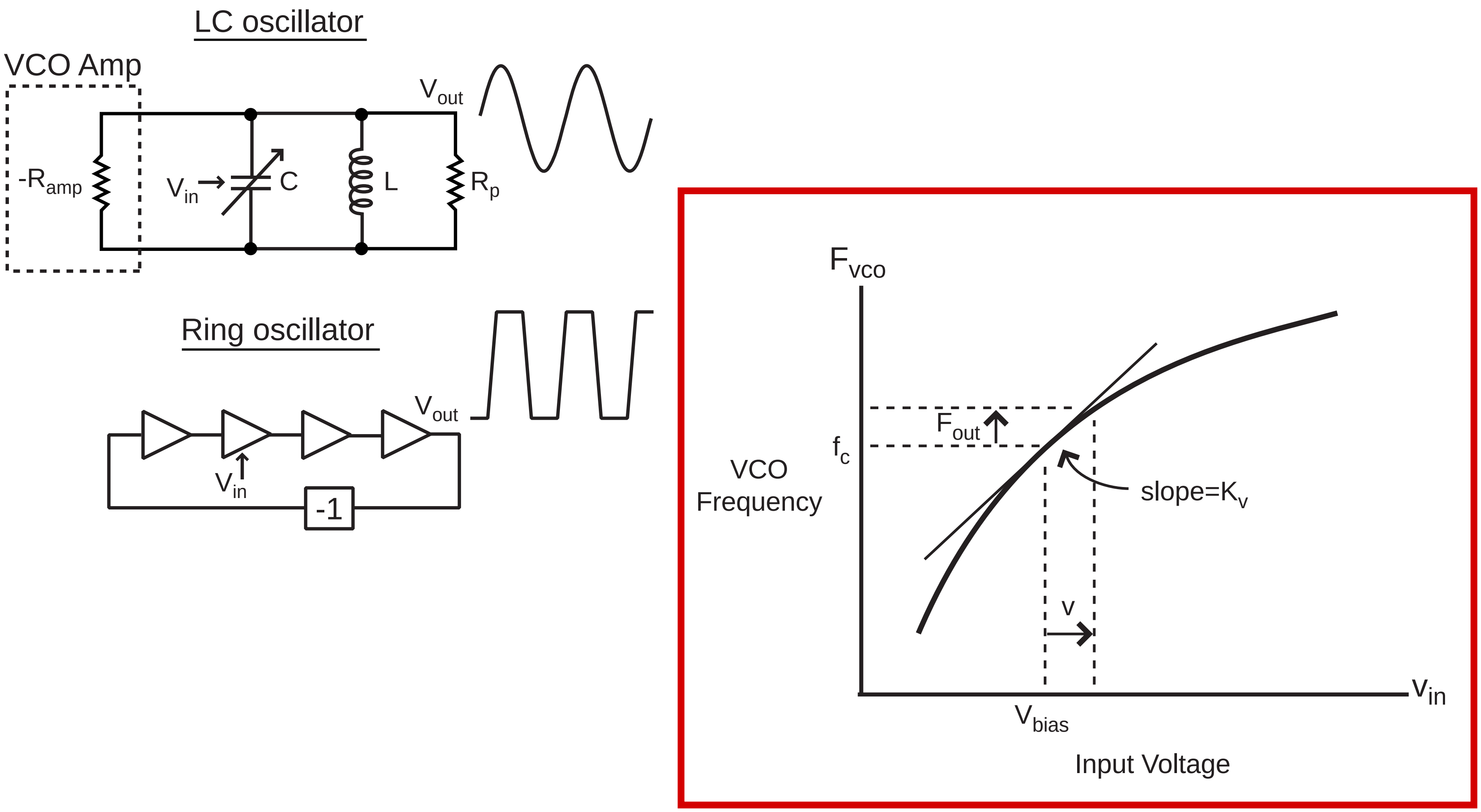
Popular VCO Structures





- **LC Oscillator: low phase noise, large area**
- **Ring Oscillator: easy to integrate, higher phase noise**

Model for Voltage to Frequency Mapping of VCO



$$F_{out}(t) = K_v v(t)$$

Model for Voltage to Phase Mapping of VCO

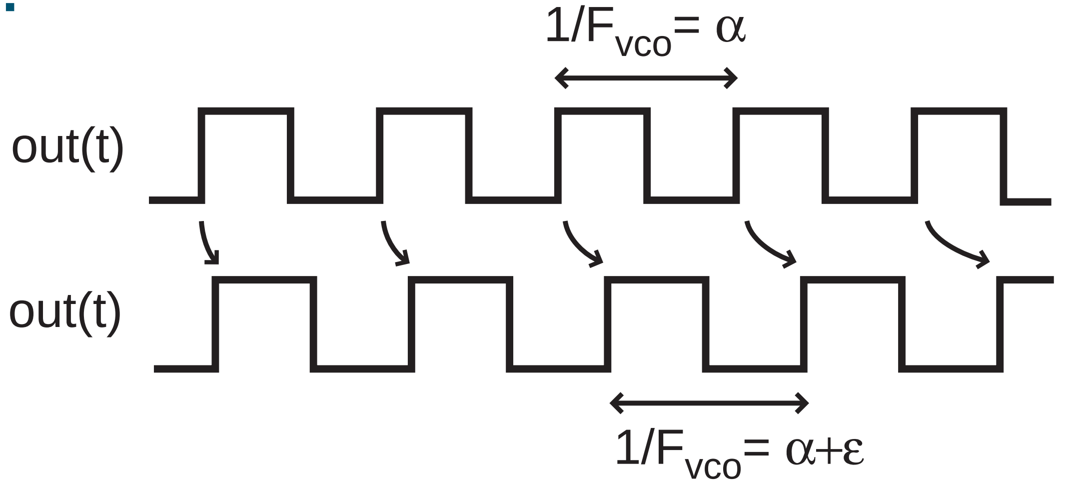
- **Time-domain frequency relationship (from previous slide)**

$$F_{out}(t) = K_v v(t)$$

- **Time-domain phase relationship**

$$\Phi_{out}(t) = \int_{-\infty}^{t} 2\pi F_{out}(\tau) d\tau = \int_{-\infty}^{t} 2\pi K_v v(\tau) d\tau$$

- **Intuition of integral relationship between frequency and phase:**

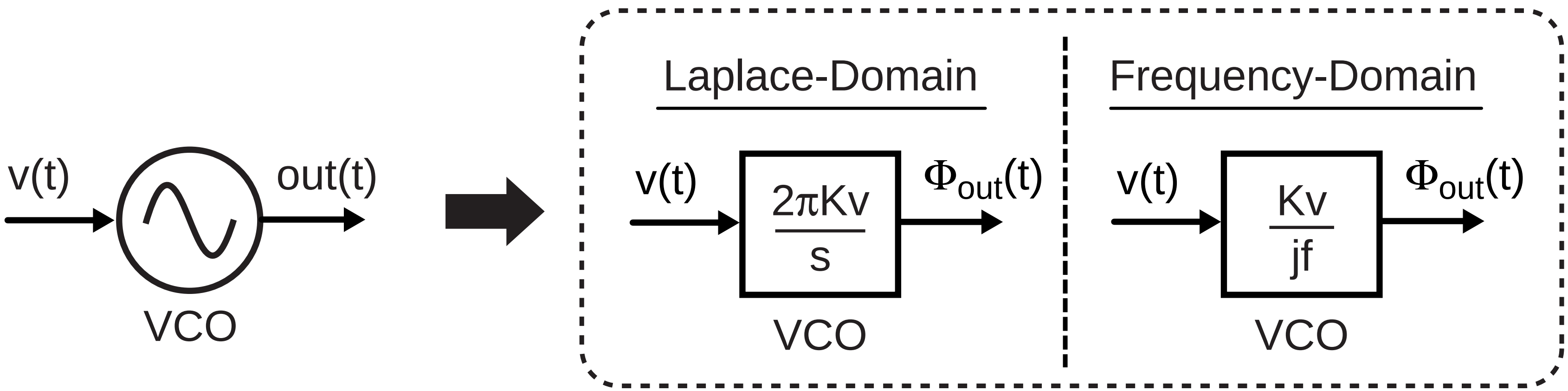


Frequency-Domain Model for VCO

- **Time-domain relationship (from previous slide)**

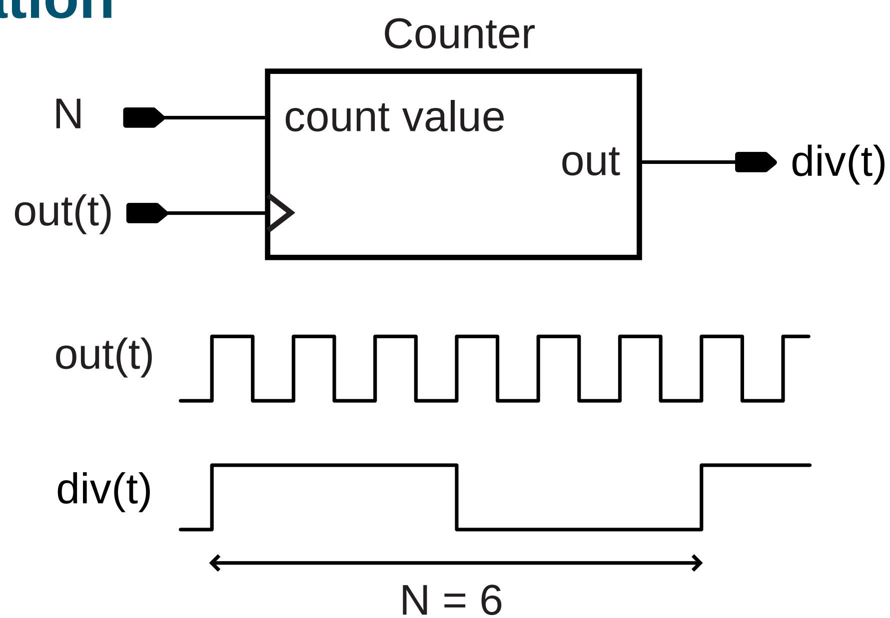
$$\Phi_{out}(t) = \int_{-\infty}^{t} 2\pi K_v v(\tau) d\tau$$

- **Corresponding frequency-domain model**



Divider

- **Implementation**



- **Time-domain model**
  - **Frequency:**

$$F_{div}(t) = \frac{1}{N} F_{out}(t).$$

  - **Phase:**

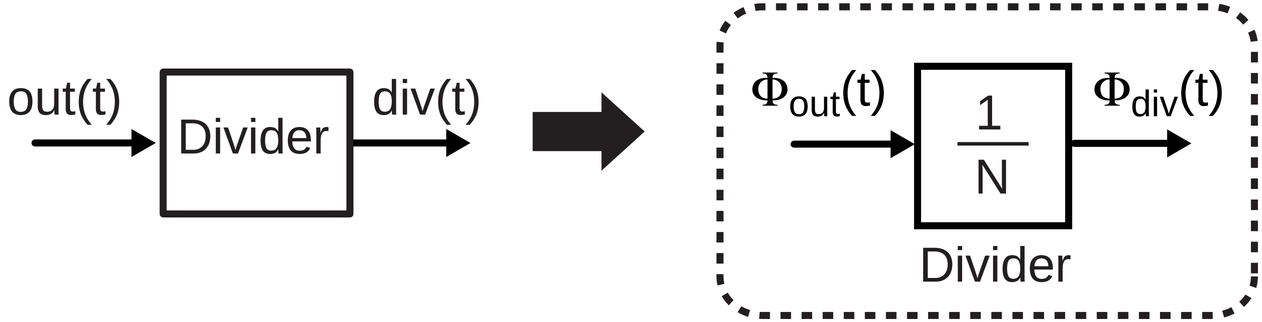
$$\Phi_{div}(t) = \int_{-\infty}^{t} 2\pi \frac{1}{N} F_{out}(\tau) d\tau = \frac{1}{N} \Phi_{out}(t)$$

Frequency-Domain Model of Divider

- **Time-domain relationship between VCO phase and divider output phase (from previous slide)**

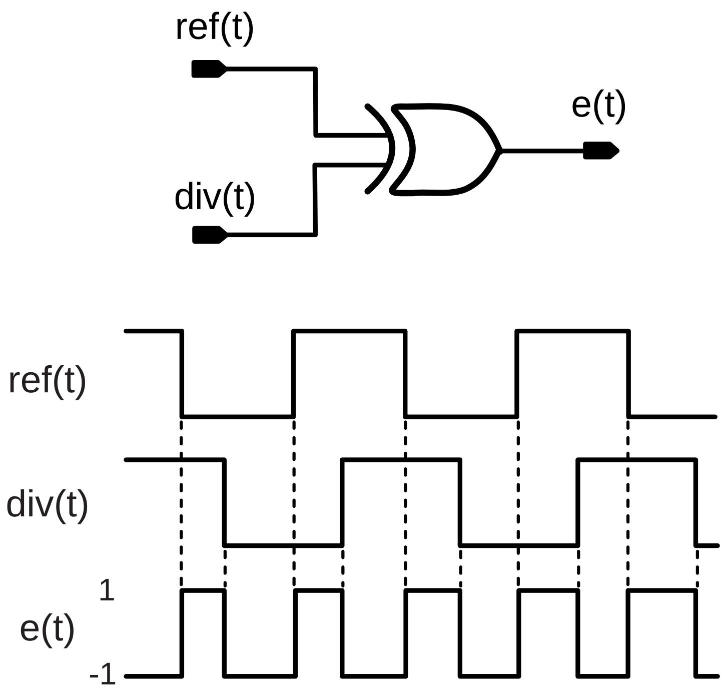
$$\Phi_{div}(t) = \frac{1}{N}\Phi_{out}(t)$$

- **Corresponding frequency-domain model (same as Laplace-domain)**



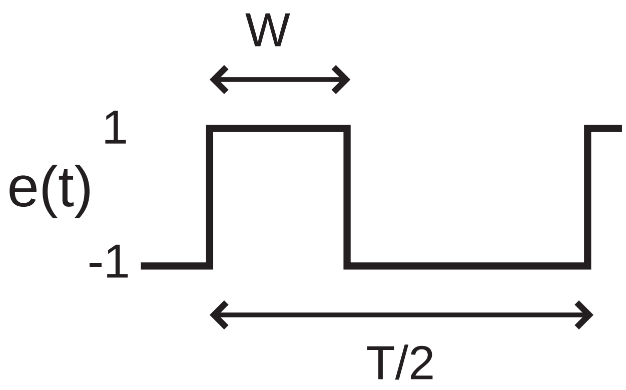
Phase Detector (PD)

- **XOR structure**
  - **Average value of error pulses corresponds to phase error**
  - **Loop filter extracts the average value and feeds to VCO**



Modeling of XOR Phase Detector

- **Average value of pulses is extracted by loop filter**
  - **Look at detector output over one cycle:**



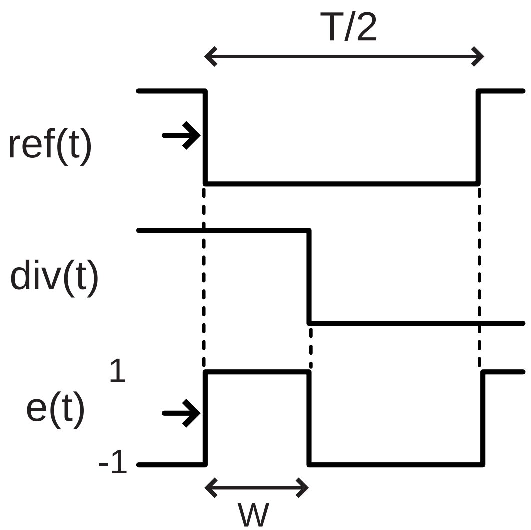
- **Equation:**

$$avg\{e(t)\} = -1 + 2\frac{W}{T/2}$$

Relate Pulse Width to Phase Error

- **Two cases:**

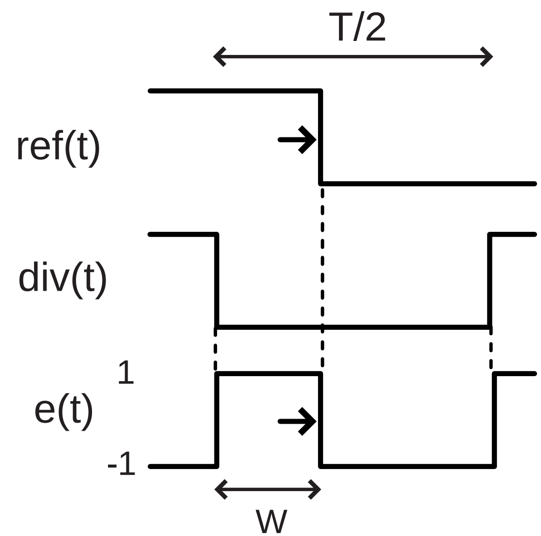
$$-\pi < \Phi_{ref} - \Phi_{div} < 0$$



$$\Downarrow$$

$$W = -\left(\frac{\Phi_{ref} - \Phi_{div}}{\pi}\right) T/2$$

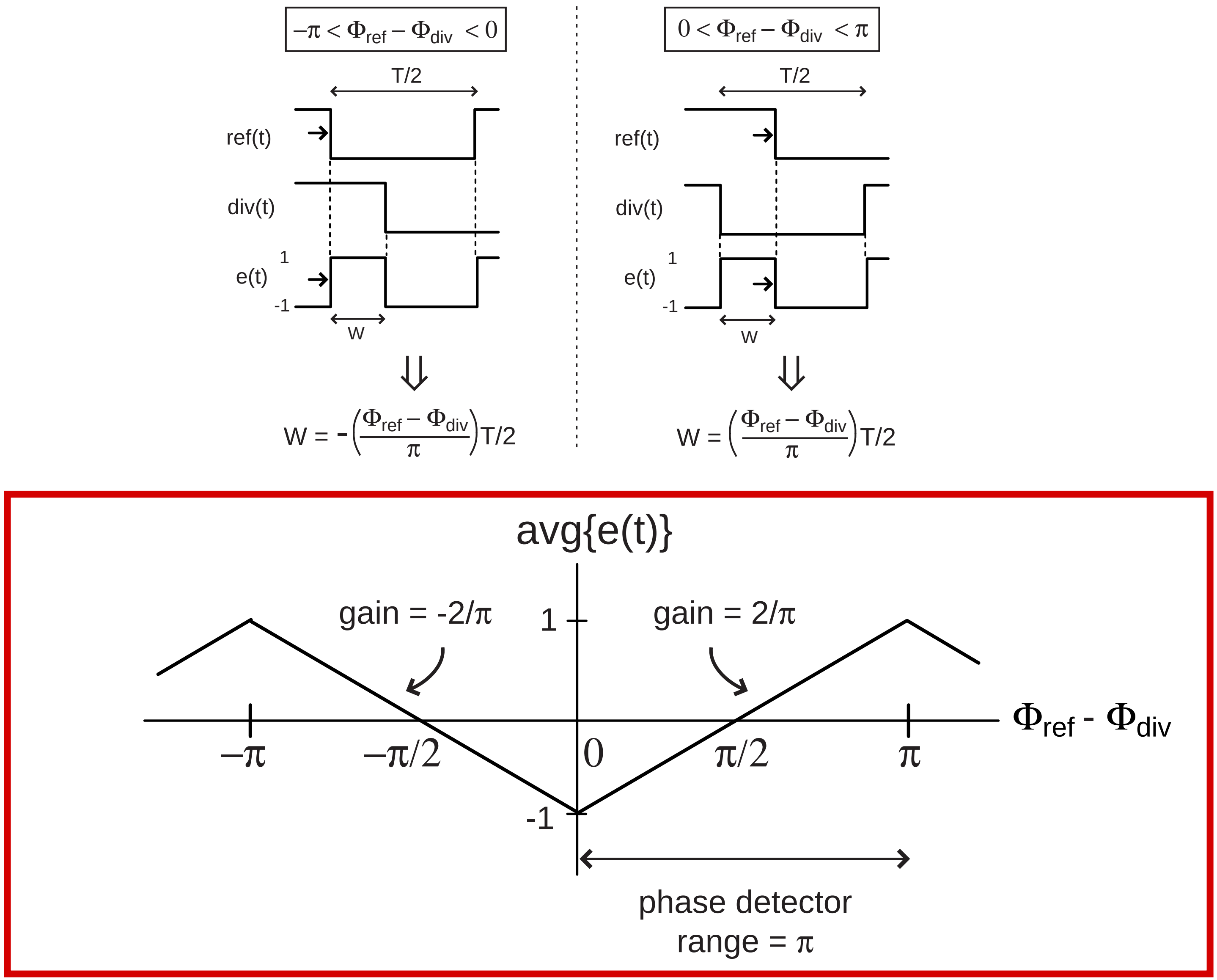
$$0 < \Phi_{ref} - \Phi_{div} < \pi$$



$$\Downarrow$$

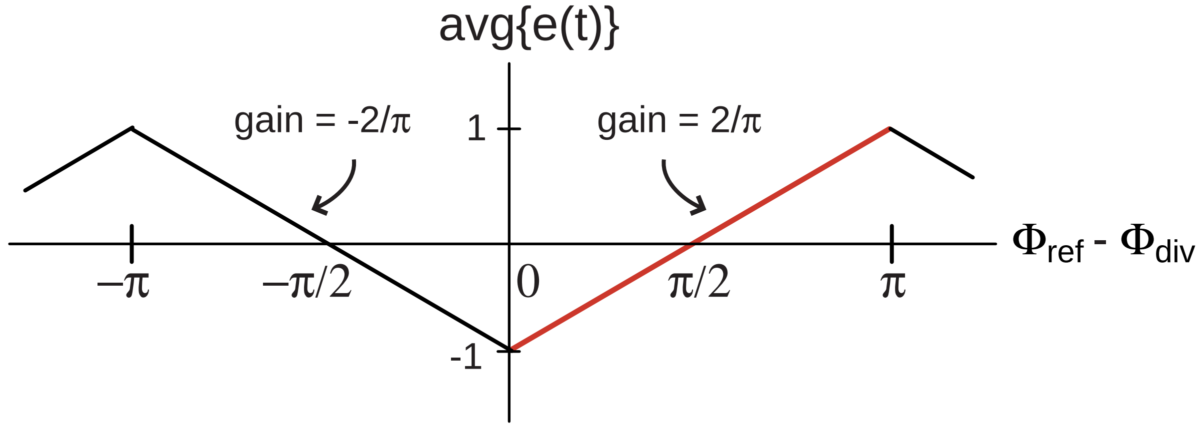
$$W = \left(\frac{\Phi_{ref} - \Phi_{div}}{\pi}\right) T/2$$

Overall XOR Phase Detector Characteristic

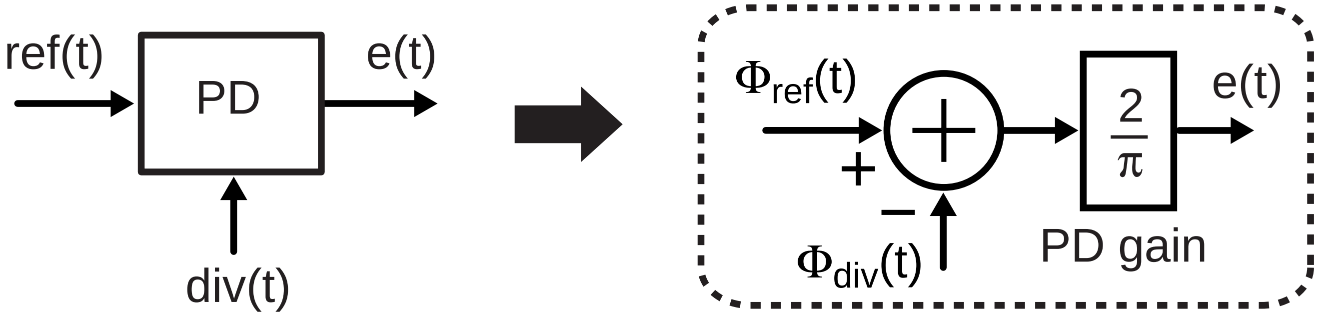


Frequency-Domain Model of XOR Phase Detector

- **Assume phase difference confined within 0 to π radians**
  - **Phase detector characteristic looks like a constant gain element**

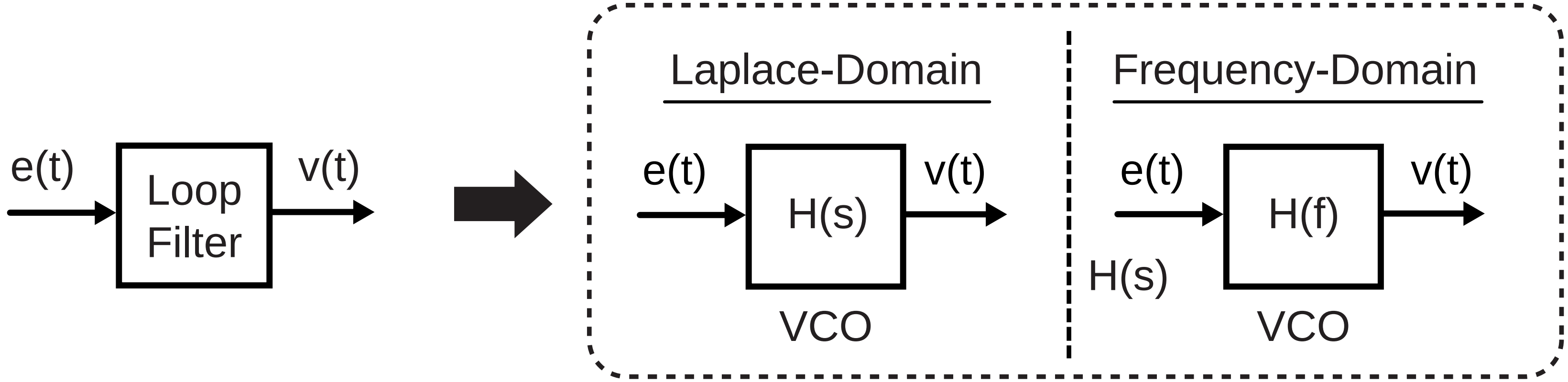


- **Corresponding frequency-domain model**

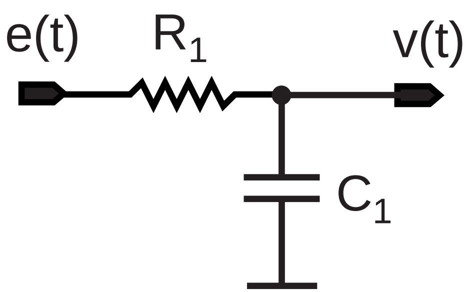


Loop Filter

- **Consists of a lowpass filter to extract average of phase detector error pulses**
- **Frequency-domain model**



- **First order example**

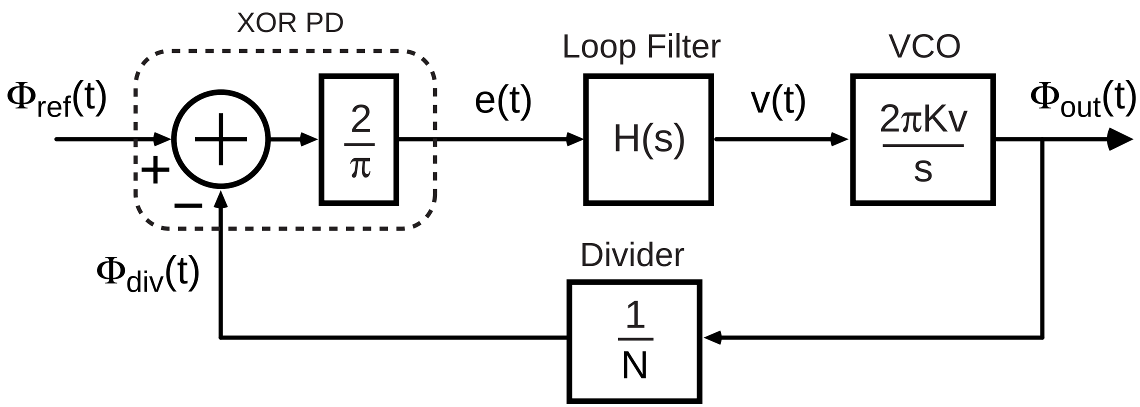


$$\Rightarrow \quad H(s) = \frac{1}{1 + sR_1C_1}$$

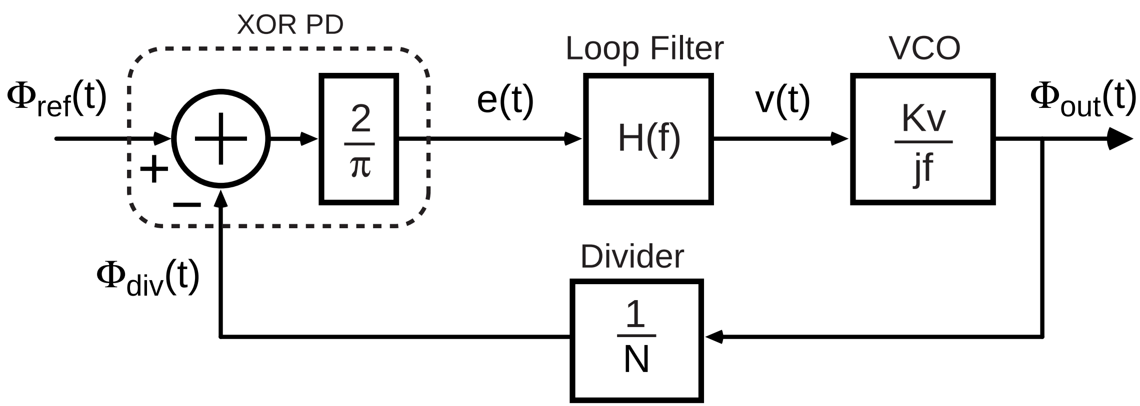
Overall Linearized PLL Frequency-Domain Model

- **Combine models of individual components**

Laplace-Domain Model

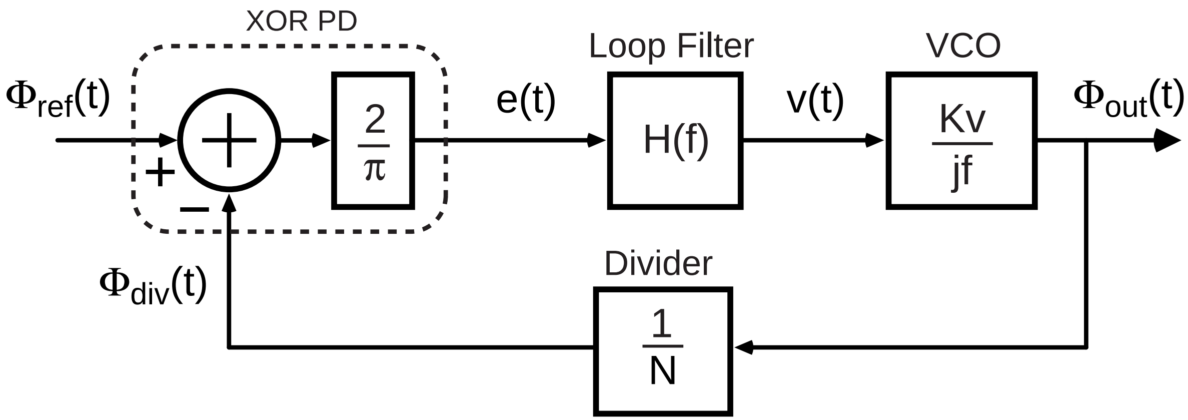


Frequency-Domain Model



Open Loop versus Closed Loop Response

- **Frequency-domain model**



- **Define A(f) as *open loop* response**

$$A(f) = \frac{2}{\pi} H(f) \left(\frac{K_v}{jf} \right) \frac{1}{N}$$

- **Define G(f) as a parameterizing *closed loop* function**
  - **More details later in this lecture**

$$G(f) = \frac{A(f)}{1 + A(f)}$$

Classical PLL Transfer Function Design Approach

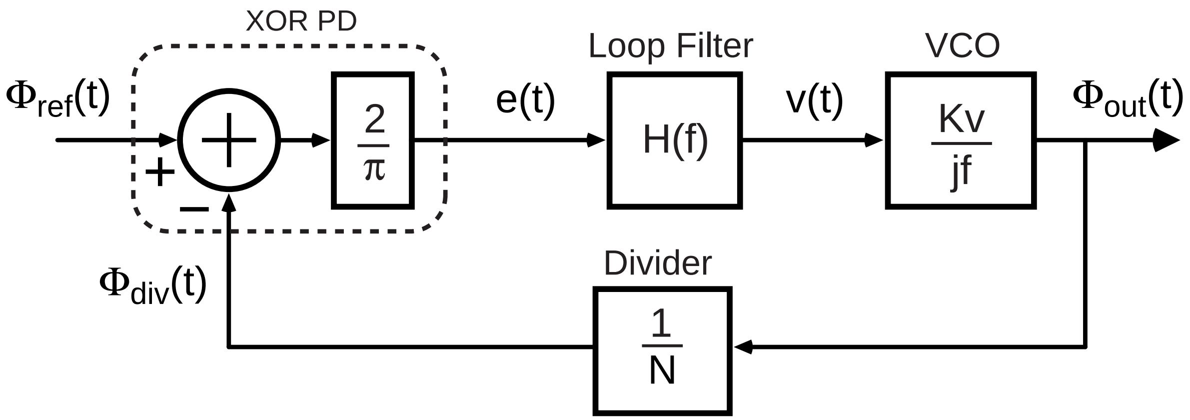
1. **Choose an appropriate topology for H(f)**
   - **Usually chosen from a small set of possibilities**

2. **Choose pole/zero values for H(f) as appropriate for the required filtering of the phase detector output**
   - **Constraint: set pole/zero locations higher than desired PLL bandwidth to allow stable dynamics to be possible**

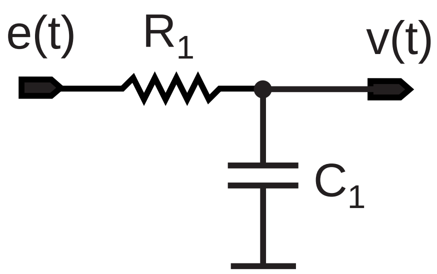
3. **Adjust the open-loop gain to achieve the required bandwidth while maintaining stability**
   - **Plot gain and phase bode plots of A(f)**
   - **Use phase (or gain) margin criterion to infer stability**

Example: First Order Loop Filter

- **Overall PLL block diagram**

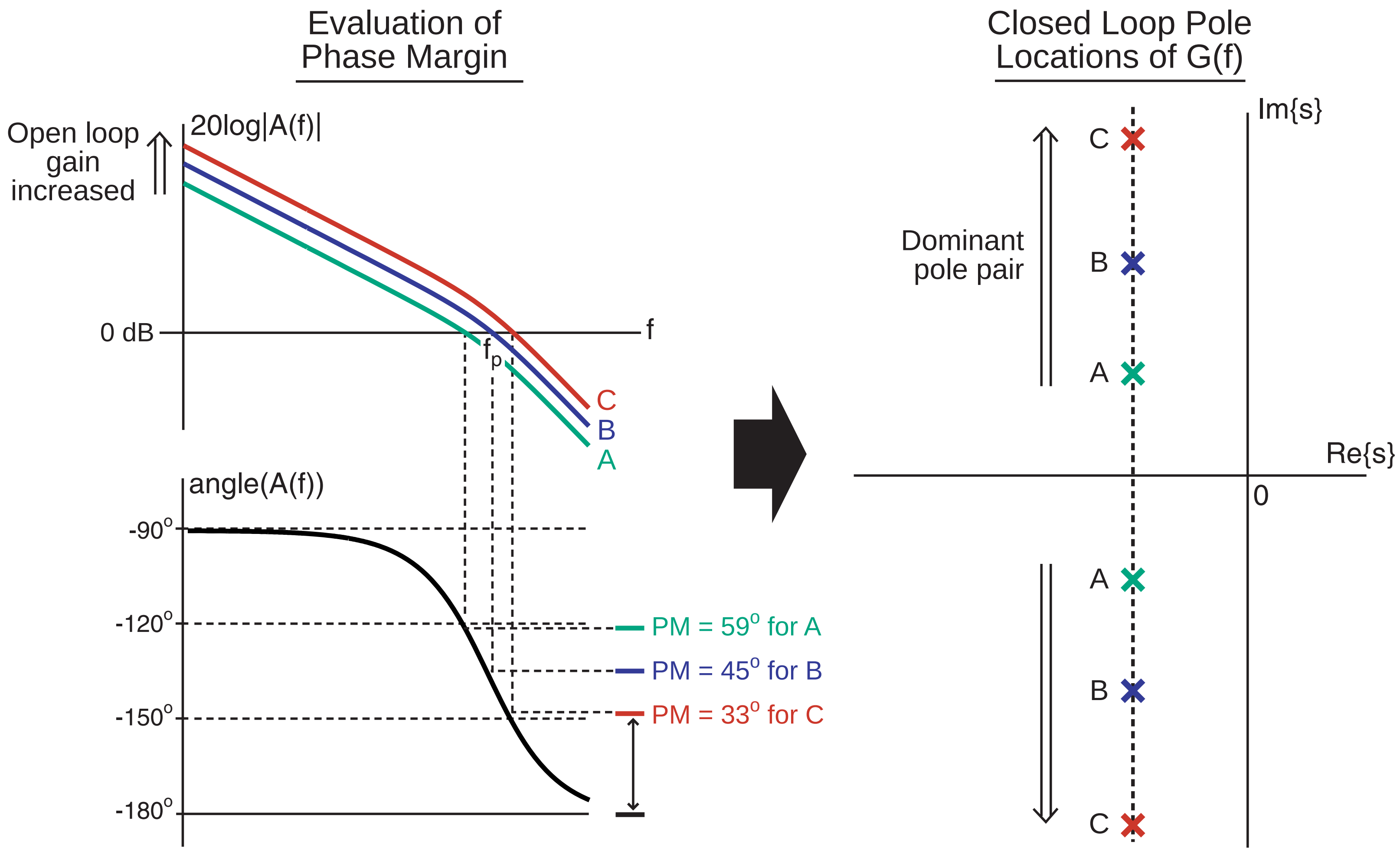


- **Loop filter**



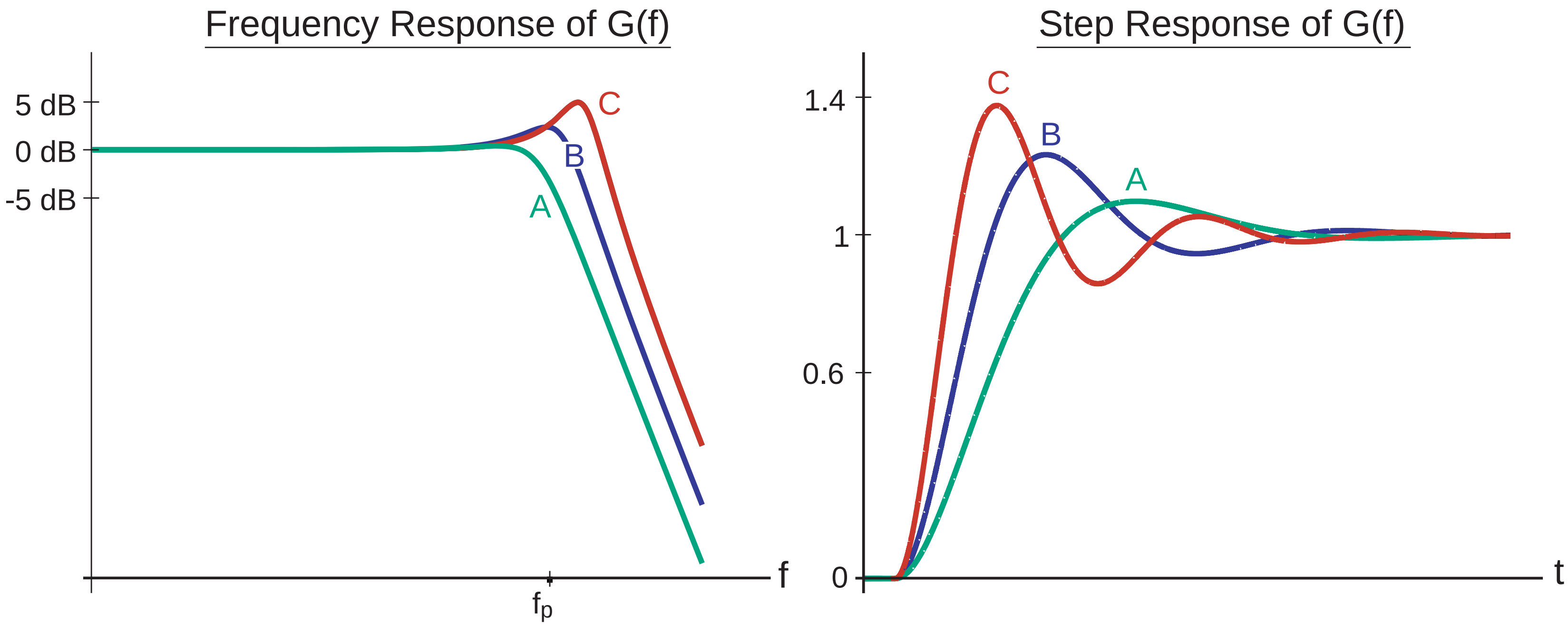
$$\Rightarrow \quad H(f) = \frac{1}{1 + jf/f_p}$$

Closed Loop Poles Versus Open Loop Gain



- **Higher open loop gain leads to an increase in Q of closed loop poles**

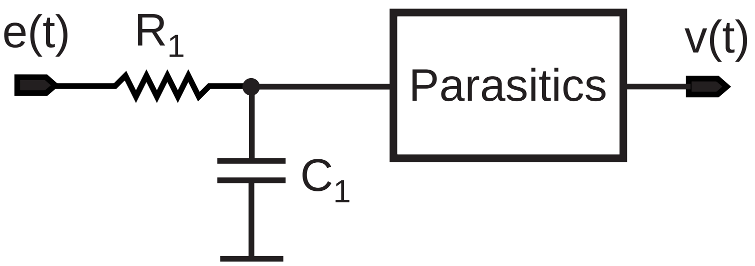
Corresponding Closed Loop Response



- **Increase in open loop gain leads to**
  - **Peaking in closed loop frequency response**
  - **Ringing in closed loop step response**

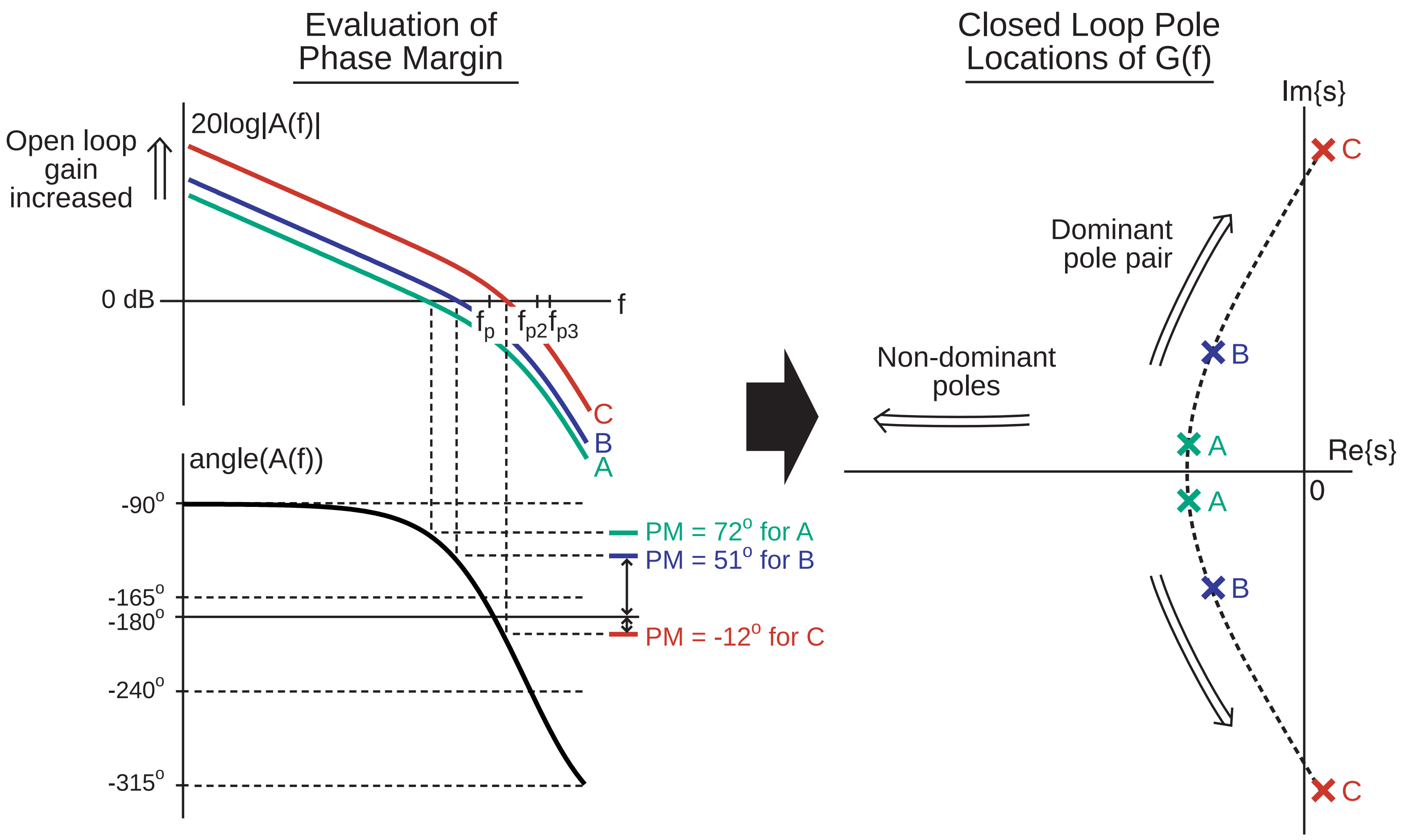
The Impact of Parasitic Poles

- **Loop filter and VCO may have additional parasitic poles and zeros due to their circuit implementation**
- **We can model such parasitics by including them in the loop filter transfer function**
- **Example: add two parasitic poles to first order filter**

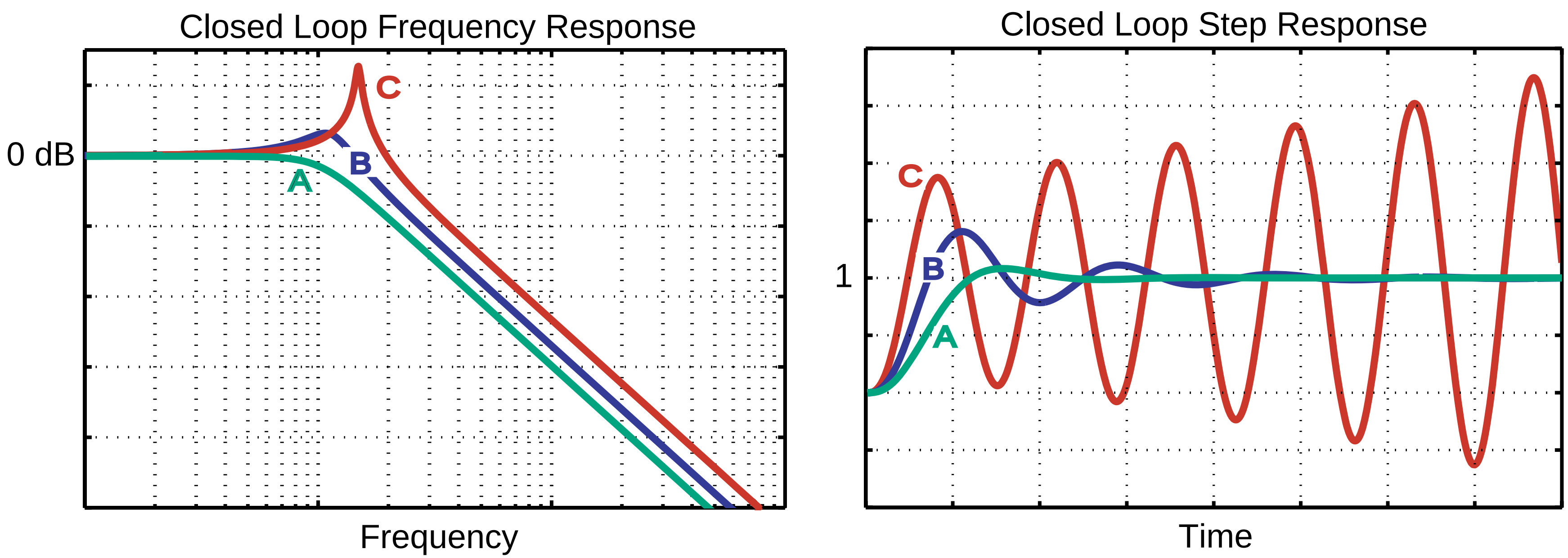


$$\Rightarrow \; H(f) = \left(\frac{1}{1+jf/f_1}\right)\left(\frac{1}{1+jf/f_2}\right)\left(\frac{1}{1+jf/f_3}\right)$$

Closed Loop Poles Versus Open Loop Gain

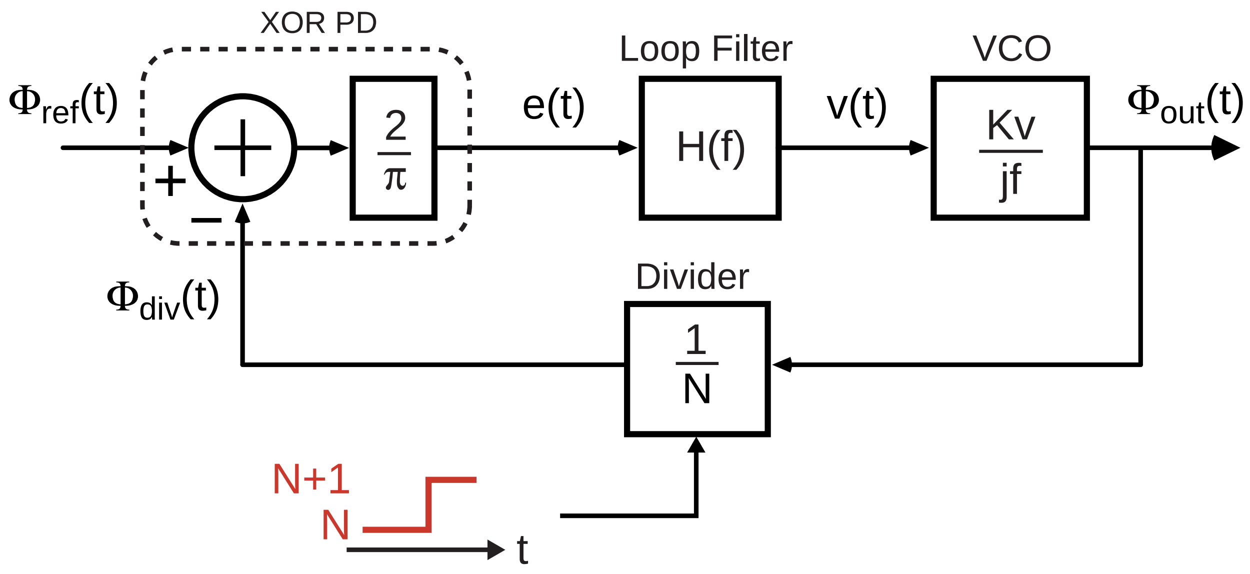


Corresponding Closed Loop Response



- **Increase in open loop gain now eventually leads to instability**
  - **Large peaking in closed loop frequency response**
  - **Increasing amplitude in closed loop step response**

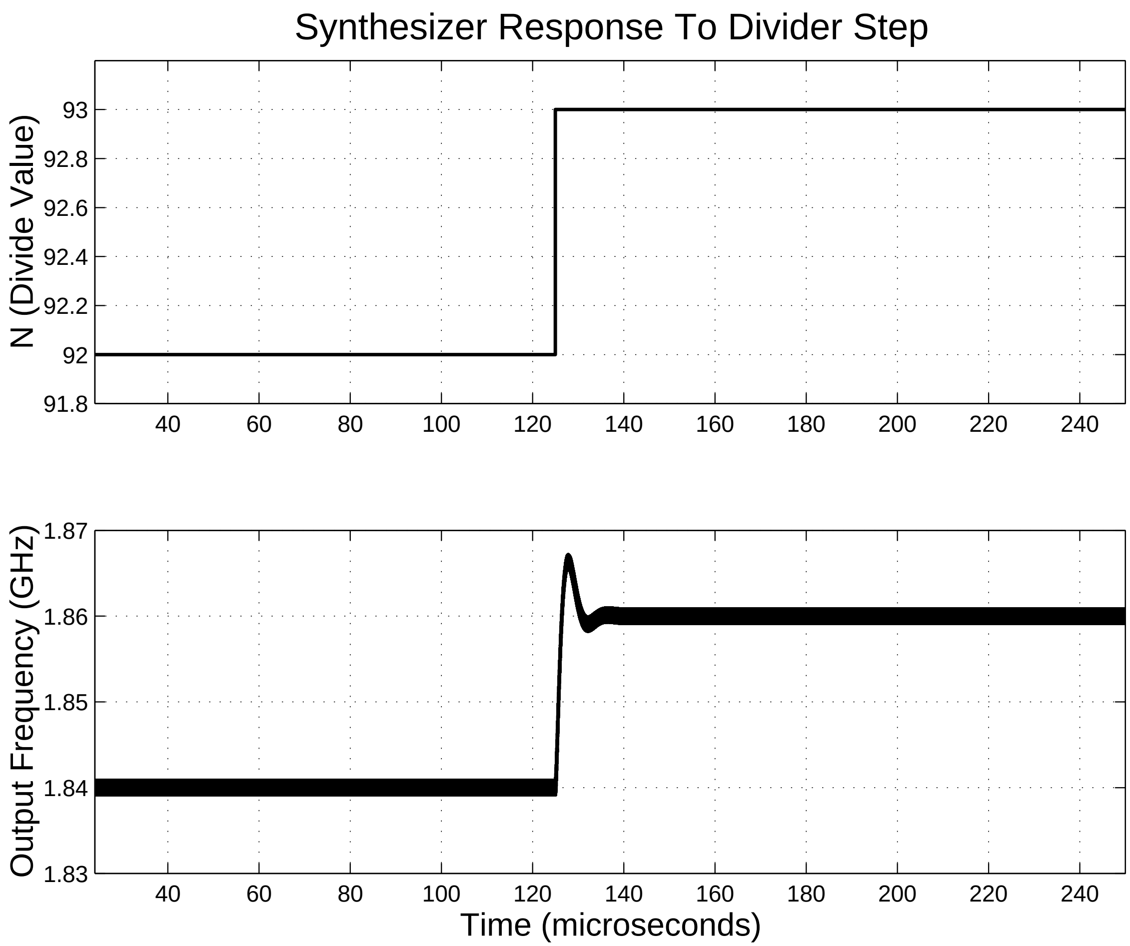
Response of PLL to Divide Value Changes



- **Change in output frequency achieved by changing the divide value**
- **Classical approach provides no direct model of impact of divide value variations**
  - **Treat divide value variation as a perturbation to a linear system**
    - PLL responds according to its closed loop response

Response of an Actual PLL to Divide Value Change

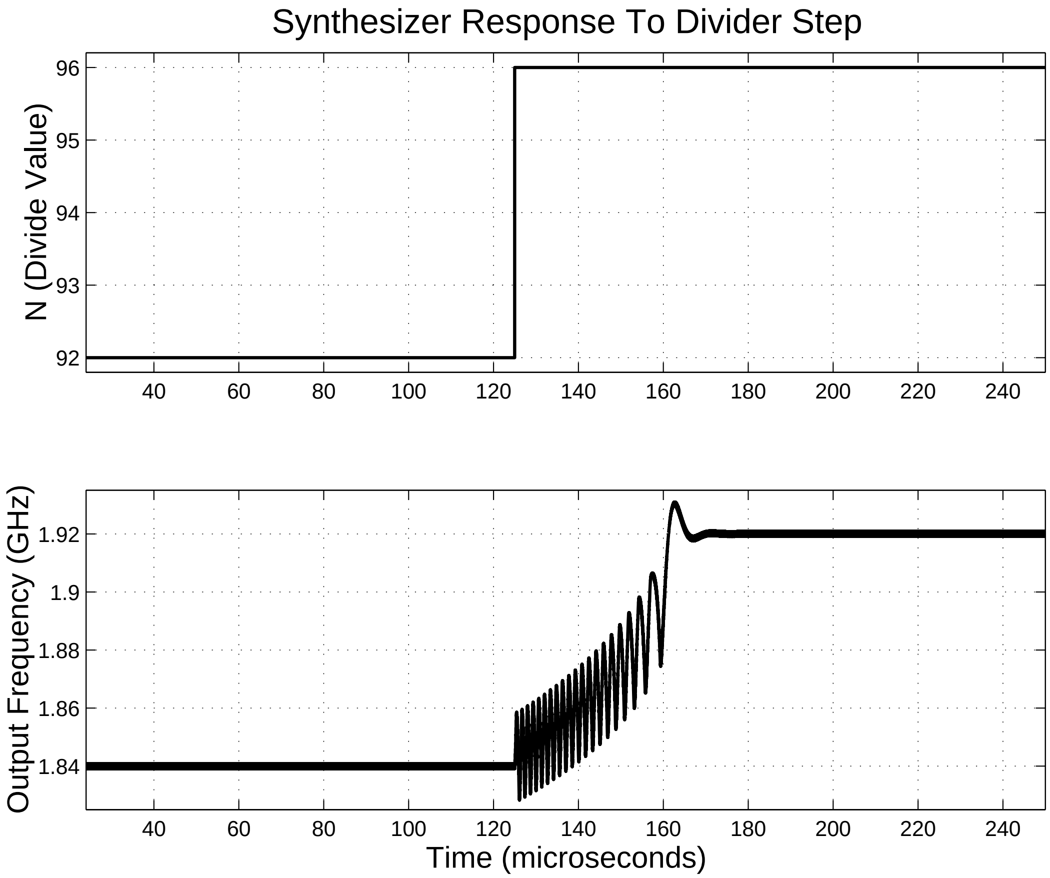
- **Example: Change divide value by one**



  - **PLL responds according to closed loop response!**

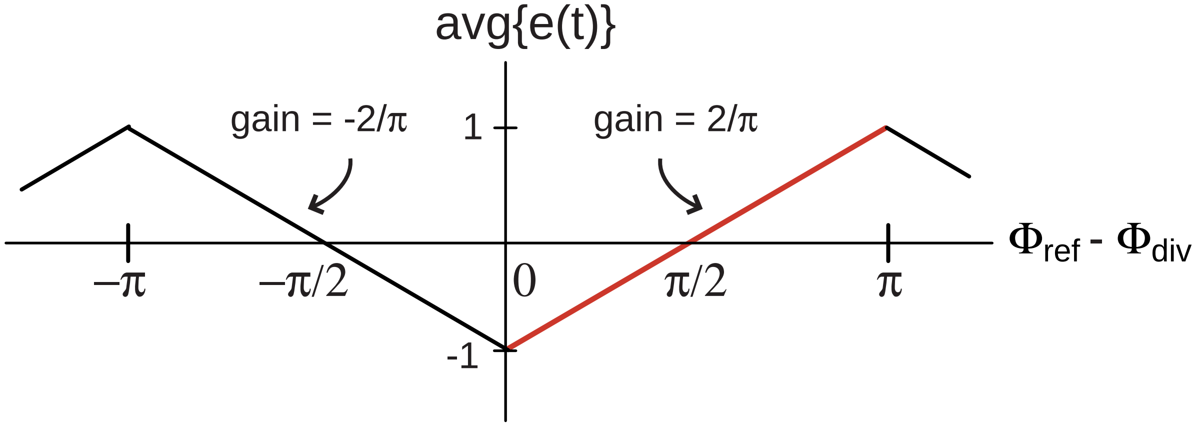
What Happens with Large Divide Value Variations?

- **PLL temporarily loses frequency lock (cycle slipping occurs)**



  - **Why does this happen?**

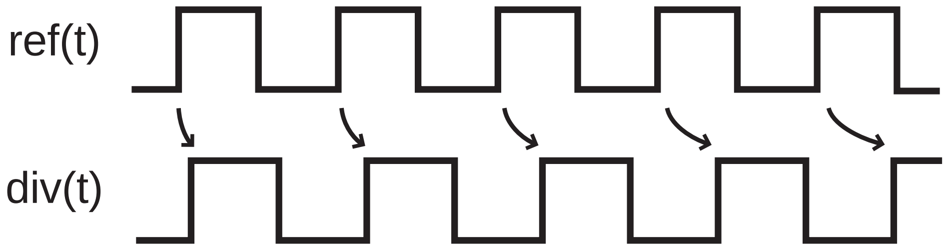
Recall Phase Detector Characteristic



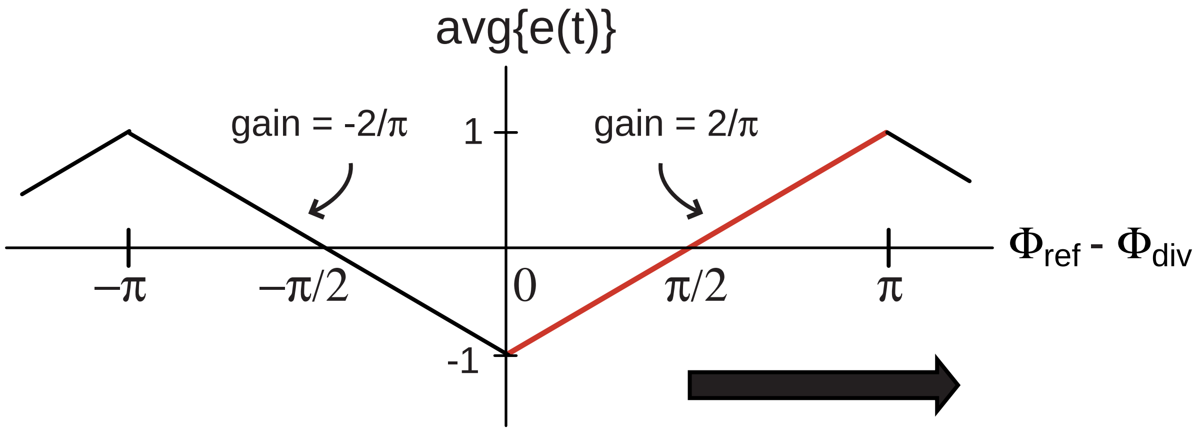
- To simplify modeling, we assumed that we always operated in a confined phase range (0 to π)
  - Led to a simple PD model
- Large perturbations knock us out of that confined phase range
  - PD behavior varies depending on the phase range it happens to be in

Cycle Slipping

- **Consider the case where there is a frequency offset between divider output and reference**
  - **We know that phase difference will accumulate**

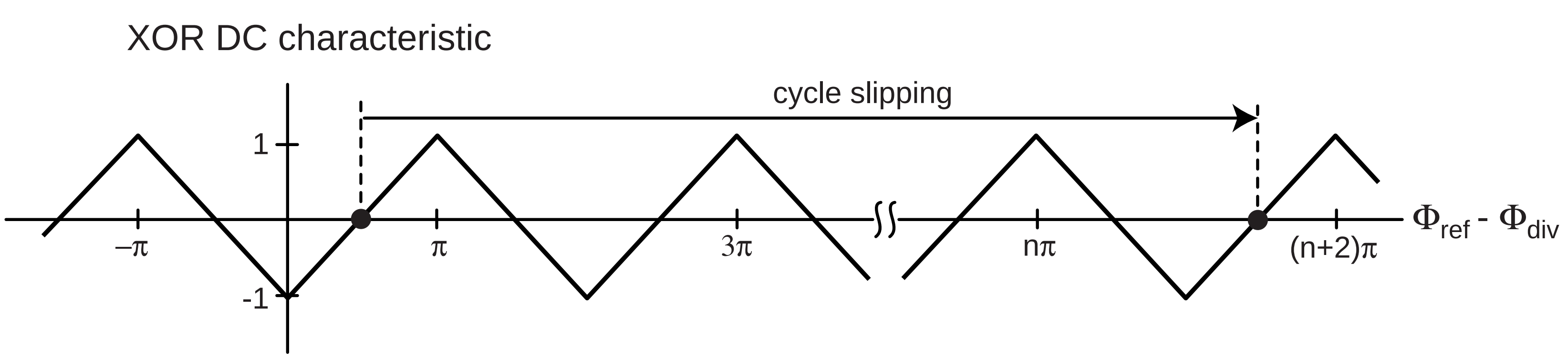


- **Resulting ramp in phase causes PD characteristic to be swept across its different regions (cycle slipping)**



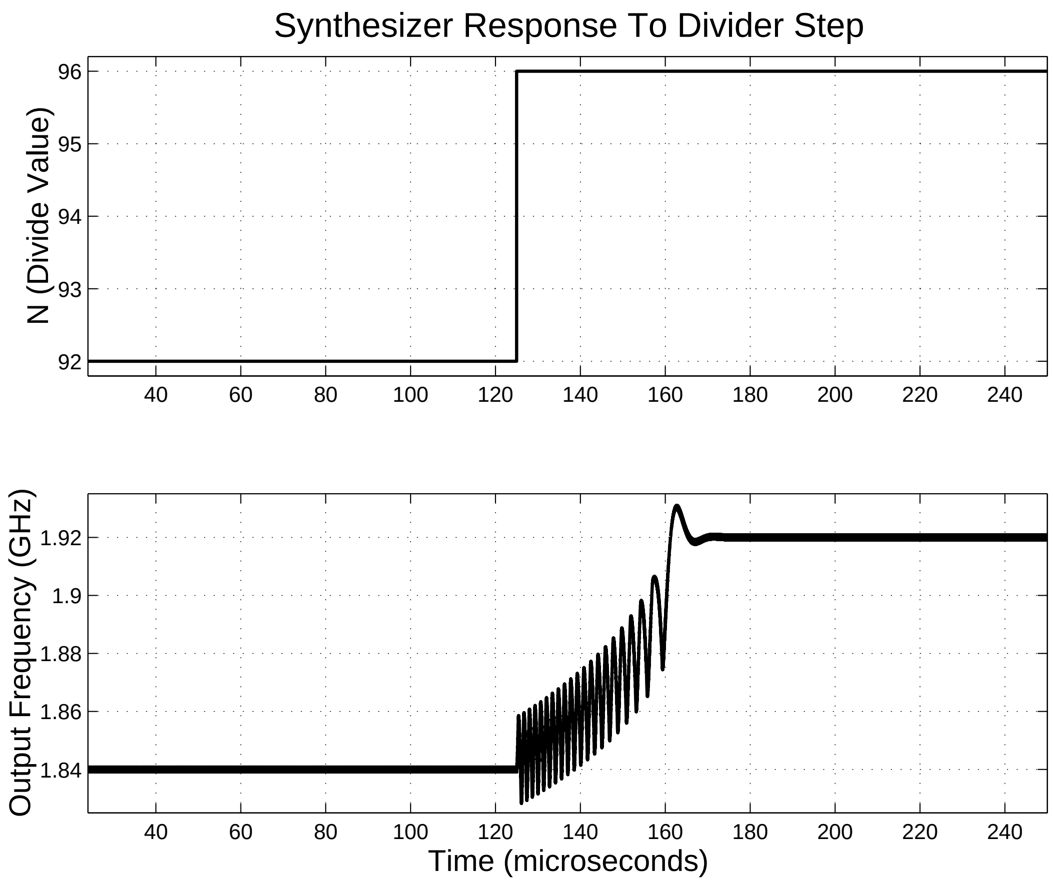
Impact of Cycle Slipping

- **Loop filter averages out phase detector output**
- **Severe cycle slipping causes phase detector to alternate between regions very quickly**
  - **Average value of XOR characteristic can be close to zero**
  - **PLL frequency oscillates according to cycle slipping**
  - **In severe cases, PLL will not re-lock**
    - PLL has finite frequency lock-in range!



Back to PLL Response Shown Previously

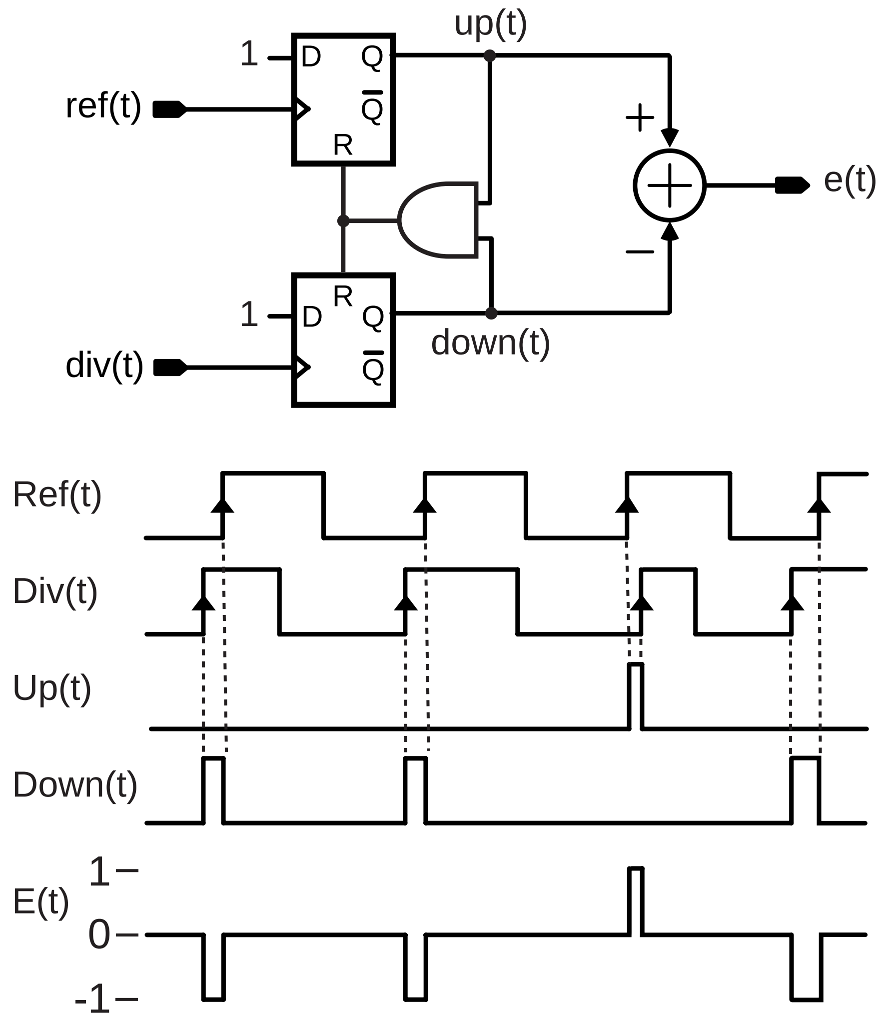
- **PLL output frequency indeed oscillates**
  - **Eventually locks when frequency difference is small enough**



  - **How do we extend the frequency lock-in range?**

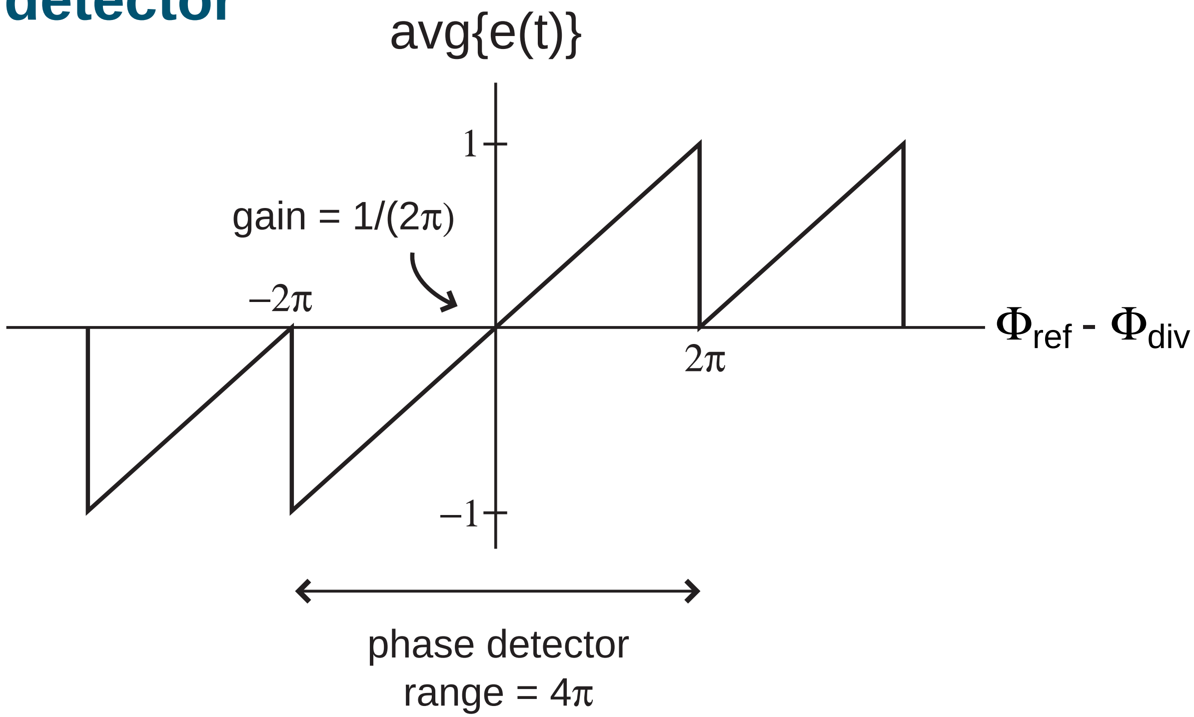
Phase Frequency Detectors (PFD)

- **Example: Tristate PFD**



Tristate PFD Characteristic

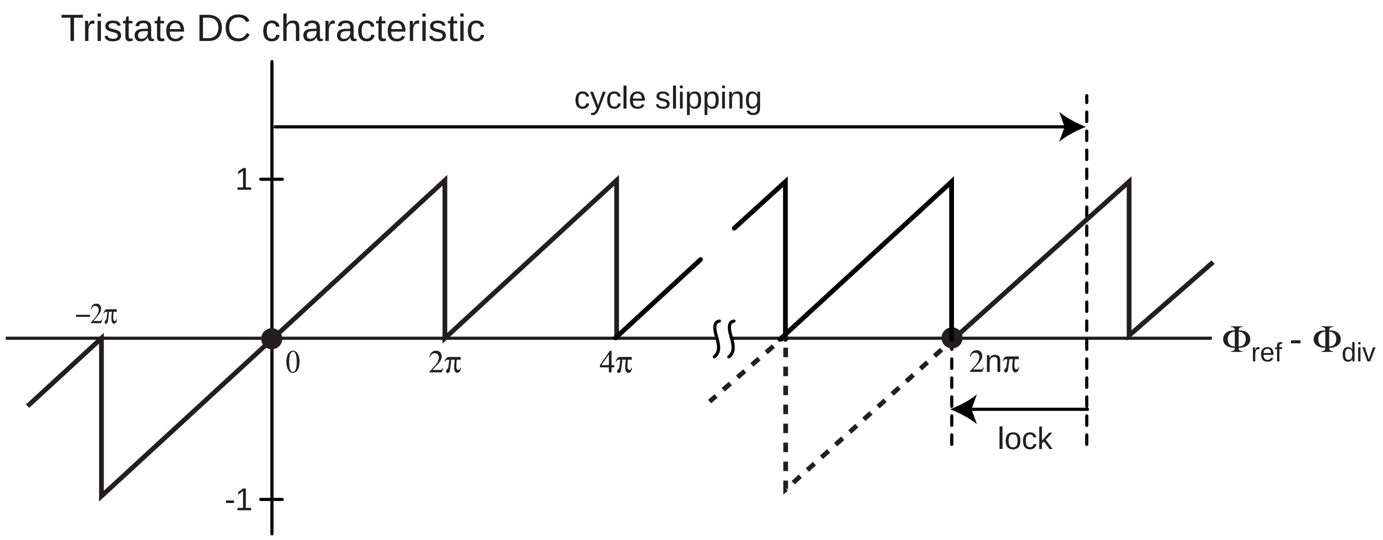
- **Calculate using similar approach as used for XOR phase detector**



- **Note that phase error characteristic is asymmetric about zero phase**
  - **Key attribute for enabling frequency detection**

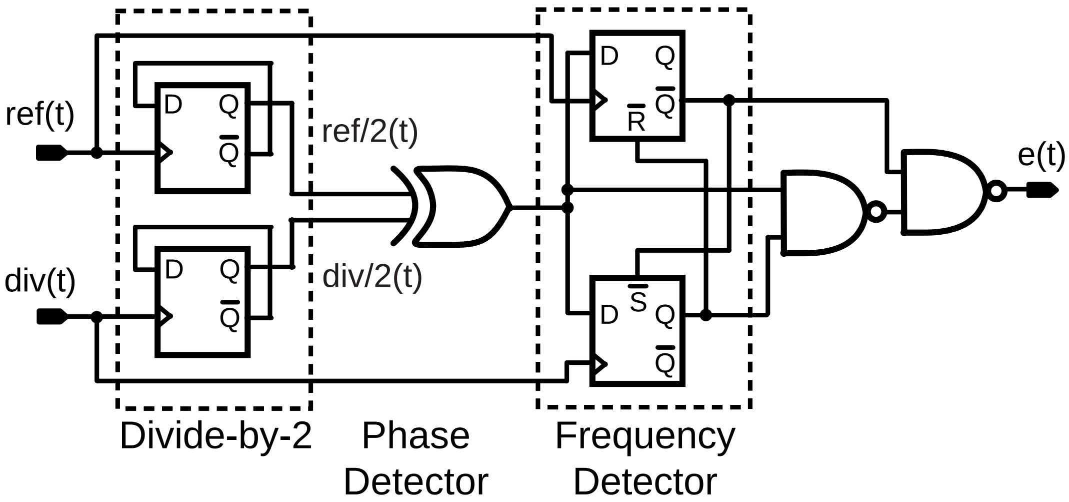
PFD Enables PLL to Always Regain Frequency Lock

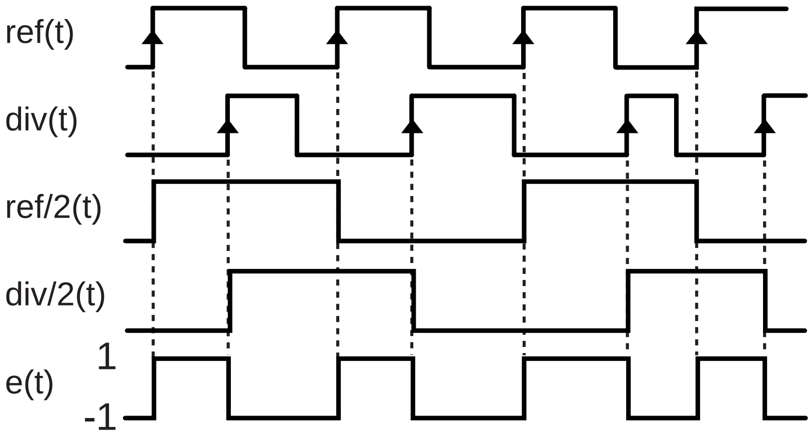
- **Asymmetric phase error characteristic allows positive frequency differences to be distinguished from negative frequency differences**
  - **Average value is now positive or negative according to sign of frequency offset**
  - **PLL will always relock**



Another PFD Structure

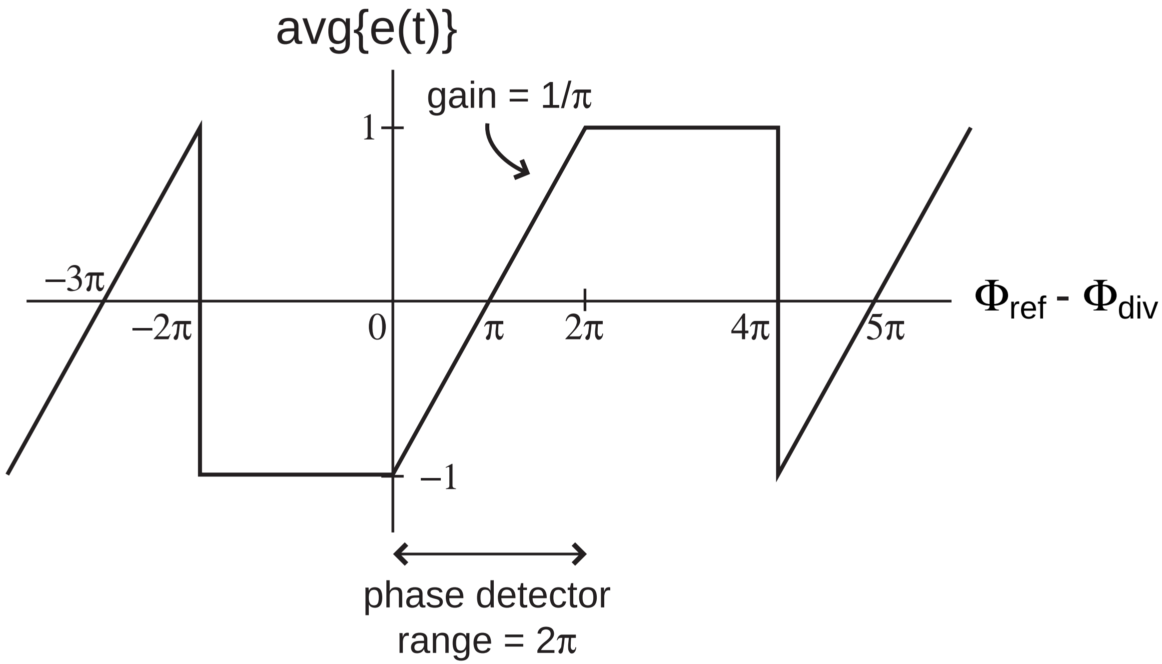
- **XOR-based PFD**





XOR-based PFD Characteristic

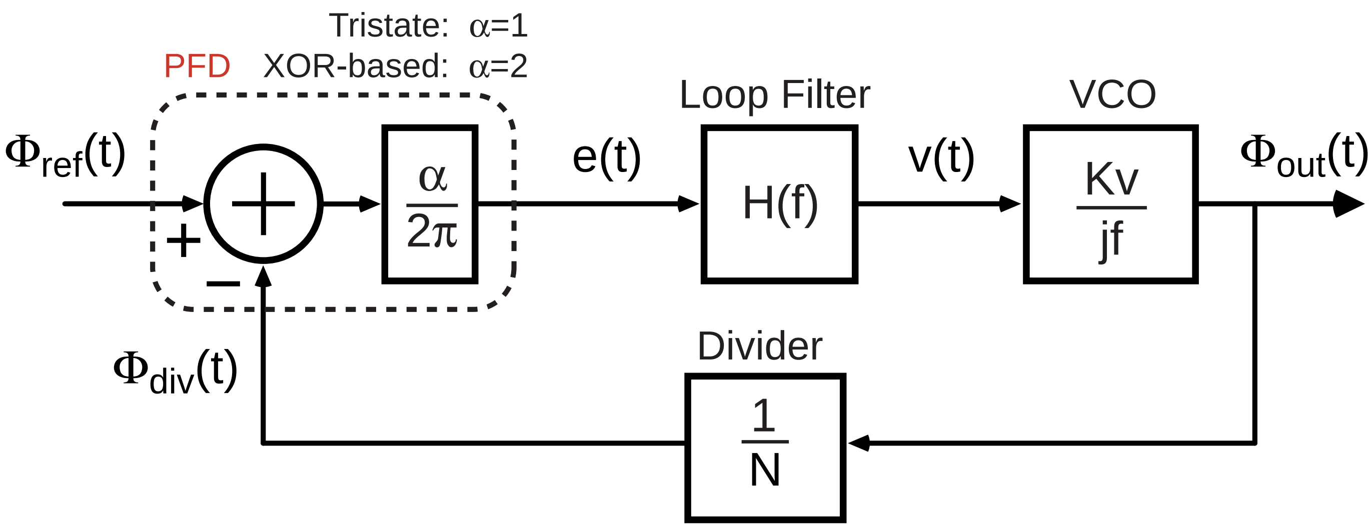
- **Calculate using similar approach as used for XOR phase detector**



- **Phase error characteristic asymmetric about zero phase**
  - **Average value of phase error is positive or negative during cycle slipping depending on sign of frequency error**

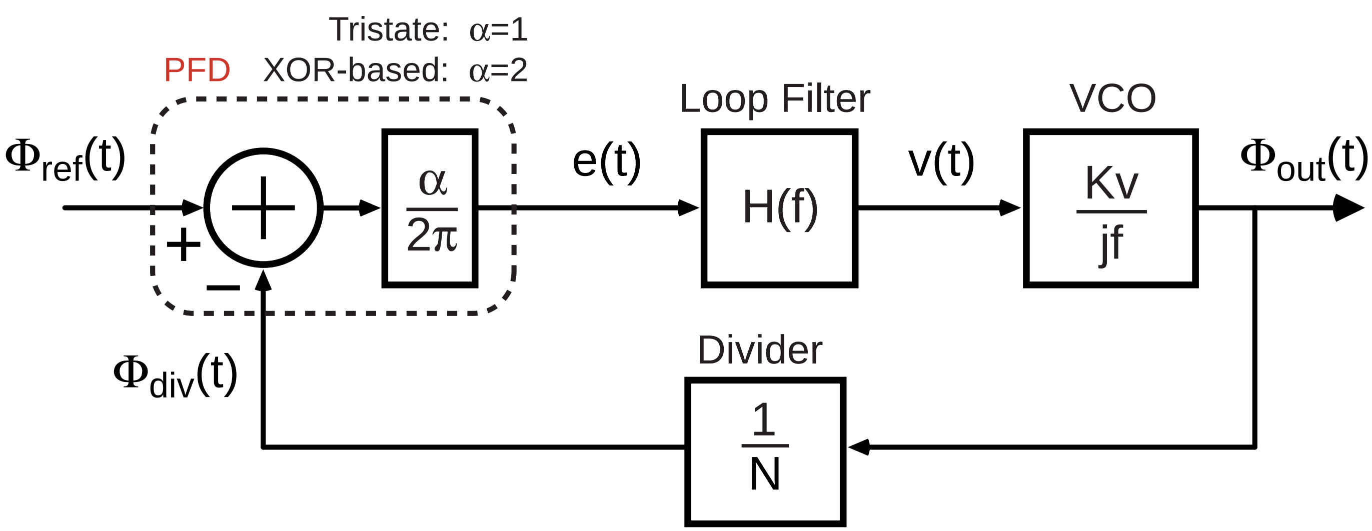
Linearized PLL Model With PFD Structures

- Assume that when PLL in lock, phase variations are within the linear range of PFD
  - Simulate impact of cycle slipping if desired (do not include its effect in model)
- Same frequency-domain PLL model as before, but PFD gain depends on topology used



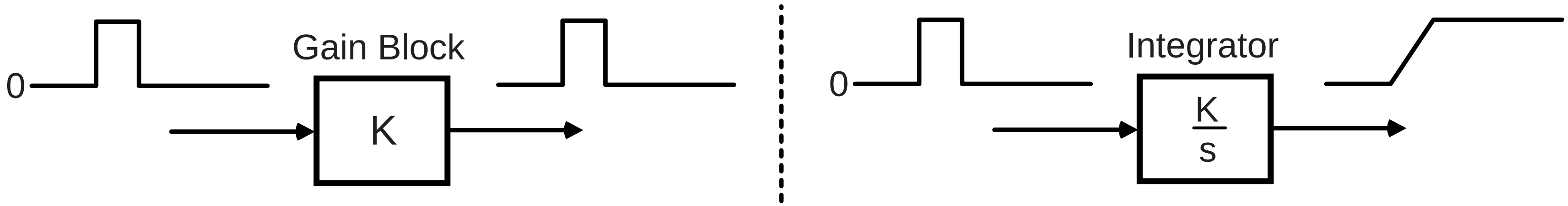
Type I versus Type II PLL Implementations

- **Type I: one integrator in PLL open loop transfer function**
  - **VCO adds on integrator**
  - **Loop filter, H(f), has no integrators**
- **Type II: two integrators in PLL open loop transfer function**
  - **Loop filter, H(f), has one integrator**

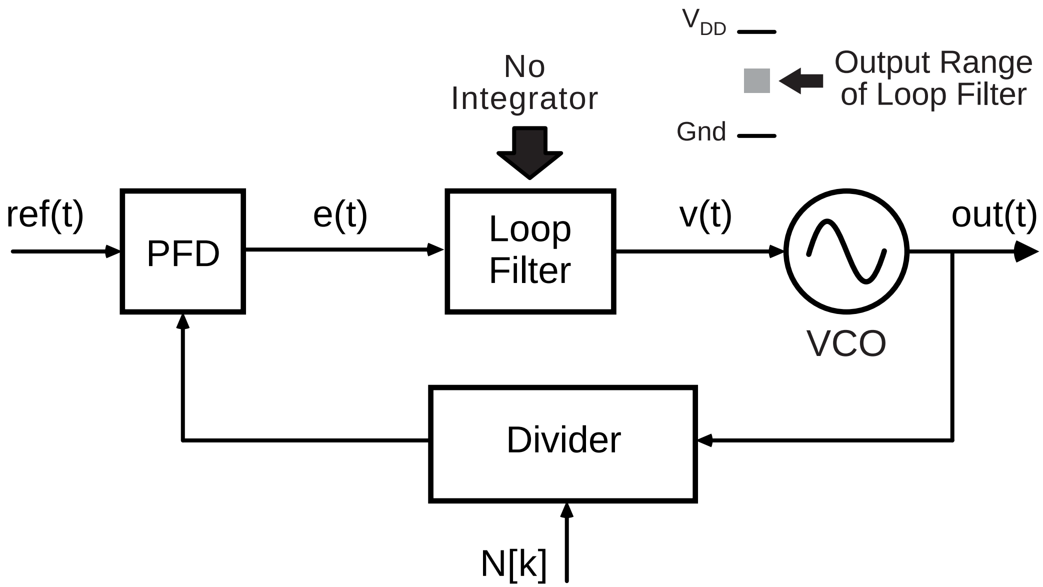


VCO Input Range Issue for Type I PLL Implementations

- **DC output range of gain block versus integrator**

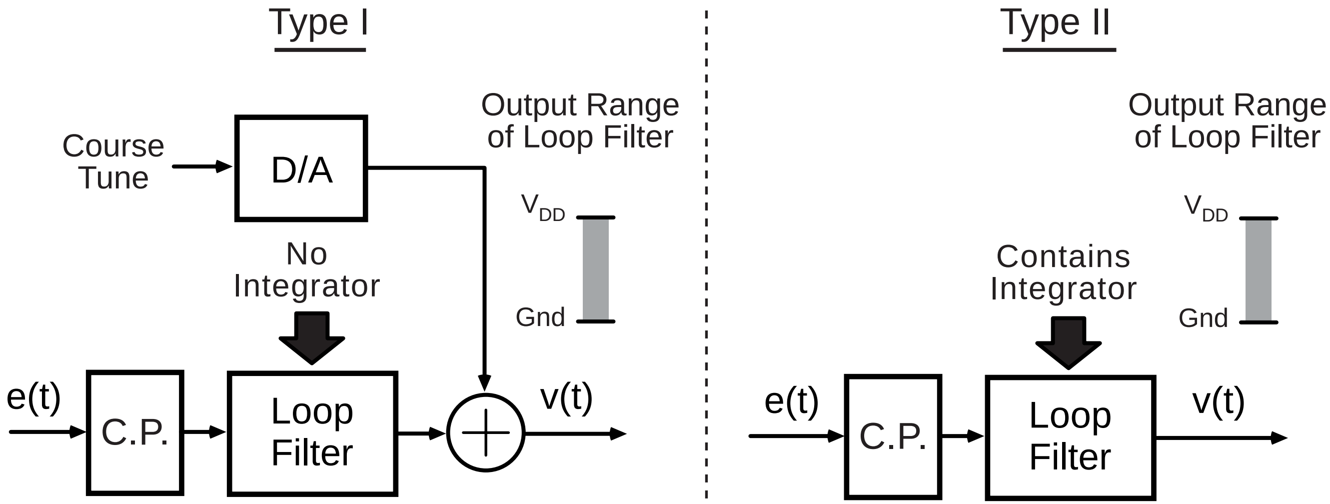


- **Issue: DC gain of loop filter often small and PFD output range is limited**
  - **Loop filter output fails to cover full input range of VCO**



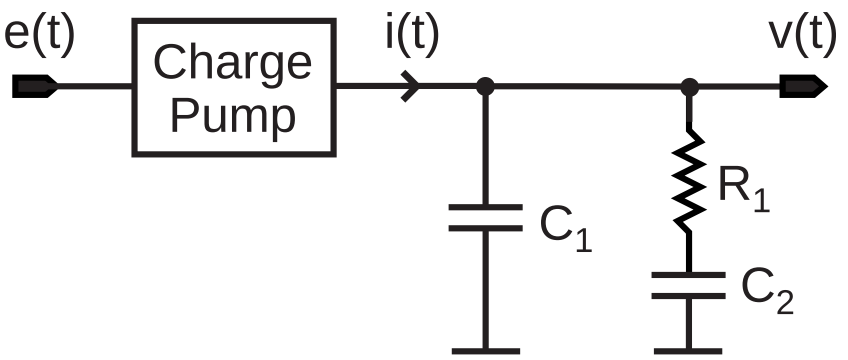
Options for Achieving Full Range Span of VCO

- **Type I**
  - **Add a D/A converter to provide coarse tuning**
    - Adds power and complexity
    - Steady-state phase error inconsistently set
- **Type II**
  - **Integrator automatically provides DC level shifting**
    - Low power and simple implementation
    - Steady-state phase error always set to zero



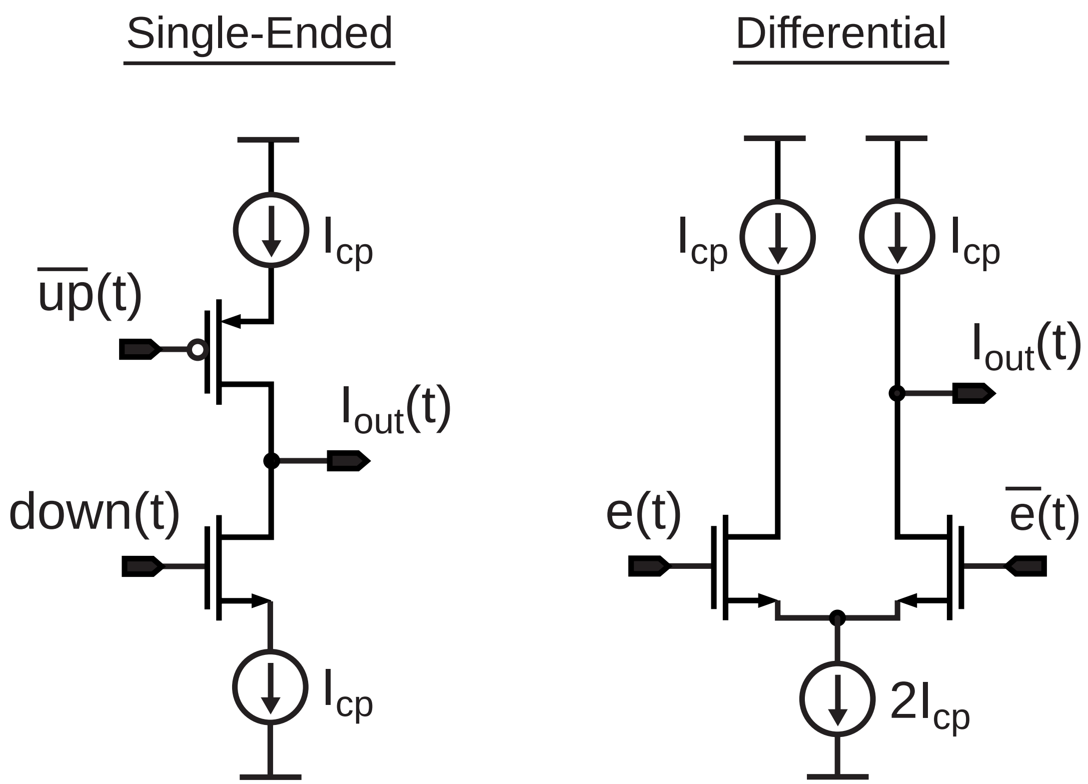
A Common Loop Filter for Type II PLL Implementation

- **Use a charge pump to create the integrator**
  - **Current onto a capacitor forms integrator**
  - **Add extra pole/zero using resistor and capacitor**
- **Gain of loop filter can be adjusted according to the value of the charge pump current**
- **Example: lead/lag network**



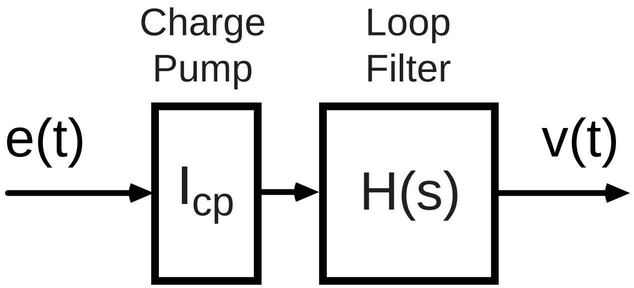
Charge Pump Implementations

- **Switch currents in and out:**



Modeling of Loop Filter/Charge Pump

- **Charge pump is gain element**
- **Loop filter forms transfer function**



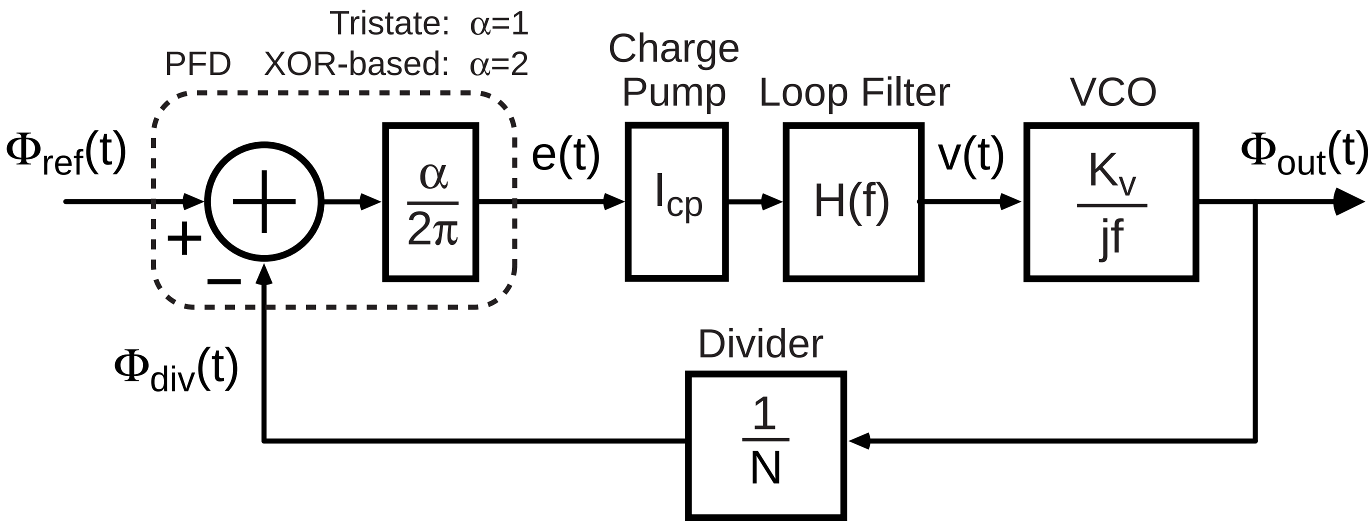
- **Example: lead/lag network from previous slide**

$$H(f) = \left(\frac{1}{sC_{sum}}\right)\frac{1 + jf/f_z}{1 + jf/f_p}$$

$$C_{sum} = C_1 + C_2, \quad f_z = \frac{1}{2\pi R_1 C_2}, \quad f_p = \frac{C_1 + C_2}{2\pi R_1 C_1 C_2}$$

PLL Design with Lead/Lag Filter

- Overall PLL block diagram

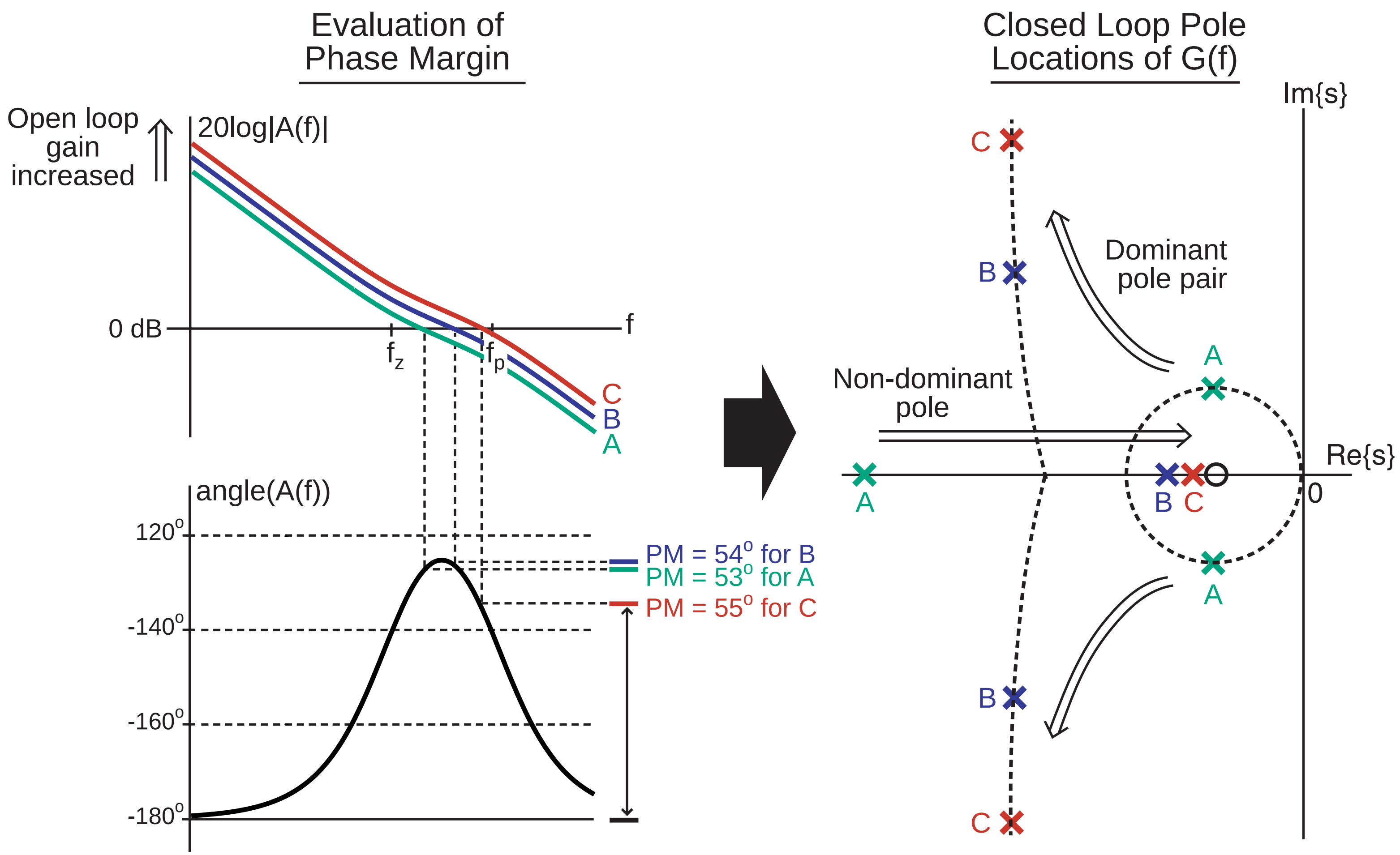


- Loop filter

$$H(f) = \left(\frac{1}{sC_{sum}}\right)\frac{1 + jf/f_z}{1 + jf/f_p}$$

- Set open loop gain to achieve adequate phase margin
  - Set f_z lower than and f_p higher than desired PLL bandwidth

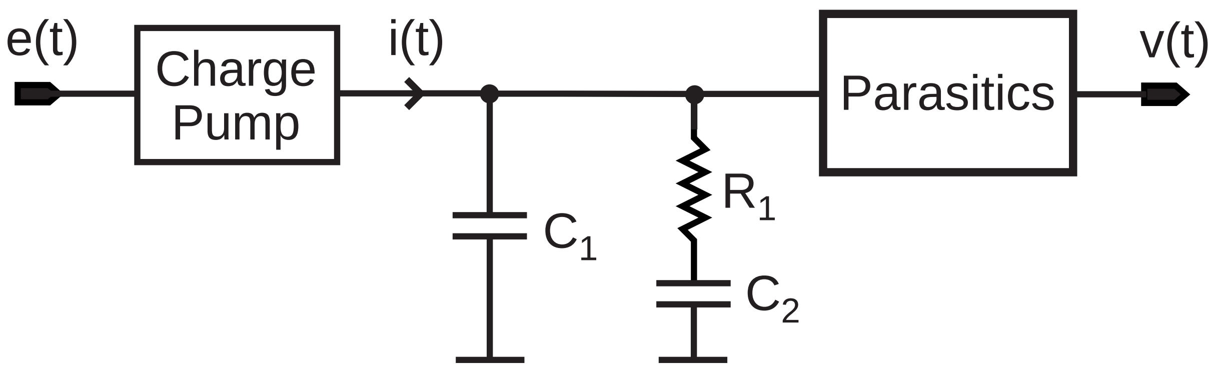
Closed Loop Poles Versus Open Loop Gain



- **Open loop gain cannot be too low or too high if reasonable phase margin is desired**

Impact of Parasitics When Lead/Lag Filter Used

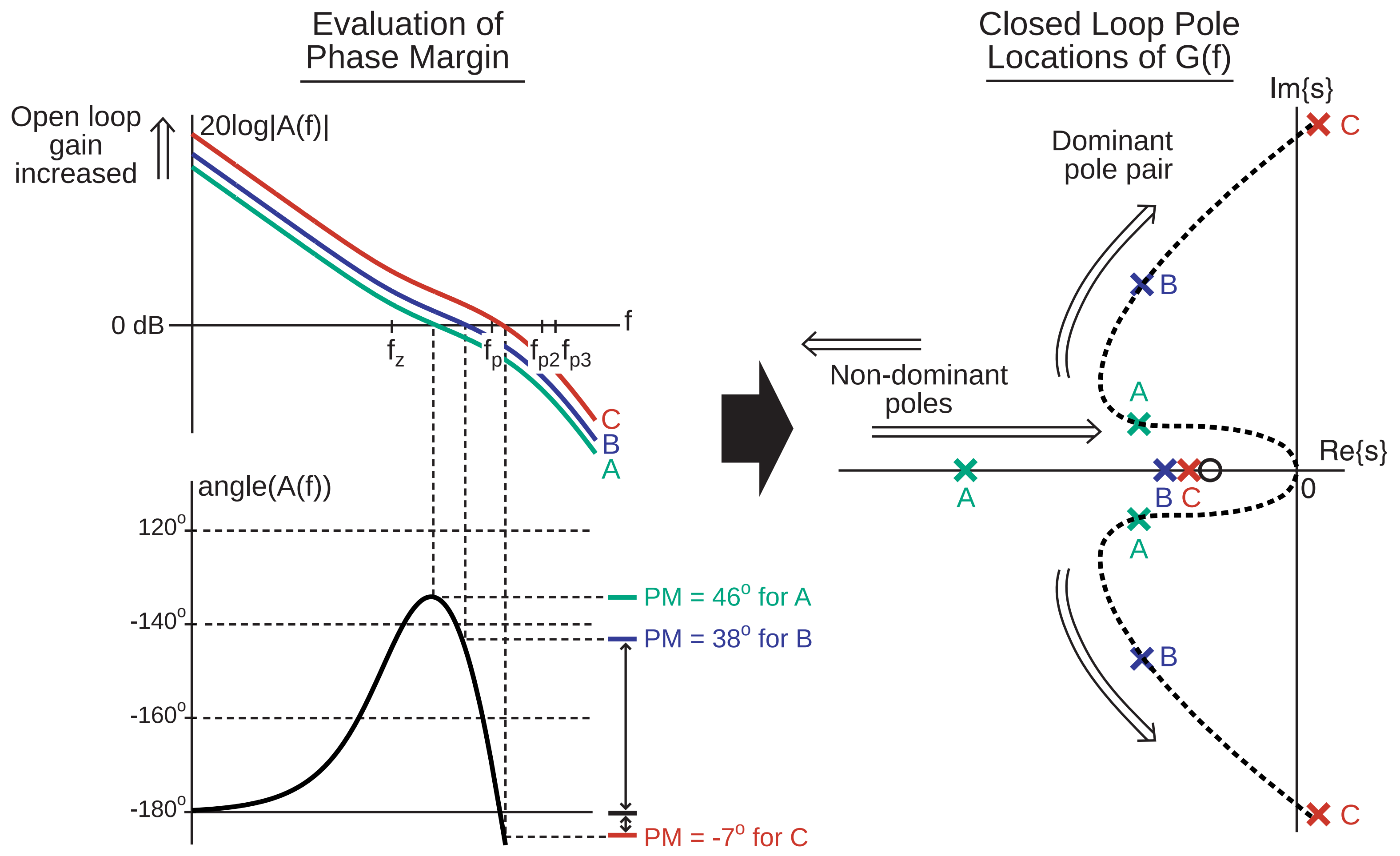
- **We can again model impact of parasitics by including them in loop filter transfer function**



- **Example: include two parasitic poles with the lead/lag transfer function**

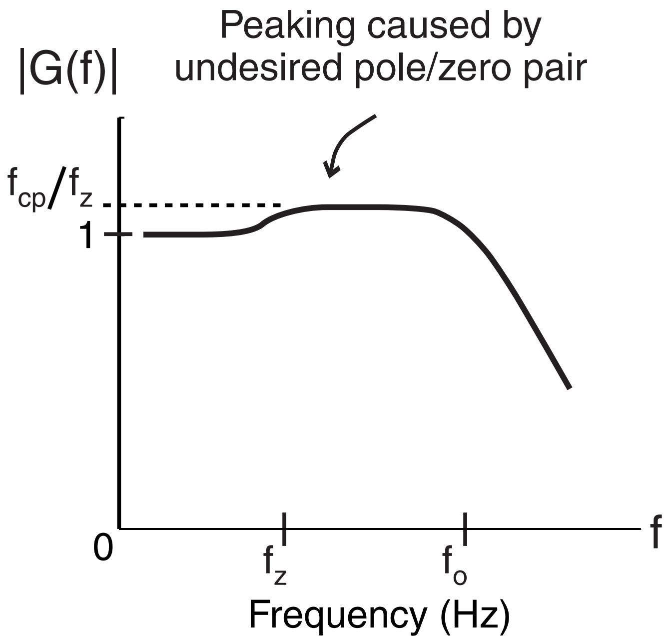
$$H(f) = \left(\frac{1}{sC_{sum}}\right)\frac{1 + jf/f_z}{1 + jf/f_p}\left(\frac{1}{1 + jf/f_{p2}}\right)\left(\frac{1}{1 + jf/f_{p3}}\right)$$

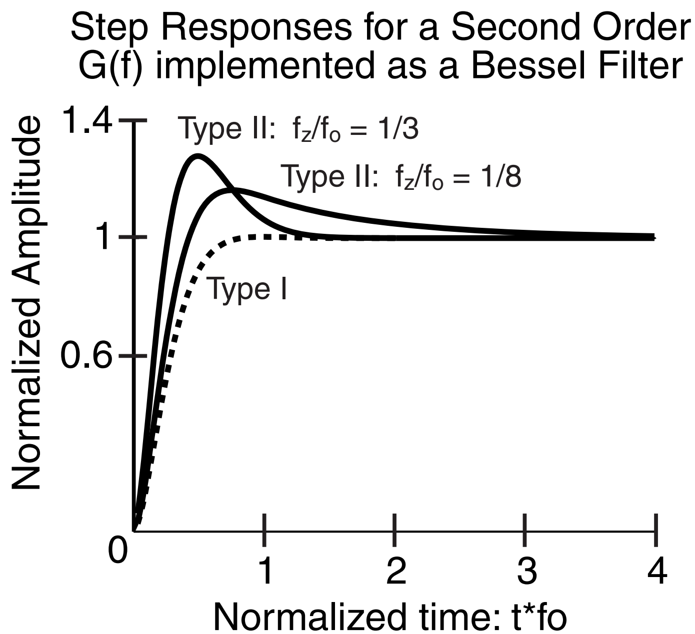
Closed Loop Poles Versus Open Loop Gain



- **Closed loop response becomes unstable if open loop gain is too high**

Negative Issues For Type II PLL Implementations





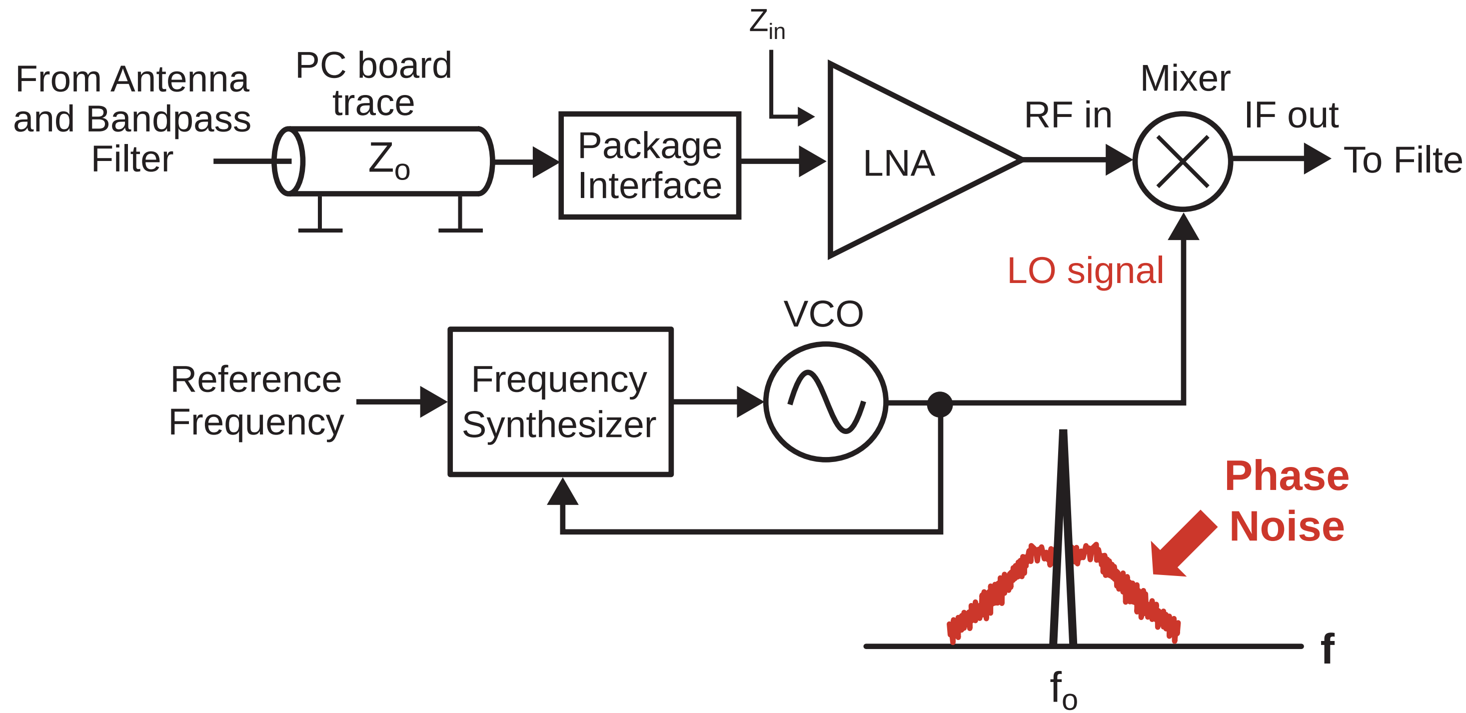
- **Parasitic pole/zero pair causes**
  - **Peaking in the closed loop frequency response**
    - A big issue for CDR systems, but not too bad for wireless
  - **Extended settling time due to parasitic "tail" response**
    - Bad for wireless systems demanding fast settling time

Summary of Integer-N Dynamic Modeling

- **Linearized models can be derived for each PLL block**
  - **Resulting transfer function model of PLL is accurate for small perturbations in PLL**
  - **Linear PLL model breaks down for large perturbations on PLL, such as a large step change in frequency**
    - Cycle slipping is key nonlinear effect
- **Key issues for designing PLL are**
  - **Achieve stable operation with desired bandwidth**
  - **Allow full range of VCO with a simple implementation**
    - Type II PLL is very popular to achieve this

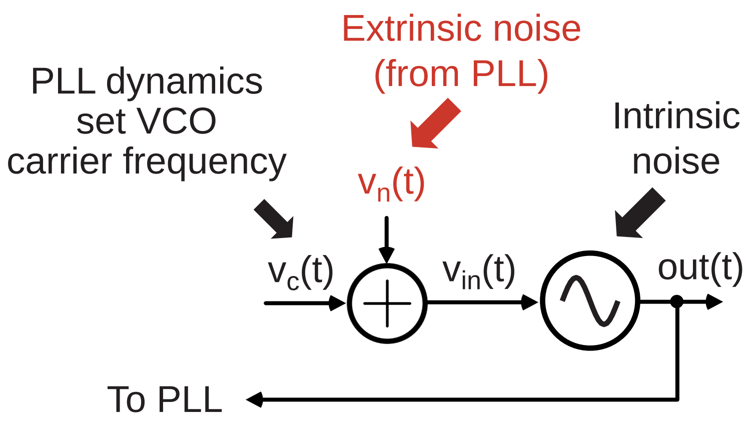
Noise Analysis of Integer-N Synthesizers

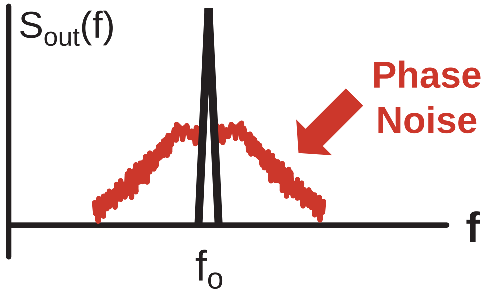
Frequency Synthesizer Noise in Wireless Systems



- **Synthesizer noise has a negative impact on system**
  - **Receiver – lower sensitivity, poorer blocking performance**
  - **Transmitter – increased spectral emissions (output spectrum must meet a mask requirement)**
- **Noise is characterized in frequency domain**

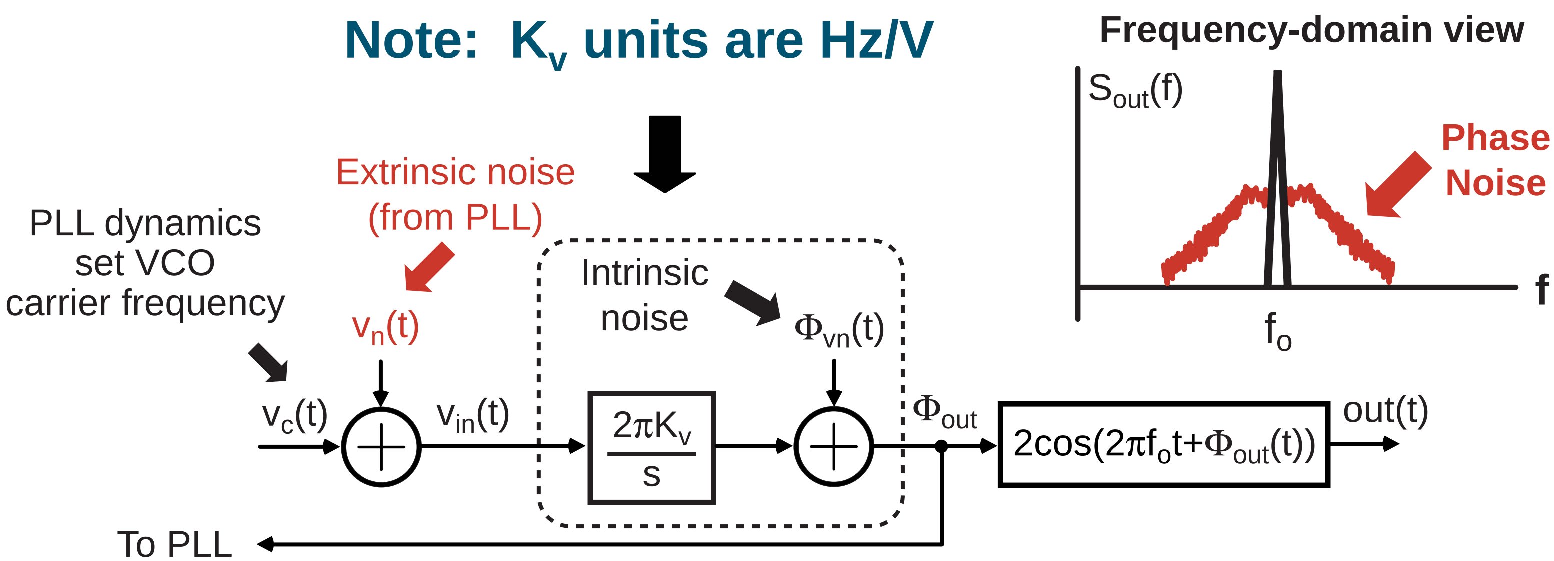
Noise Modeling for Frequency Synthesizers





- **PLL has an impact on VCO noise in two ways**
  - **Adds extrinsic noise from various PLL circuits**
  - **Highpass filters VCO noise through PLL feedback dynamics**
- **Focus on modeling the above based on phase deviations**
  - **Simpler than dealing directly with PLL sine wave output**

Phase Deviation Model for Noise Analysis



- **Model the impact of noise on instantaneous phase**
  - **Relationship between PLL output and instantaneous phase**

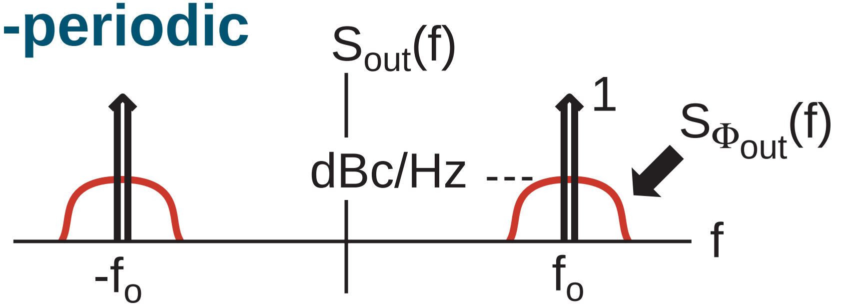
$$out(t) = 2\cos(2\pi f_o t + \underline{\Phi_{out}(t)})$$

  - **Output spectrum (we will derive this in a later lecture)**

$$S_{out}(f) = S_{sin}(f) + S_{sin}(f) * S_{\Phi_{out}}$$

Phase Noise Versus Spurious Noise

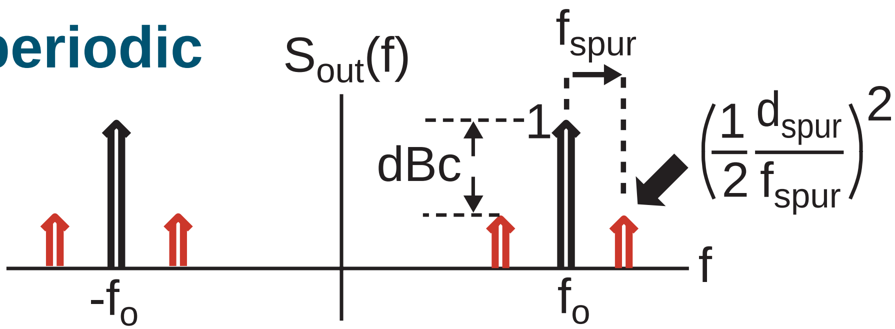
- **Phase noise is non-periodic**



  - **Described as a spectral density relative to carrier power**

$$L(f) = 10\log(S_{\Phi_{out}}(f))\ \mathrm{dBc/Hz}$$

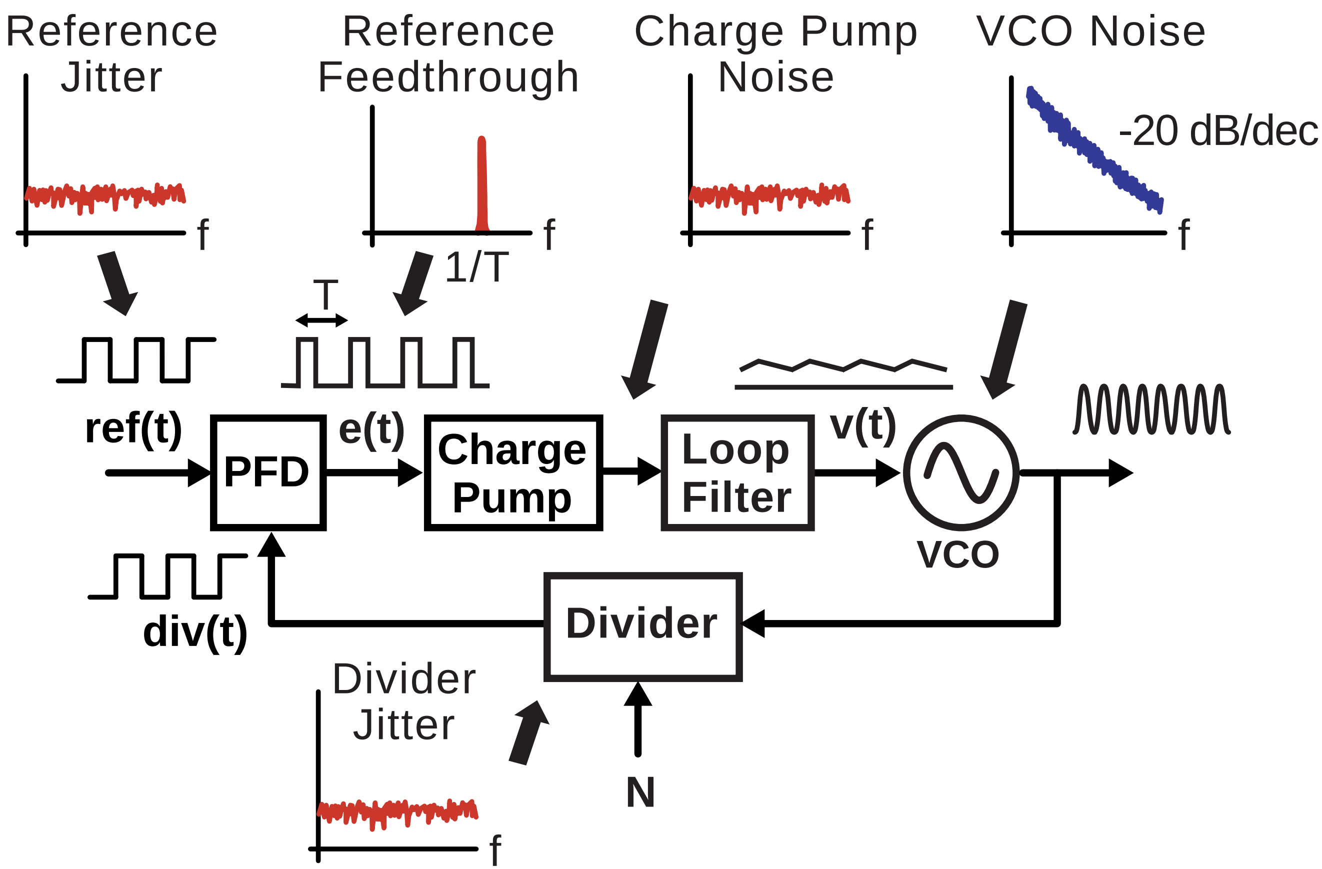
- **Spurious noise is periodic**



  - **Described as tone power relative to carrier power**

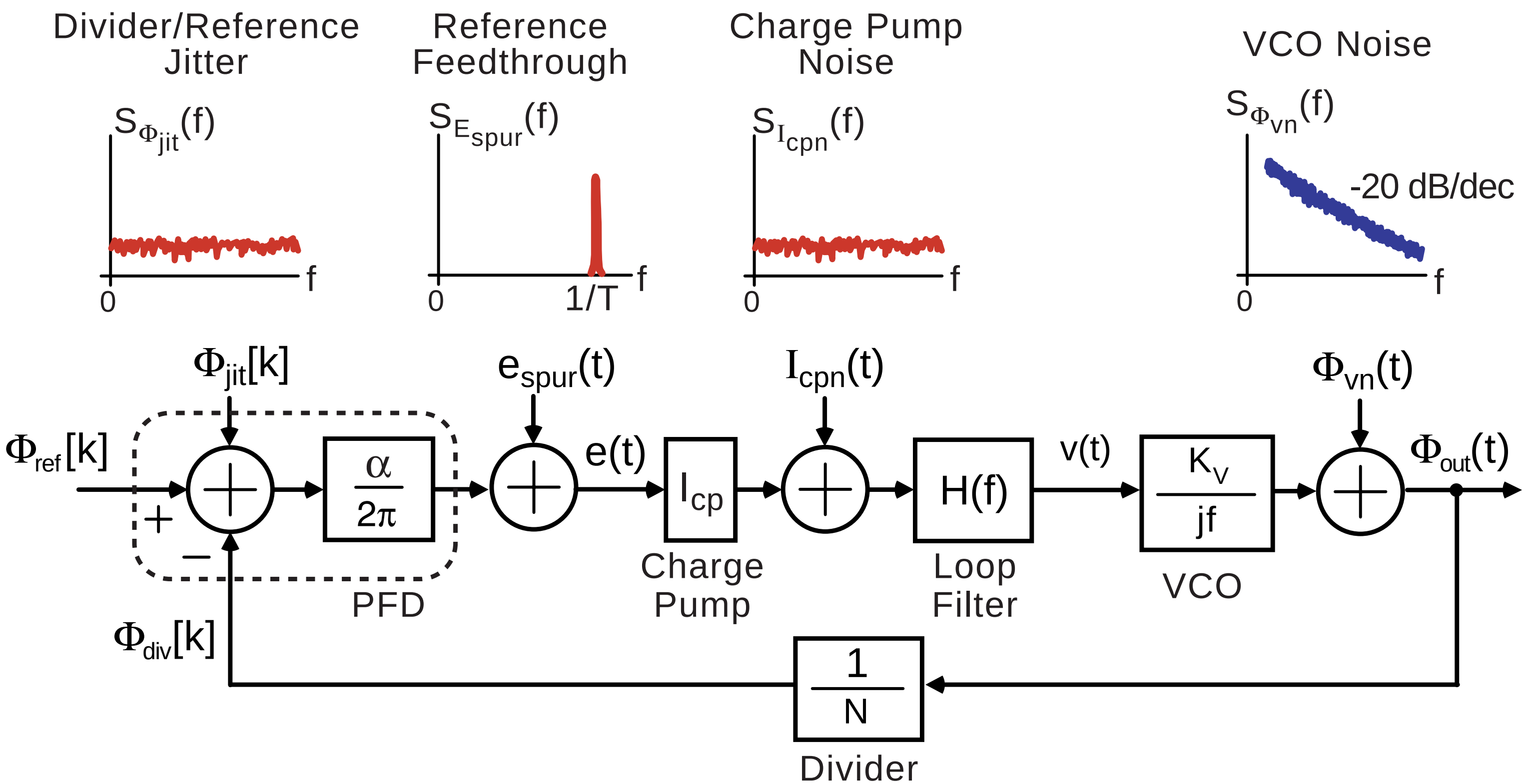
$$20\log\left(\frac{d_{spur}}{2f_{spur}}\right)\ \mathrm{dBc}$$

Sources of Noise in Frequency Synthesizers



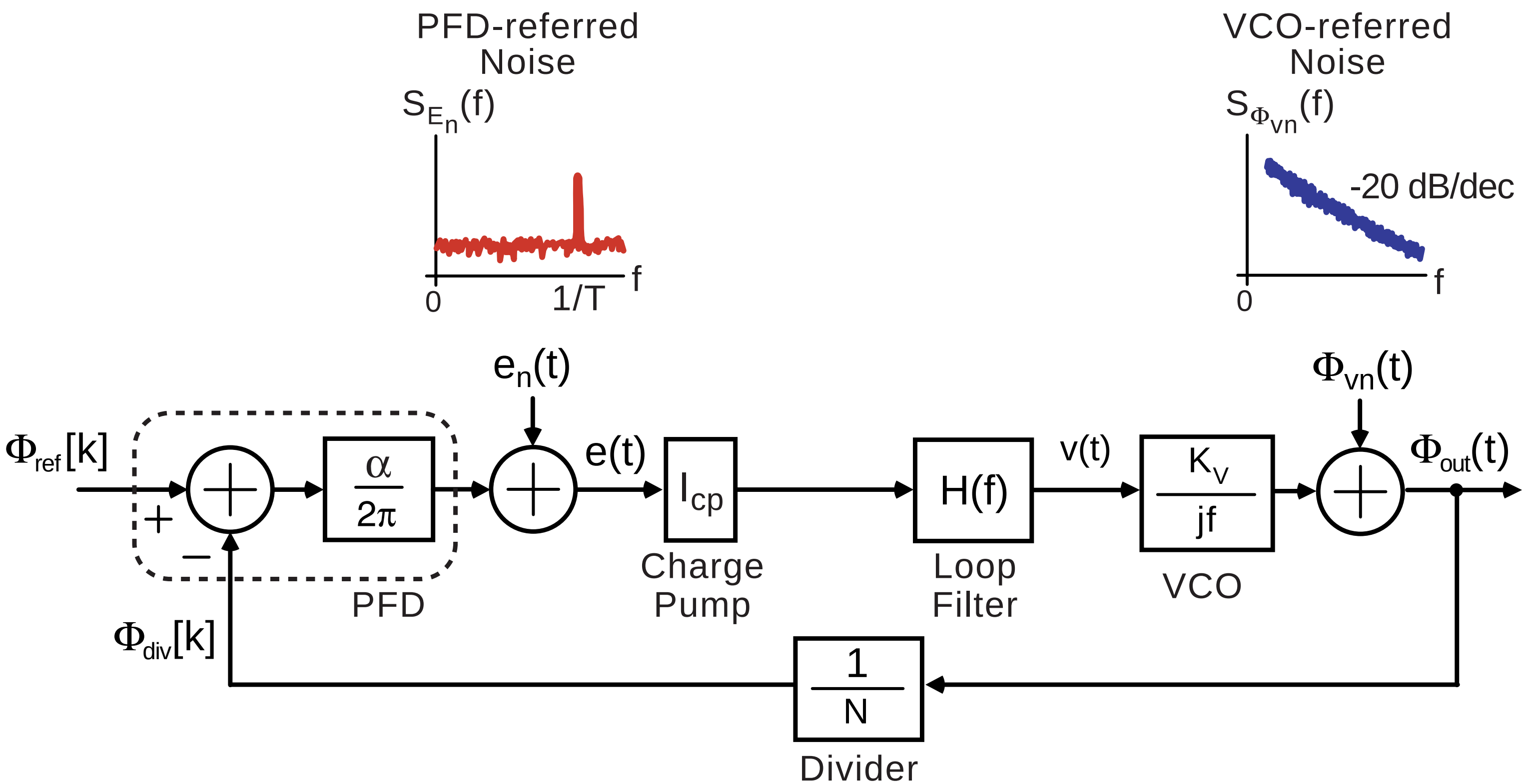
- Extrinsic noise sources to VCO
  - Reference/divider jitter and reference feedthrough
  - Charge pump noise

Modeling the Impact of Noise on Output Phase of PLL



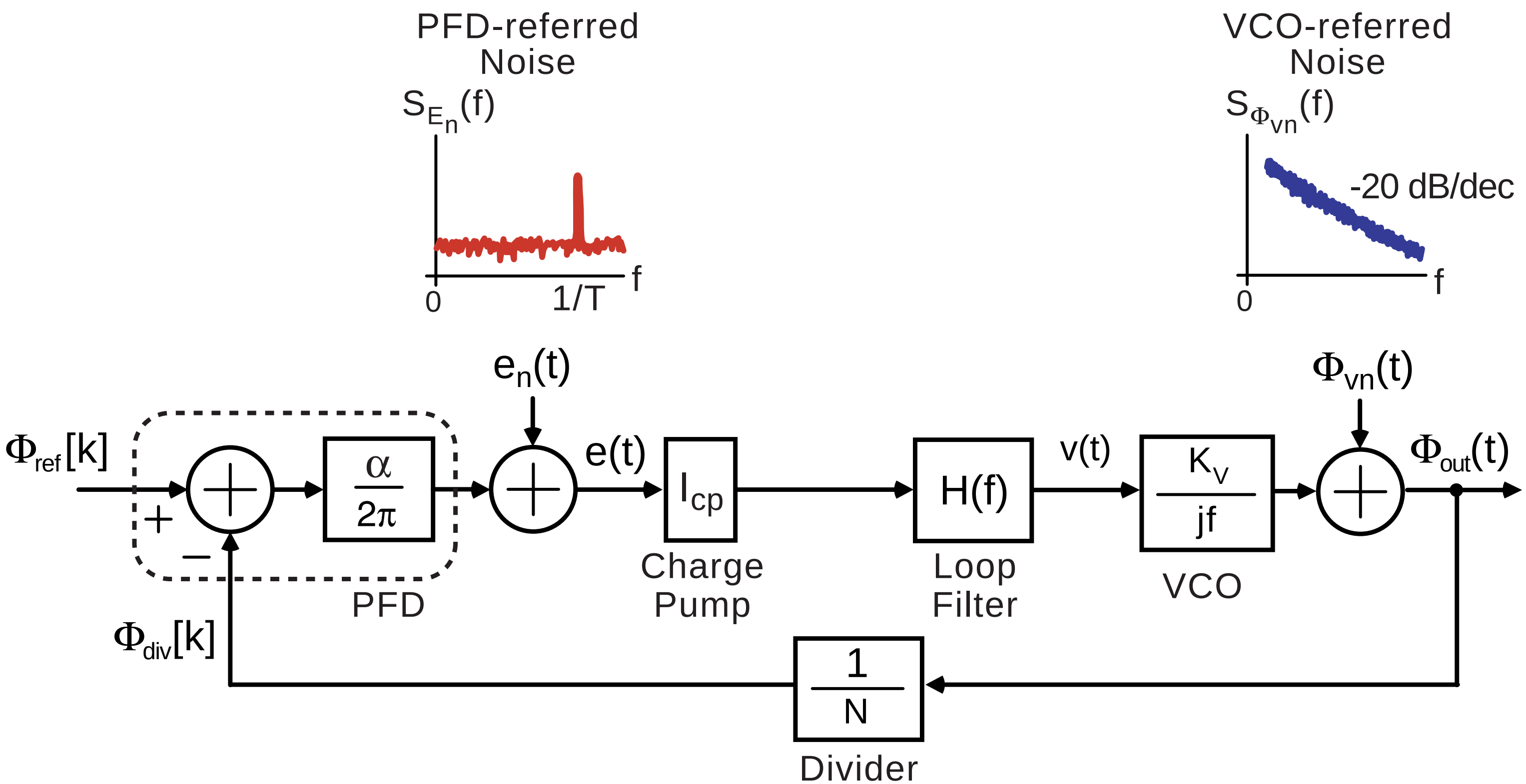
- Determine impact on output phase by deriving transfer function from each noise source to PLL output phase
  - There are a lot of transfer functions to keep track of!

Simplified Noise Model



- **Refer all PLL noise sources (other than the VCO) to the PFD output**
  - **PFD-referred noise corresponds to the sum of these noise sources referred to the PFD output**

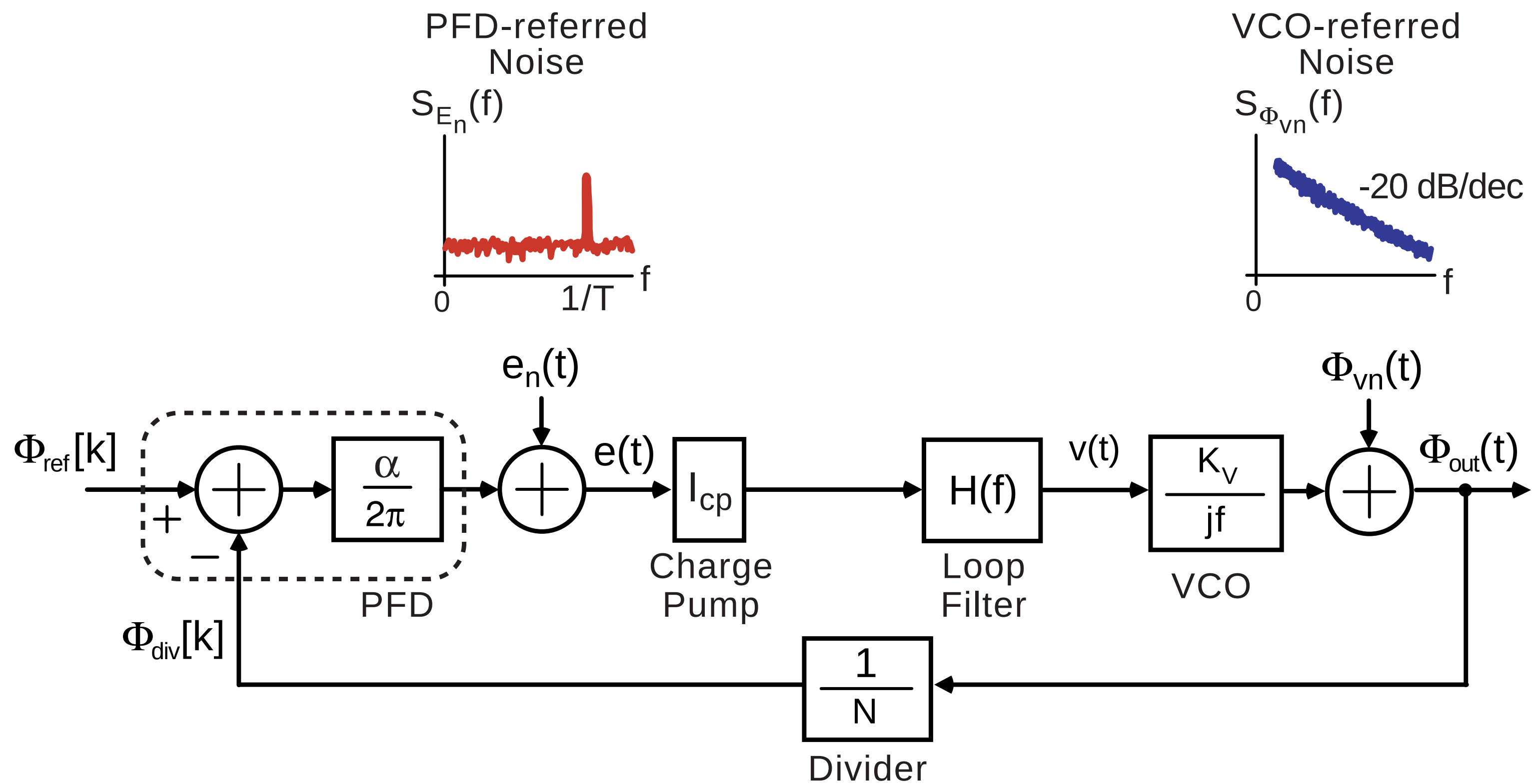
Impact of PFD-referred Noise on Synthesizer Output



- **Transfer function derived using Black's formula**

$$\frac{\Phi_{out}}{e_n} = \frac{I_{cp}H(f)K_v/(jf)}{1 + \alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

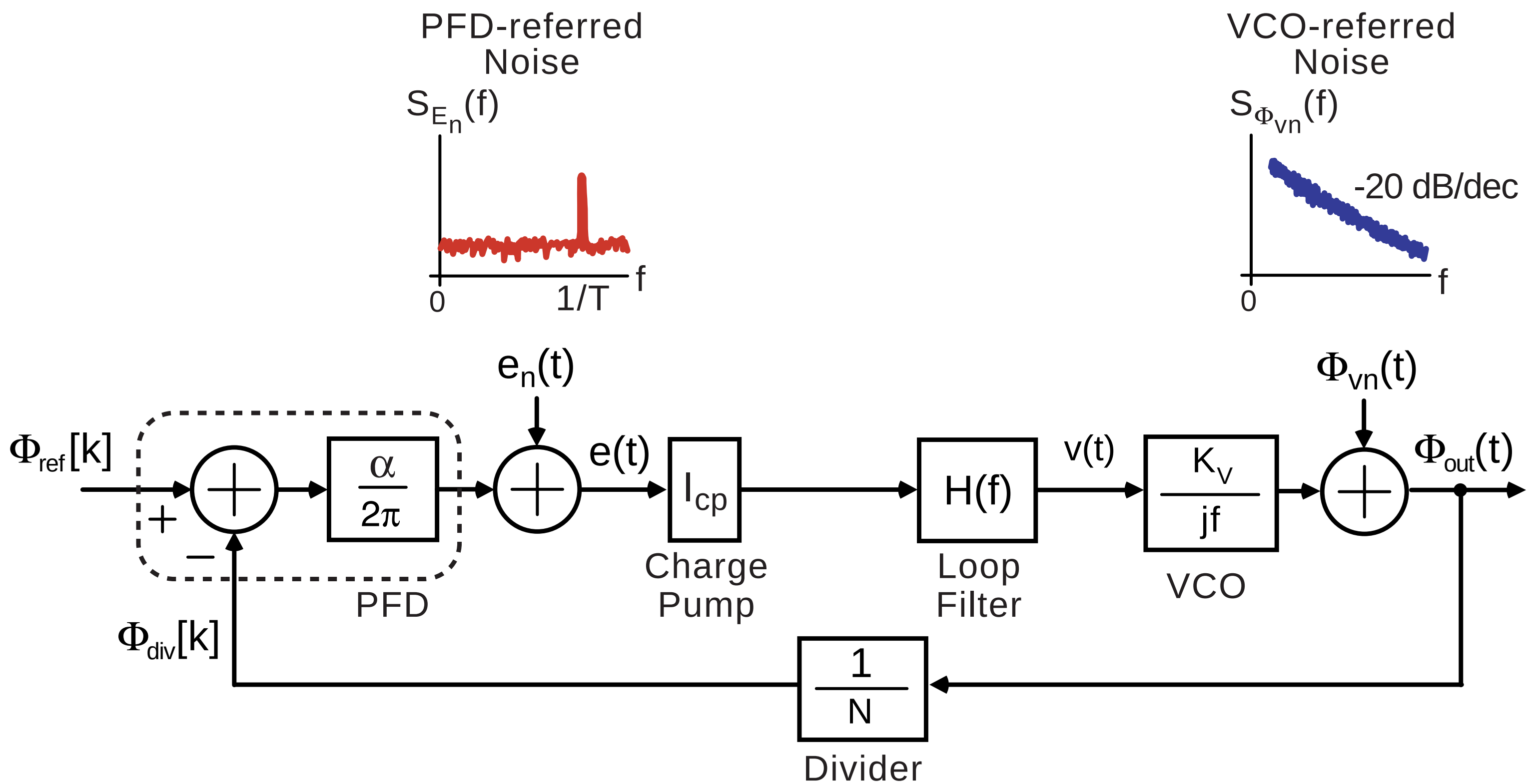
Impact of VCO-referred Noise on Synthesizer Output



- **Transfer function again derived from Black's formula**

$$\frac{\Phi_{out}}{\Phi_{vn}} = \frac{1}{1 + \alpha/(2\pi) I_{cp} H(f) K_v/(jf)(1/N)}$$

A Simpler Parameterization for PLL Transfer Functions



- **Define G(f) as**

$$G(f) = \frac{A(f)}{1 + A(f)}$$

Always has a gain of one at DC

  - **A(f) is the open loop transfer function of the PLL**

$$A(f) = \alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)$$

Parameterize Noise Transfer Functions in Terms of G(f)

- **PFD-referred noise**

$$\frac{\Phi_{out}}{e_n} = \frac{I_{cp}H(f)K_v/(jf)}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

$$= \frac{2\pi}{\alpha}N\frac{\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

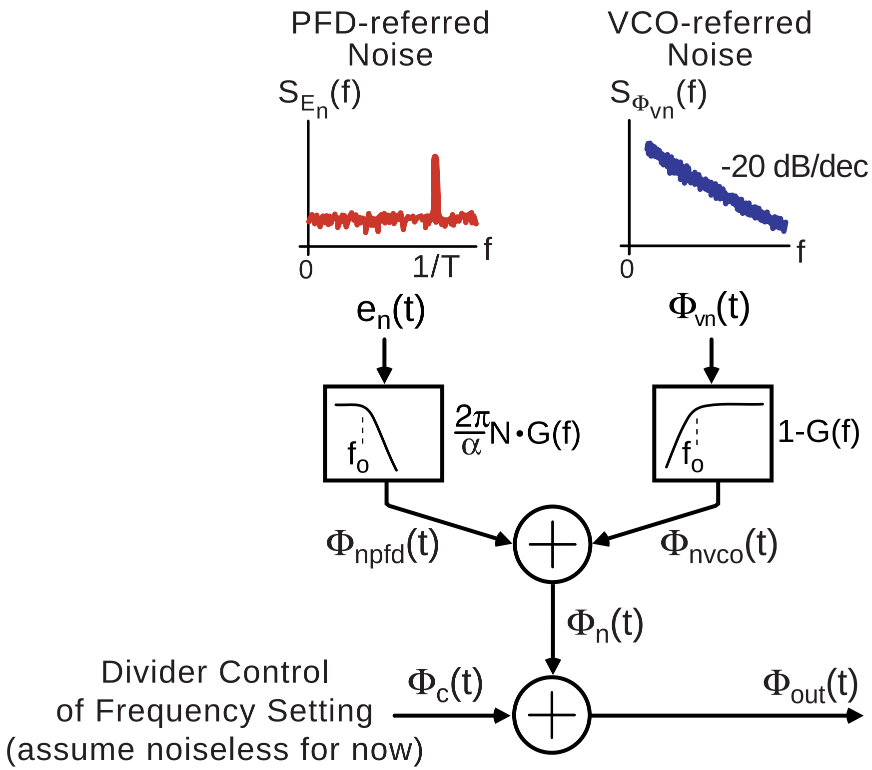
$$= \frac{2\pi}{\alpha}N\frac{A(f)}{1+A(f)} = \boxed{\frac{2\pi}{\alpha}NG(f)}$$

- **VCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_{vn}} = \frac{1}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

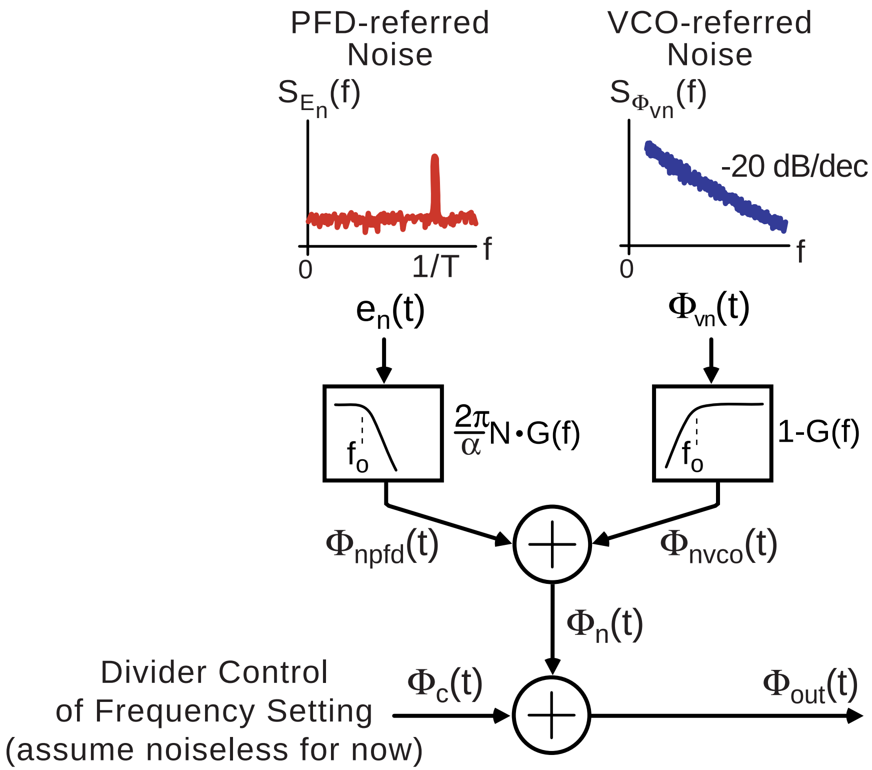
$$= \frac{1}{1+A(f)} = 1 - \frac{A(f)}{1+A(f)} = \boxed{1-G(f)}$$

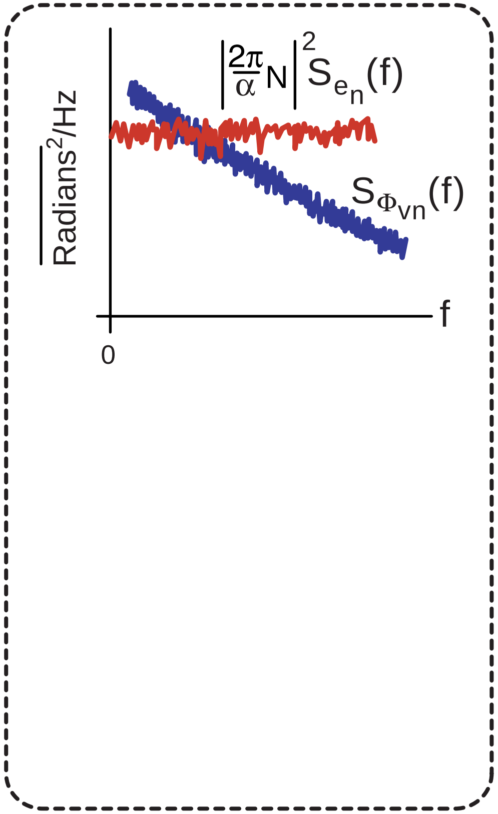
Parameterized PLL Noise Model



- **PFD-referred noise is lowpass filtered**
- **VCO-referred noise is highpass filtered**
- **Both filters have the same transition frequency values**
  - **Defined as f_o**

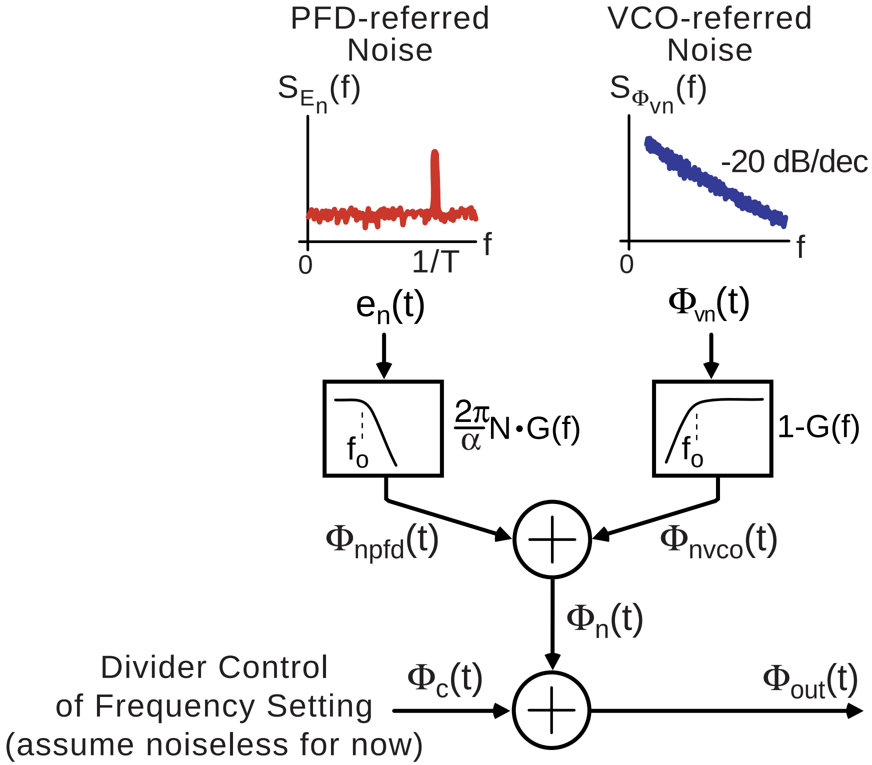
Impact of PLL Parameters on Noise Scaling

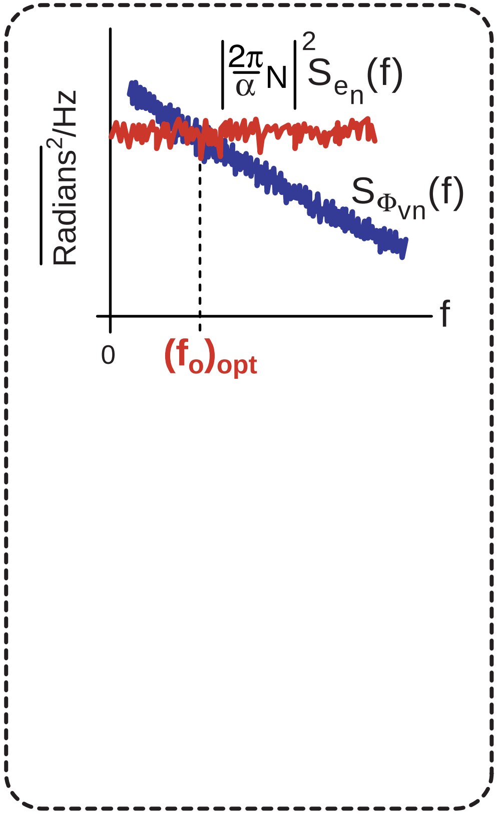




- **PFD-referred noise is scaled by square of divide value and inverse of PFD gain**
  - **High divide values lead to large multiplication of this noise**
- **VCO-referred noise is not scaled (only filtered)**

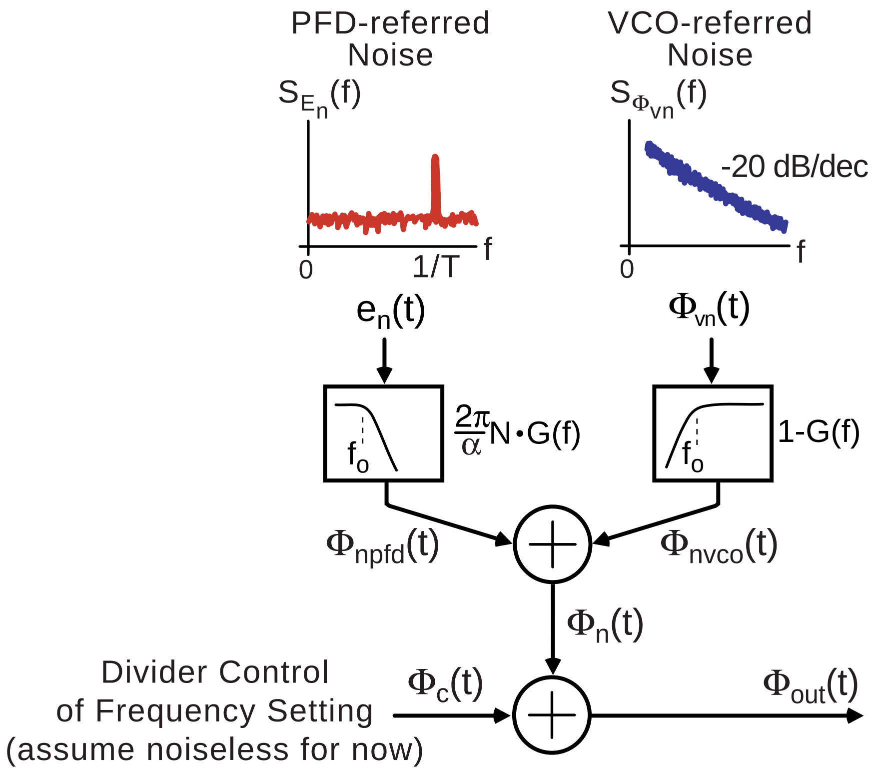
Optimal Bandwidth Setting for Minimum Noise

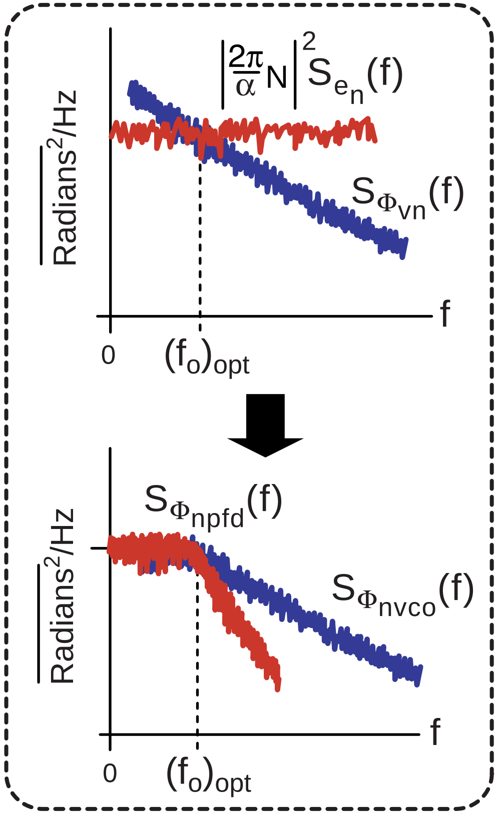




- **Optimal bandwidth is where scaled noise sources meet**
  - **Higher bandwidth will pass more PFD-referred noise**
  - **Lower bandwidth will pass more VCO-referred noise**

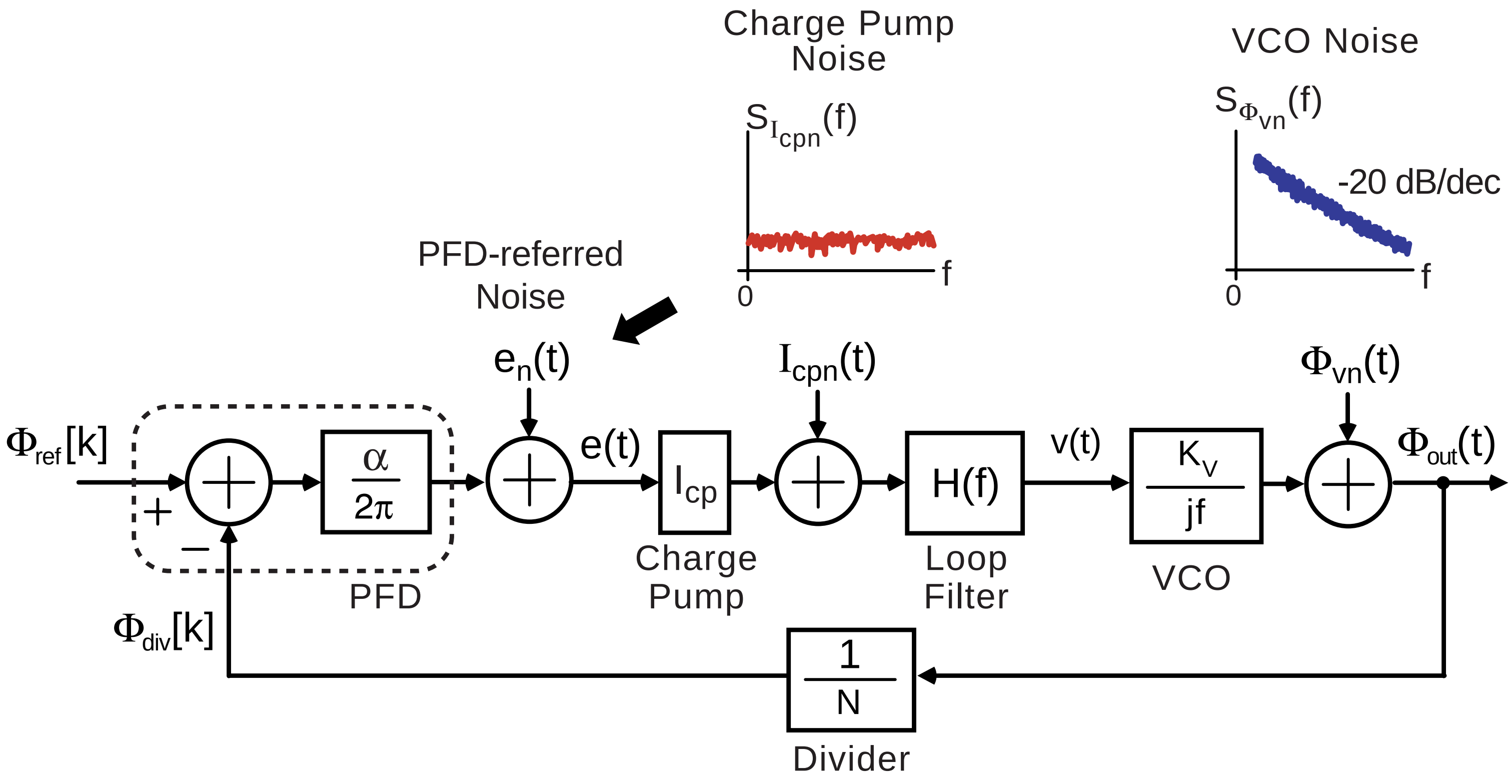
Resulting Output Noise with Optimal Bandwidth





- **PFD-referred noise dominates at low frequencies**
  - **Corresponds to close-in phase noise of synthesizer**
- **VCO-referred noise dominates at high frequencies**
  - **Corresponds to far-away phase noise of synthesizer**

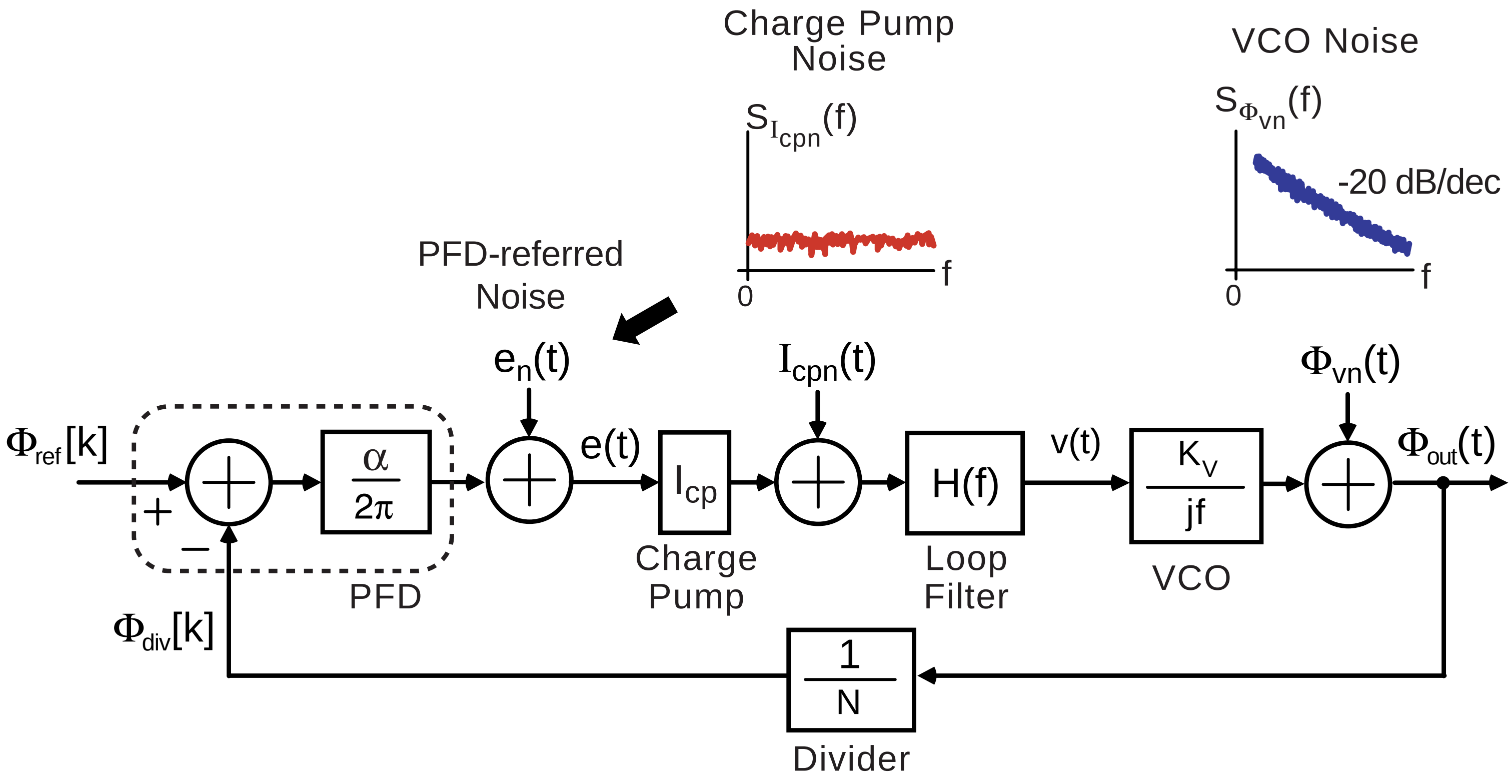
Analysis of Charge Pump Noise Impact



- **We can refer charge pump noise to PFD output by simply scaling it by $1/I_{cp}$**

$$\frac{\Phi_{out}}{I_{cpn}} = \left(\frac{1}{I_{cp}}\right)\frac{\Phi_{out}}{e_n} = \left(\frac{1}{I_{cp}}\right)\frac{2\pi}{\alpha}NG(f)$$

Calculation of Charge Pump Noise Impact

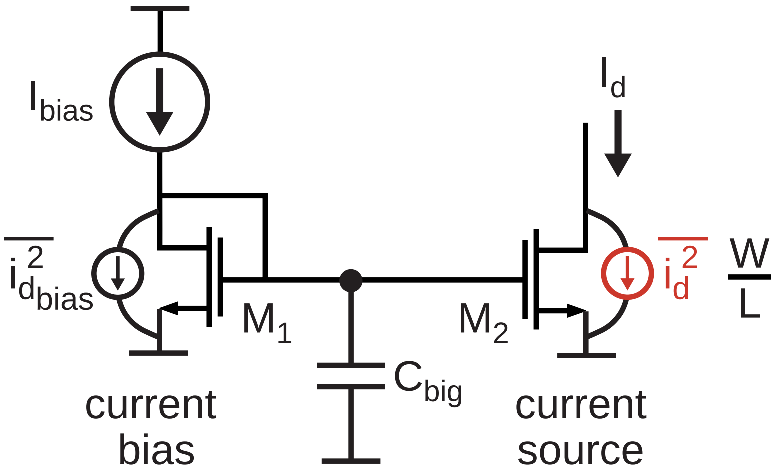


- **Contribution of charge pump noise to overall output noise**

$$S_{\Phi_{out}}(f) = \left(\frac{1}{I_{cp}}\right)^2 \left(\frac{2\pi}{\alpha}N\right)^2 |G(f)|^2 S_{I_{cpn}}(f) + \text{other sources}$$

  - **Need to determine impact of I_{cp} on $S_{Icpn}(f)$**

Impact of Transistor Current Value on its Noise



- **Charge pump noise will be related to the current it creates as**

$$S_{I_{cpn}}(f) \propto \frac{\overline{I_d^2}}{\Delta f} = 4kT\gamma g_{do}$$

- **Recall that g_{do} is the channel resistance at zero V_{ds}**
  - **At *a fixed current density*, we have**

$$g_{do} \propto W \propto I_d \;\Rightarrow\; \boxed{\overline{I_d^2} \propto I_d}$$

Impact of Charge Pump Current Value on Output Noise

- **Recall**

$$S_{\Phi_{out}}(f) = \left(\frac{1}{I_{cp}}\right)^2 \left(\frac{2\pi}{\alpha}N\right)^2 |G(f)|^2 S_{I_{cpn}}(f) + \text{other sources}$$

- **Given previous slide, we can say**

$$S_{I_{cpn}}(f) \propto I_{cp}$$

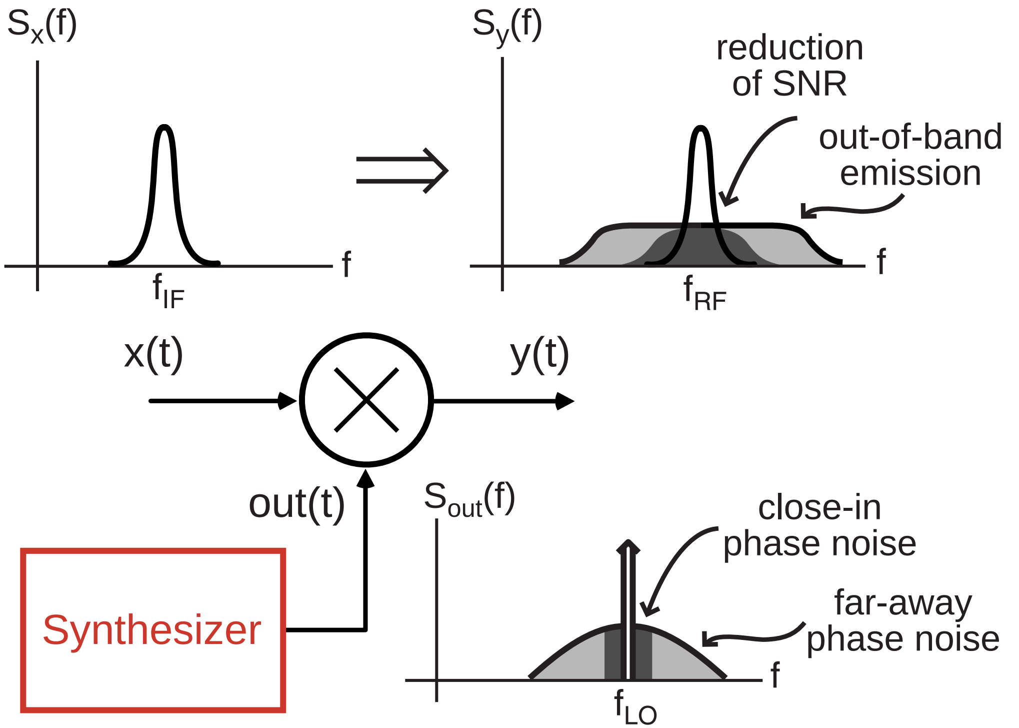
  - **Assumes a fixed current density for the key transistors in the charge pump as I_{cp} is varied**

- **Therefore**

$$S_{\Phi_{out}}(f)\Big|_{\text{charge pump}} \propto \frac{1}{I_{cp}}$$

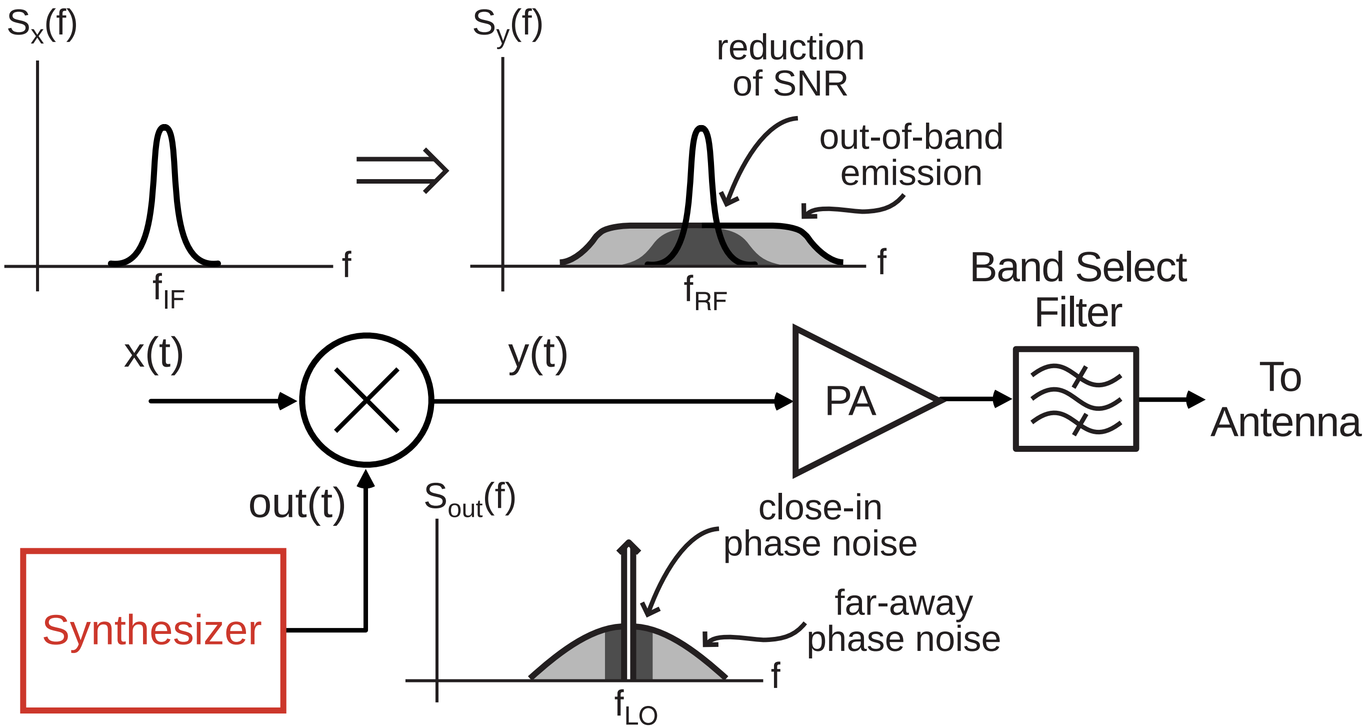
  - **Want high charge pump current to achieve low noise**
  - **Limitation set by power and area considerations**

Impact of Synthesizer Noise on Transmitters



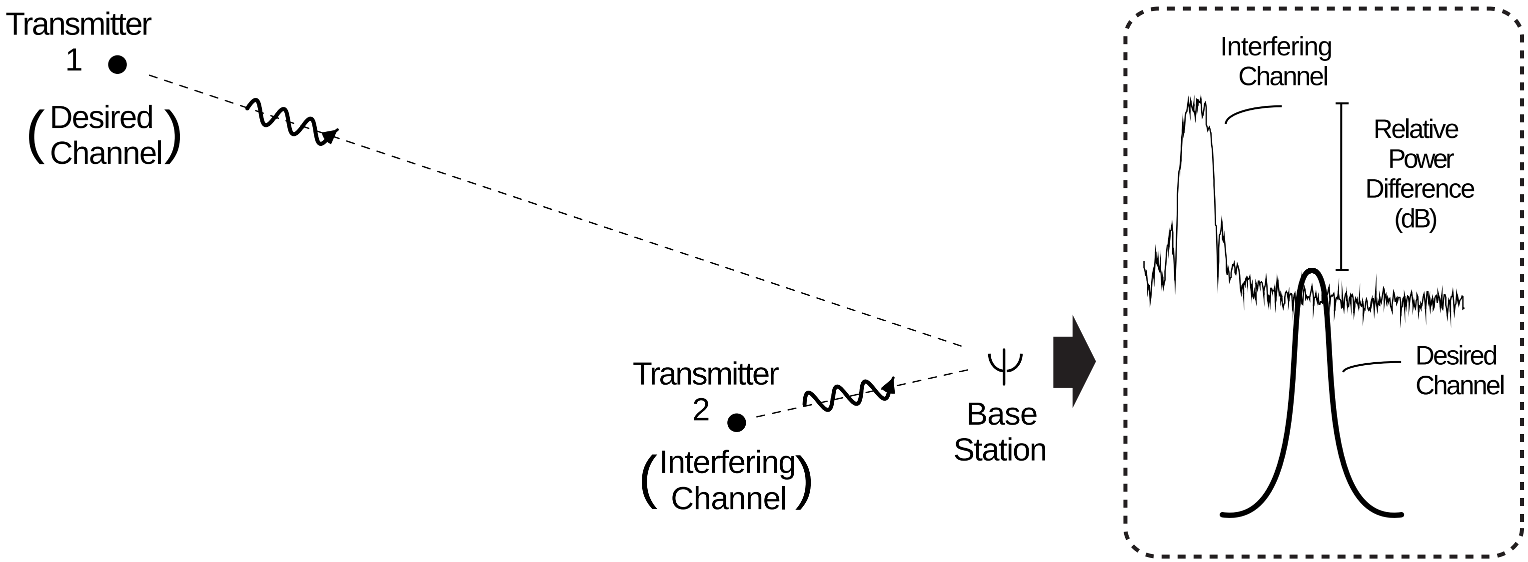
- **Synthesizer noise can be lumped into two categories**
  - **Close-in phase noise: reduces SNR of modulated signal**
  - **Far-away phase noise: creates spectral emissions outside the desired transmit channel**
    - This is the critical issue for transmitters

Impact of Remaining Portion of Transmitter



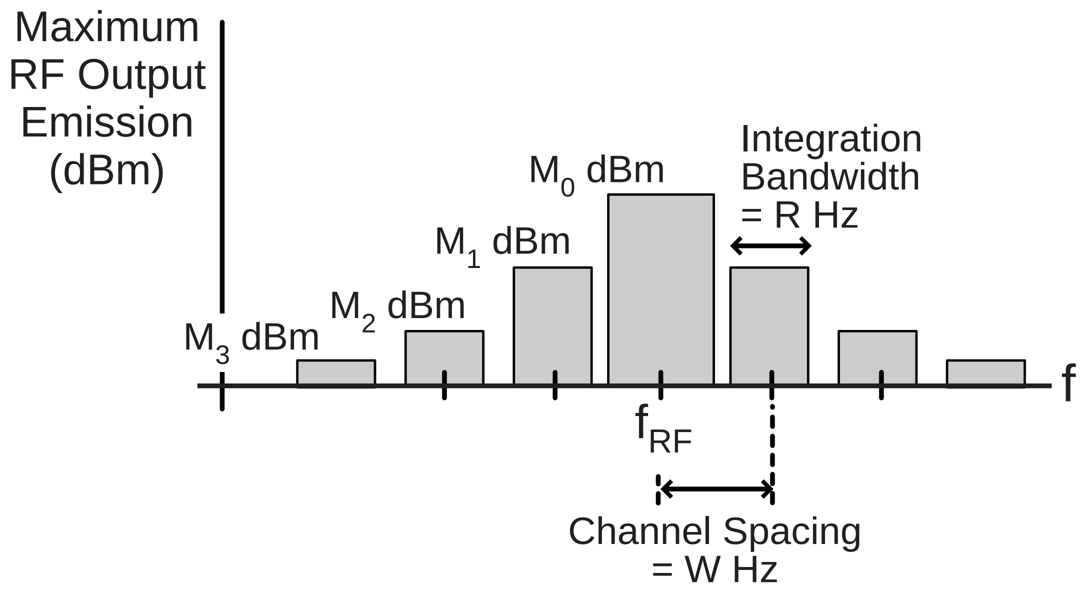
- **Power amplifier**
  - **Nonlinearity will increase out-of-band emission and create harmonic content**
- **Band select filter**
  - **Removes harmonic content, but not out-of-band emission**

Why is Out-of-Band Emission A Problem?



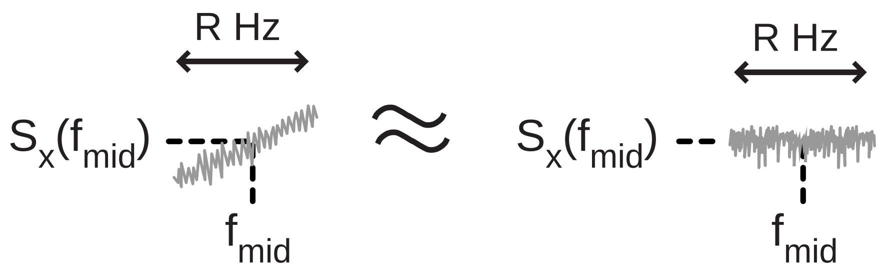
- **Near-far problem**
  - **Interfering transmitter closer to receiver than desired transmitter**
  - **Out-of-emission requirements must be stringent to prevent complete corruption of desired signal**

Specification of Out-of-Band Emissions



- **Maximum radiated power is specified in desired and adjacent channels**
  - **Desired channel power: maximum is M_0 dBm**
  - **Out-of-band emission: maximum power defined as integration of transmitted spectral density over bandwidth R centered at midpoint of each channel offset**

Calculation of Transmitted Power in a Given Channel



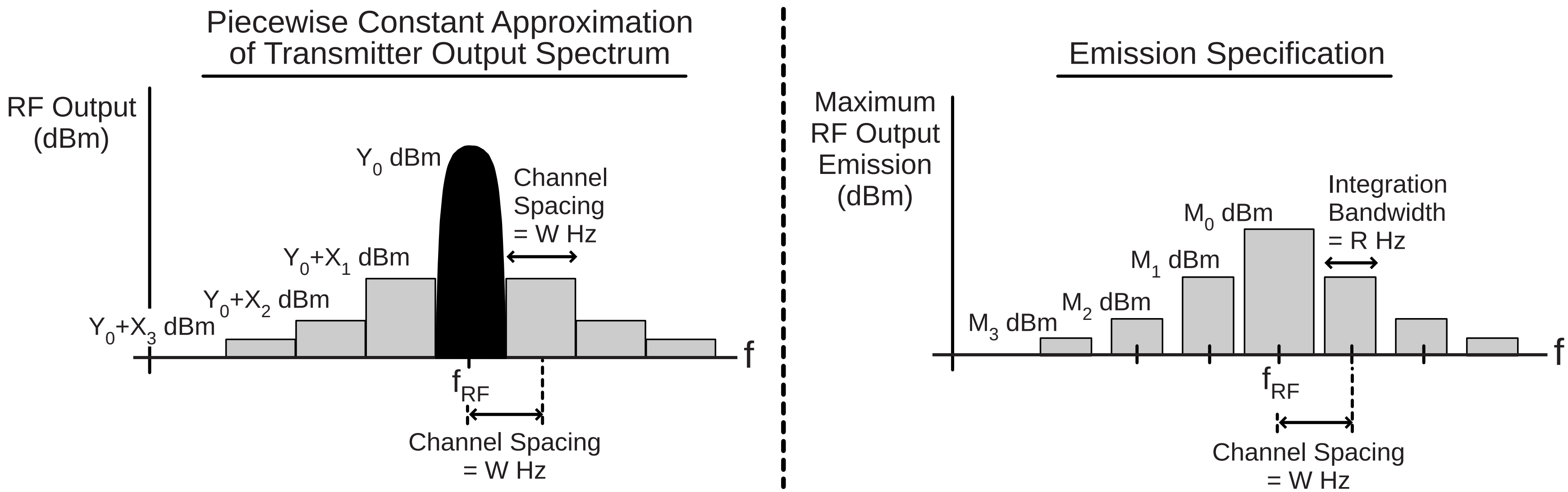
- **For simplicity, assume that the spectral density is flat over the channel bandwidth**
  - **Actual spectral density of signal often varies with frequency over the bandwidth of a given channel**
- **Resulting power calculation (single-sided $S_x(f)$)**

$$P_x = \int_{f_{mid}-R/2}^{f_{mid}+R/2} S_x(f)df \approx RS_x(f_{mid})$$

- **Express in dB (Note: dB(x) = 10log(x))**

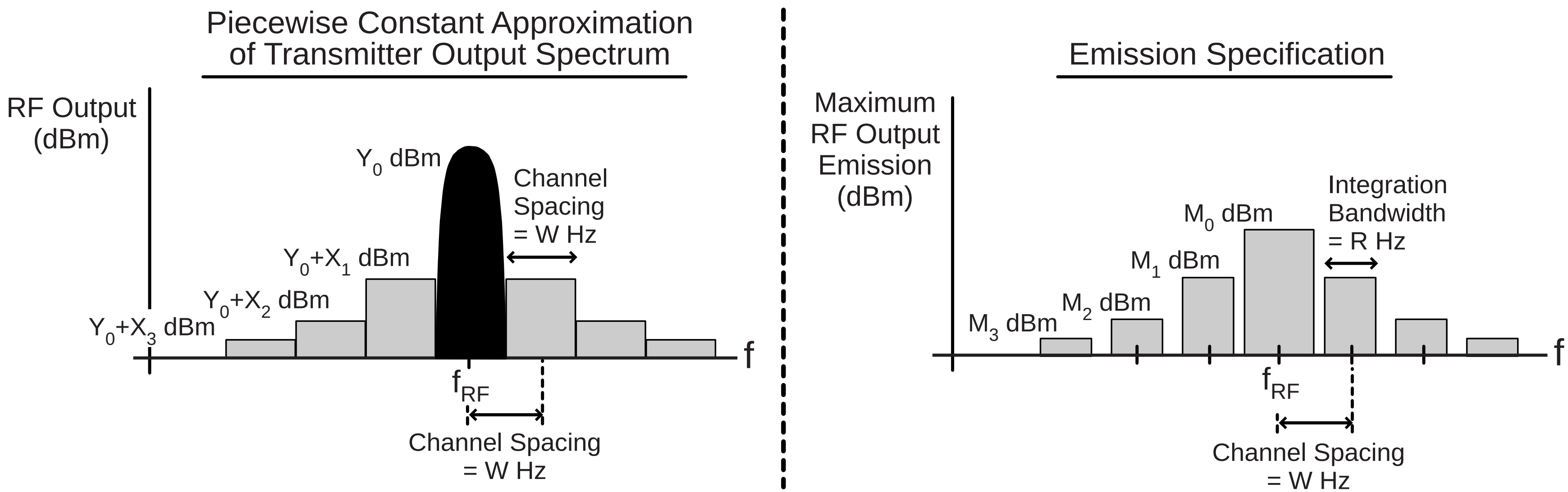
$$\text{dB}(P_x) \approx \text{dB}(RS_x(f_{mid})) = \boxed{\text{dB}(S_x(f_{mid})) + \text{dB}(R)}$$

Transmitter Output Versus Emission Specification



- **Assume a piecewise constant spectral density profile for transmitter**
  - **Simplifies calculations**
- **Issue: emission specification is measured over a narrower band than channel spacing**
  - **Need to account for bandwidth discrepancy when doing calculations**

Correction Factor for Bandwidth Mismatch



- **Calculation of maximum emission in offset channel 1**

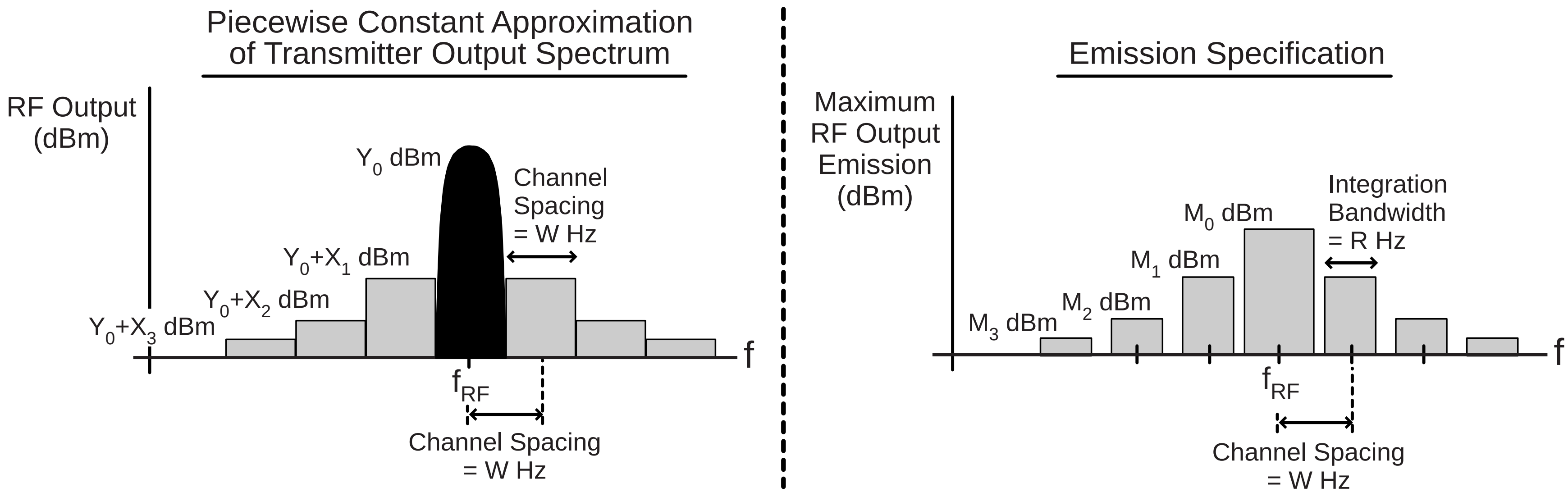
$$\text{dB}(S_{(Y_0+X_1)}R) \;\leq\; M_1$$

$$\Rightarrow\; \text{dB}\left(S_{(Y_0+X_1)}W\frac{R}{W}\right) \;\leq\; M_1$$

$$\Rightarrow\; \text{dB}\left(S_{(Y_0+X_1)}W\right) + \text{dB}\left(\frac{R}{W}\right) \;\leq\; M_1$$

$$\Rightarrow\; Y_0+X_1+\text{dB}\left(\frac{R}{W}\right) \;\leq\; M_1 \quad \Rightarrow\; \boxed{X_1 \;\leq\; M_1-Y_0+\text{dB}\left(\frac{W}{R}\right)}$$

Condition for Most Stringent Emission Requirement



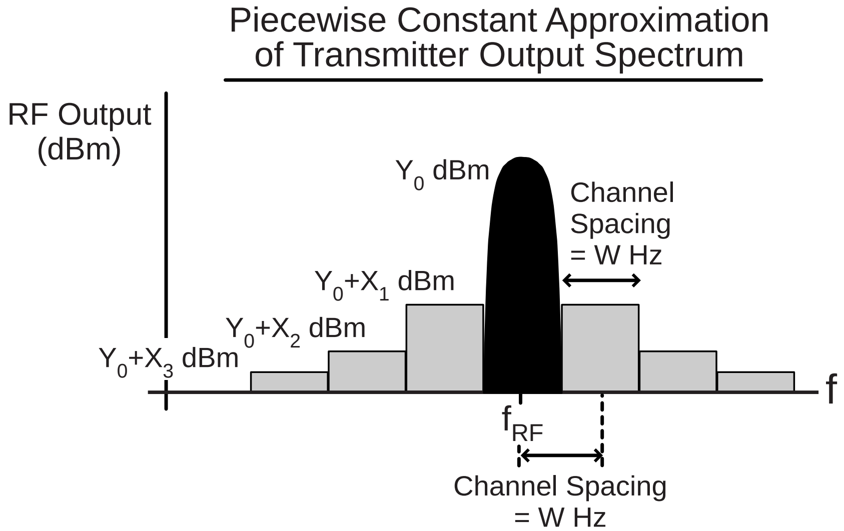
- **Out-of-band emission requirements are function of the power of the signal in the desired channel**
  - **For offset channel 1 (as calculated on previous slide)**

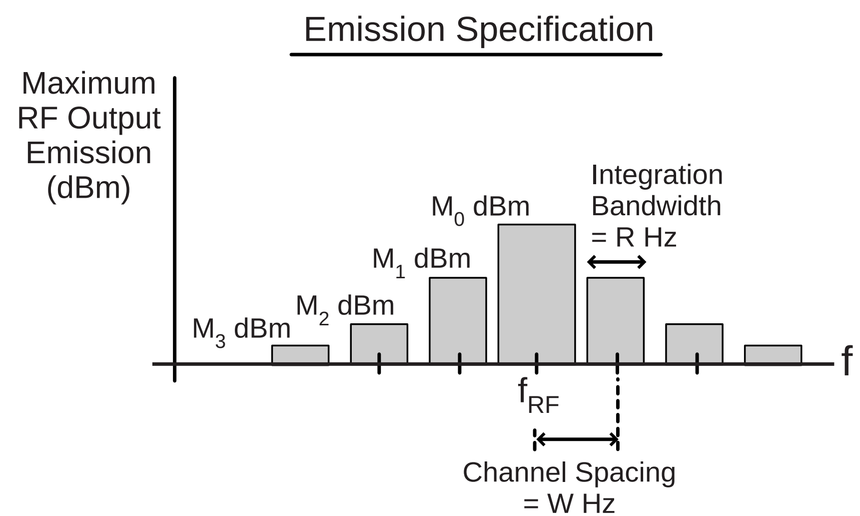
$$X_1 \; \leq \; M_1 - Y_0 + \mathrm{dB}\left(\frac{W}{R}\right)$$

  - **Most stringent case is when Y_0 maximum**

$$\Rightarrow \; Y_0 = M_0$$

Table of Most Stringent Emission Requirements

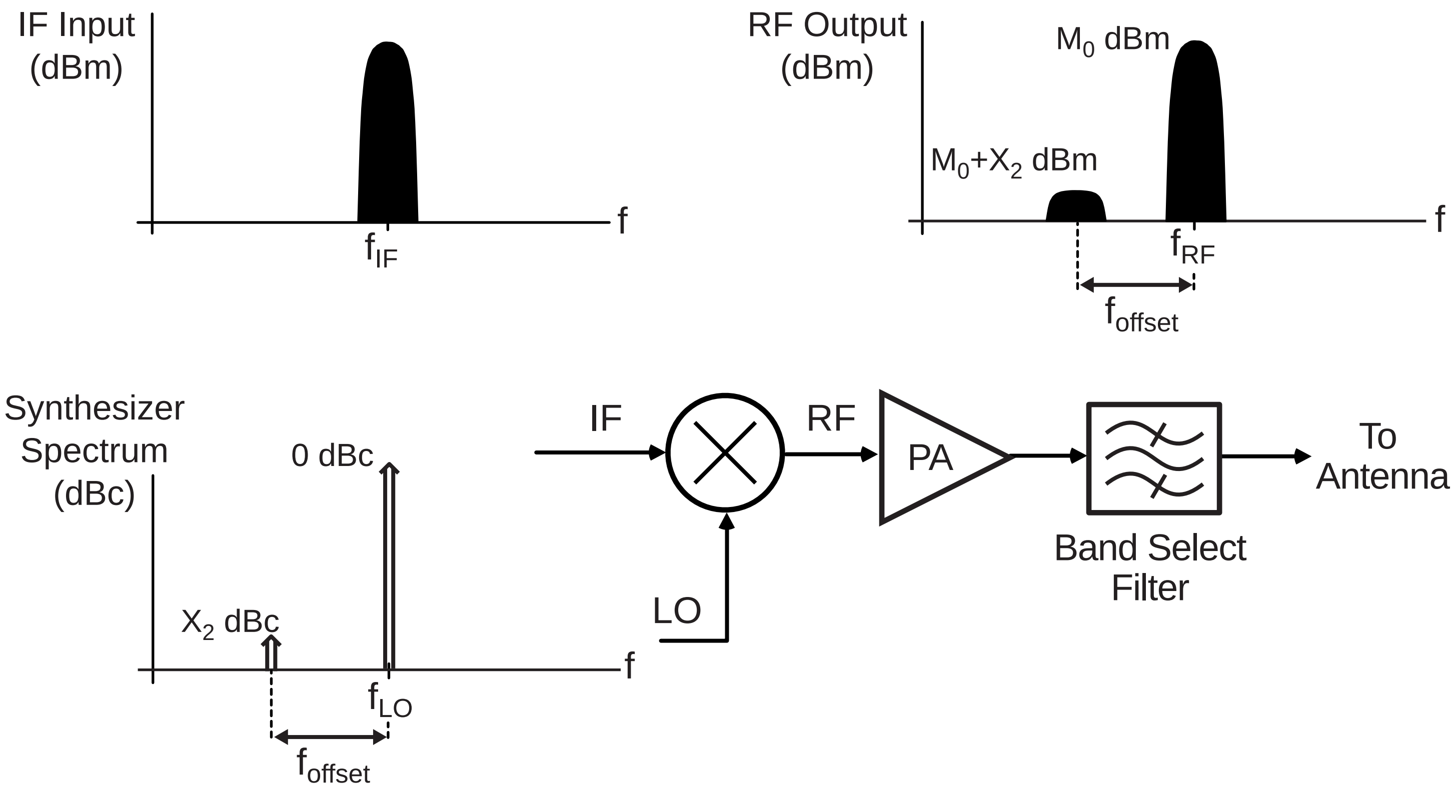




Channel Offset	Mask Power	Emission Requirements (Most Stringent)
0	M_0 dBm	$Y_0 = M_0$ (for most stringent case)
1	M_1 dBm	$X_1 = M_1 - M_0 + \text{dB}(W/R)$ dB
2	M_2 dBm	$X_2 = M_2 - M_0 + \text{dB}(W/R)$ dB
3	M_3 dBm	$X_3 = M_3 - M_0 + \text{dB}(W/R)$ dB

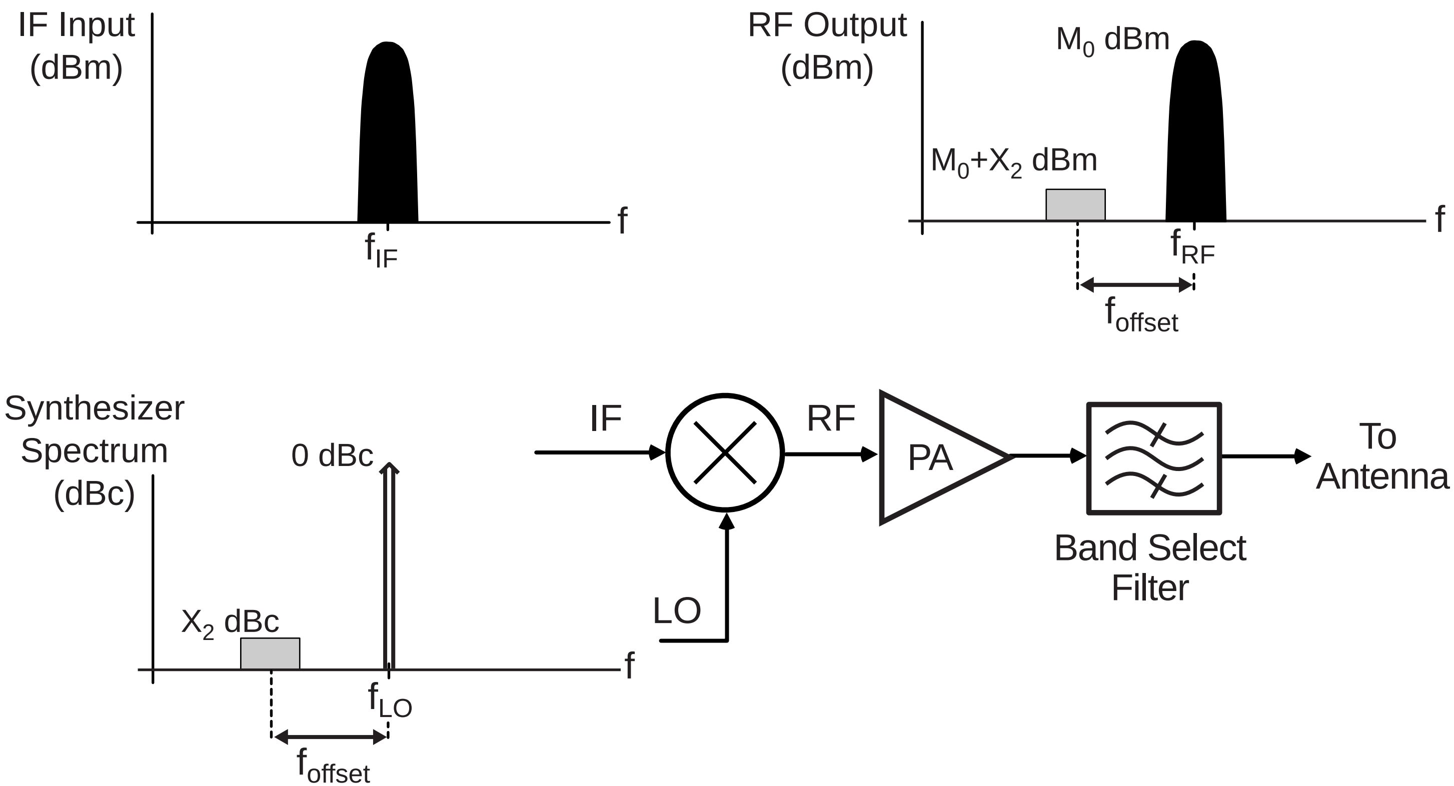
$$(\text{Note}: \quad \text{dB}(W/R) = 10\log(W/R))$$

Impact of Synthesizer Noise on Transmitter Output



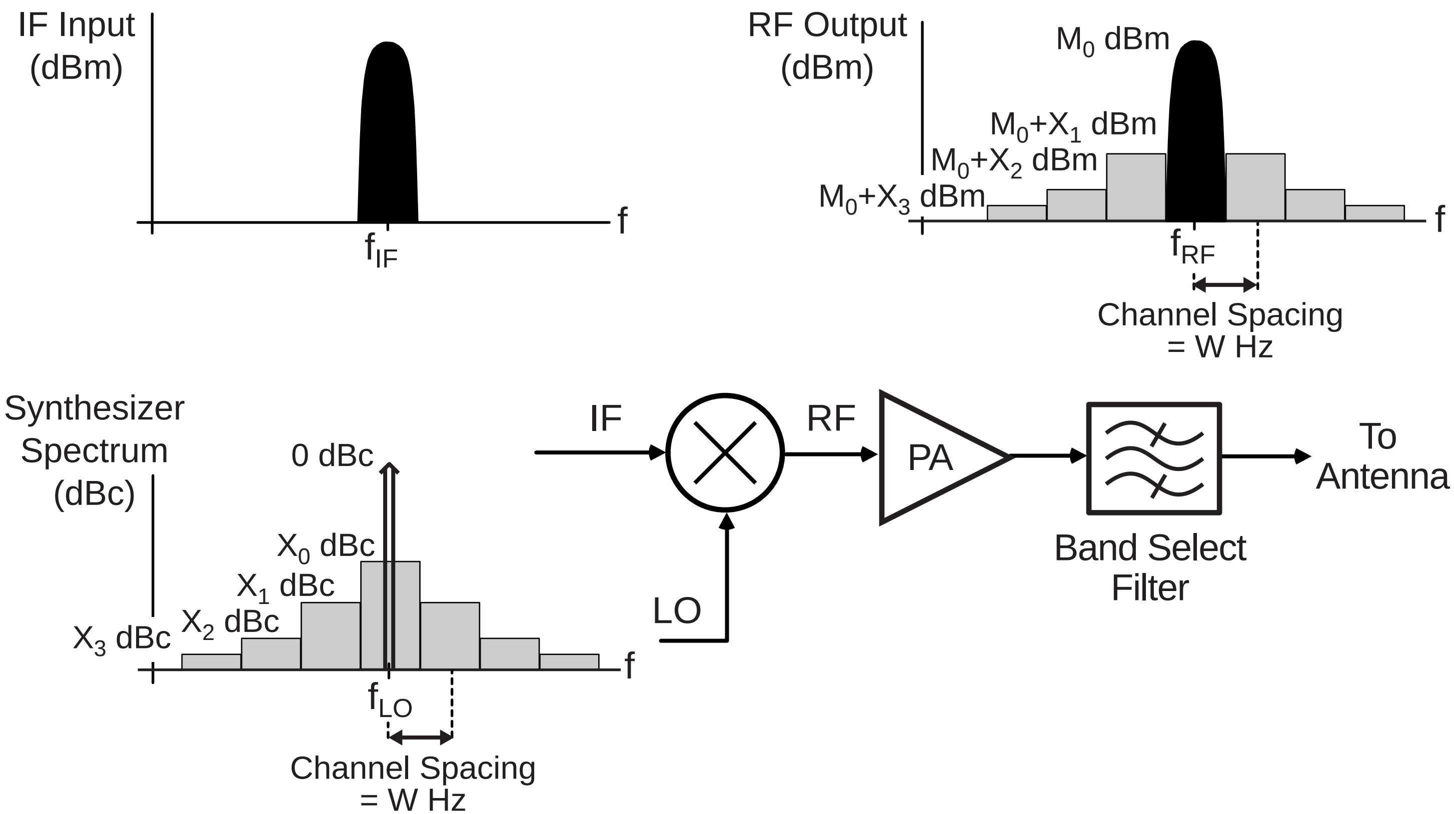
- **Consider a spurious tone at a given offset frequency**
  - **Convolution with IF signal produces a replica of the desired signal at the given offset frequency**

Impact of Synthesizer Phase Noise (Isolated Channel)



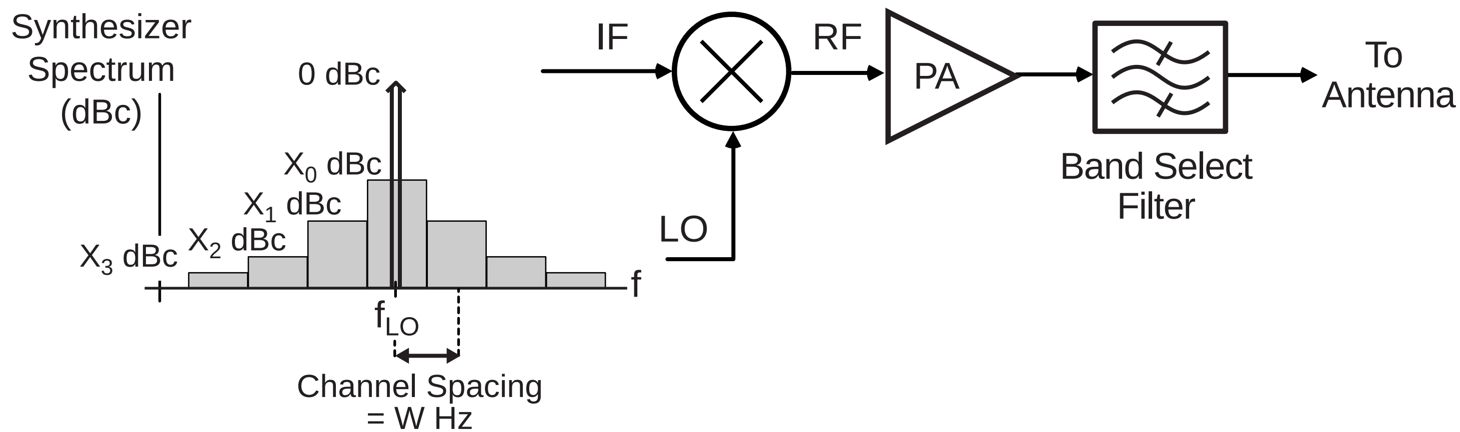
- **Consider phase noise at a given offset frequency**
  - **Convolution with IF signal produces a smeared version of the desired signal at the given offset frequency**
    - For simplicity, approximate smeared signal as shown

Impact of Synthesizer Phase Noise (All Channels)



- **Partition synthesizer phase noise into channels**
  - **Required phase noise power (dBc) in each channel is related directly to spectral mask requirements**
    - Exception is X_0 – set by transmit SNR requirements

Synthesizer Phase Noise Requirements



- **Impact of channel bandwidth (offset channel 1)**

$$\mathrm{dB}(S_{X_1}W) \leq X_1\ \mathrm{dBc} \Rightarrow \boxed{\mathrm{dB}(S_{X_1}) \leq X_1 - \mathrm{dB}(W)\ \mathrm{dBc/Hz}}$$

- **Overall requirements (most stringent, i.e., $Y_0 = M_0$)**

Channel Offset	Emission Requirements (Most Stringent)	Maximum Synth. Phase Noise (Most Stringent)
0	$Y_0 = M_0$	set by required transmit SNR
1	$X_1 = M_1 - M_0 + \mathrm{dB}(W/R)$ dB	X_1 - dB(W) dBc/Hz
2	$X_2 = M_2 - M_0 + \mathrm{dB}(W/R)$ dB	X_2 - dB(W) dBc/Hz
3	$X_3 = M_3 - M_0 + \mathrm{dB}(W/R)$ dB	X_3 - dB(W) dBc/Hz

Example – DECT Cordless Telephone Standard

- **Standard for many cordless phones operating at 1.8 GHz**
- **Transmitter Specifications**
  - **Channel spacing: W = 1.728 MHz**
  - **Maximum output power: M_o = 250 mW (24 dBm)**
  - **Integration bandwidth: R = 1 MHz**
  - **Emission mask requirements**

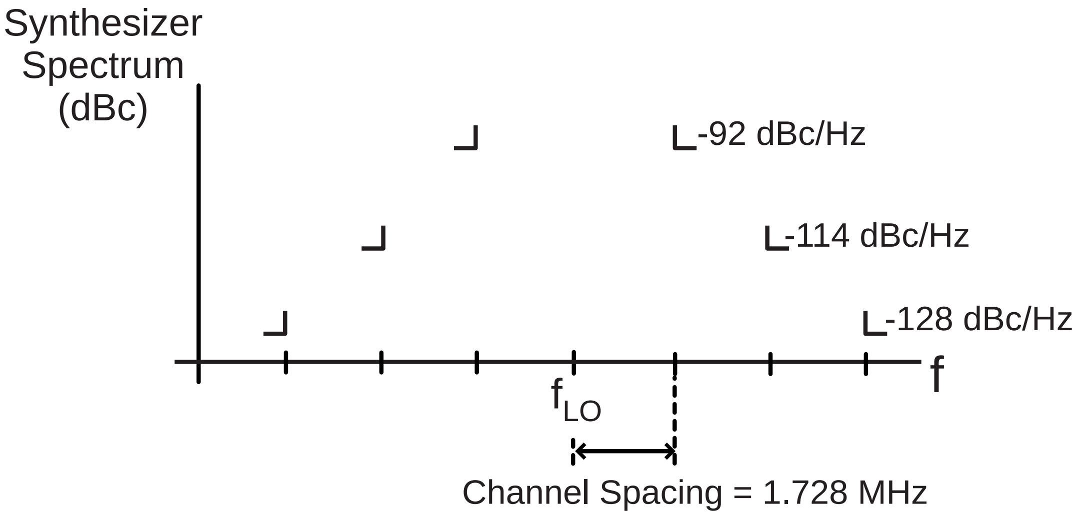
f_{offset} (MHz)	Emission Mask (dBm)
0	M_0 = 24 dBm
1.728	M_1 = -8 dBm
3.456	M_2 = -30 dBm
5.184	M_3 = -44 dBm

Synthesizer Phase Noise Requirements for DECT

- **Using previous calculations with DECT values**

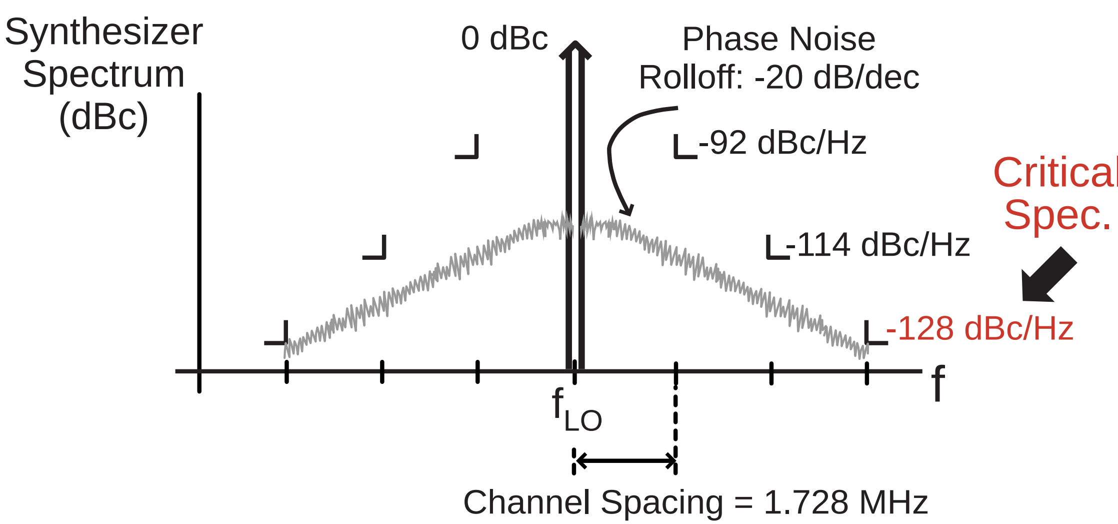
Channel Offset	Mask Power	Maximum Synth. Noise Power in Integration BW	Maximum Synth. Phase Noise at Channel Offset
0	24 dBm	set by required transmit SNR	
1.728 MHz	-8 dBm	X_1 = -29.6 dBc	-92 dBc/Hz
3.456 MHz	-30 dBm	X_2 = -51.6 dBc	-114 dBc/Hz
5.184 MHz	-44 dBm	X_3 = -65.6 dBc	-128 dBc/Hz

- **Graphical display of phase noise mask**

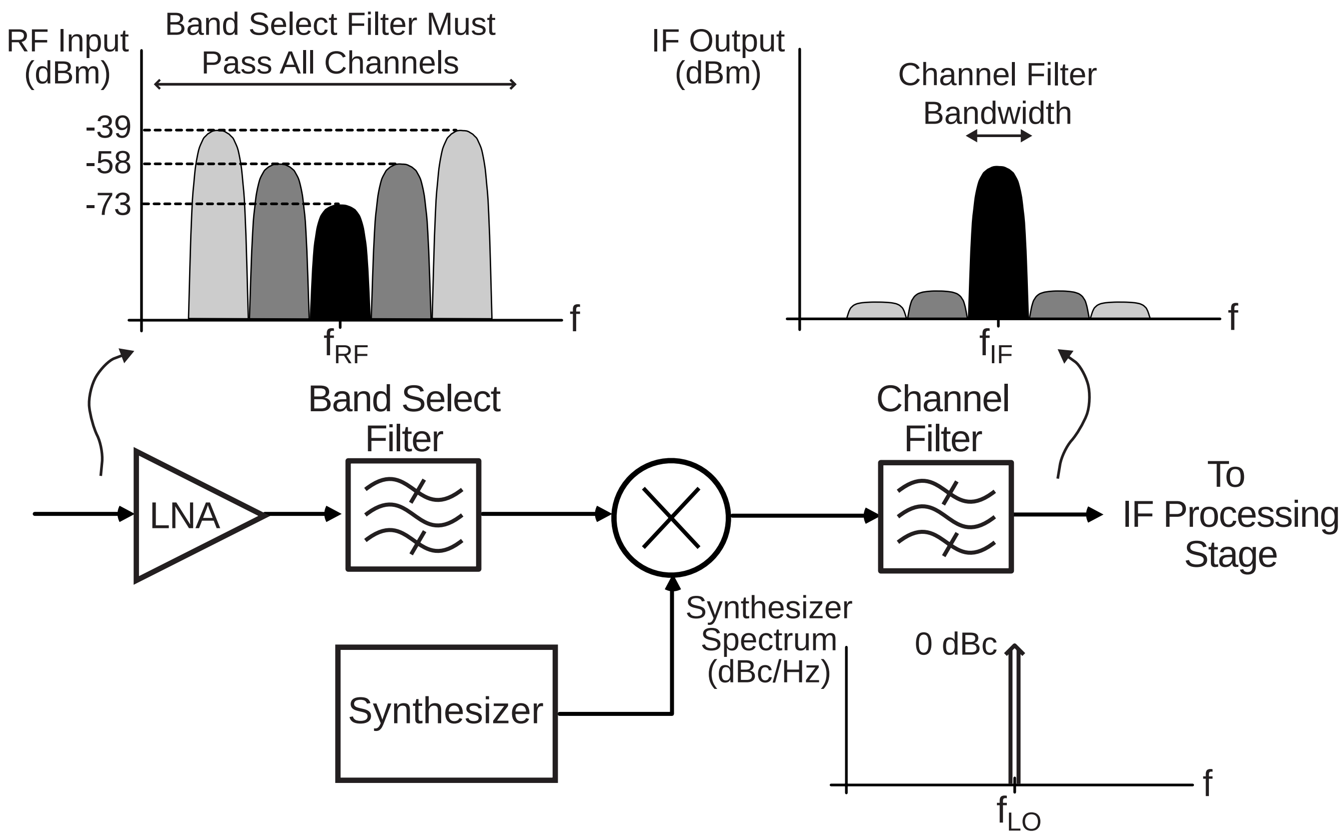


Critical Specification for Phase Noise

- **Critical specification is defined to be the one that is hardest to meet with an assumed phase noise rolloff**
  - **Assume synthesizer phase noise rolls off at -20 dB/decade**
    - Corresponds to VCO phase noise characteristic
- **For DECT transmitter synthesizer**
  - **Critical specification is -128 dBc/Hz at 5.184 MHz offset**

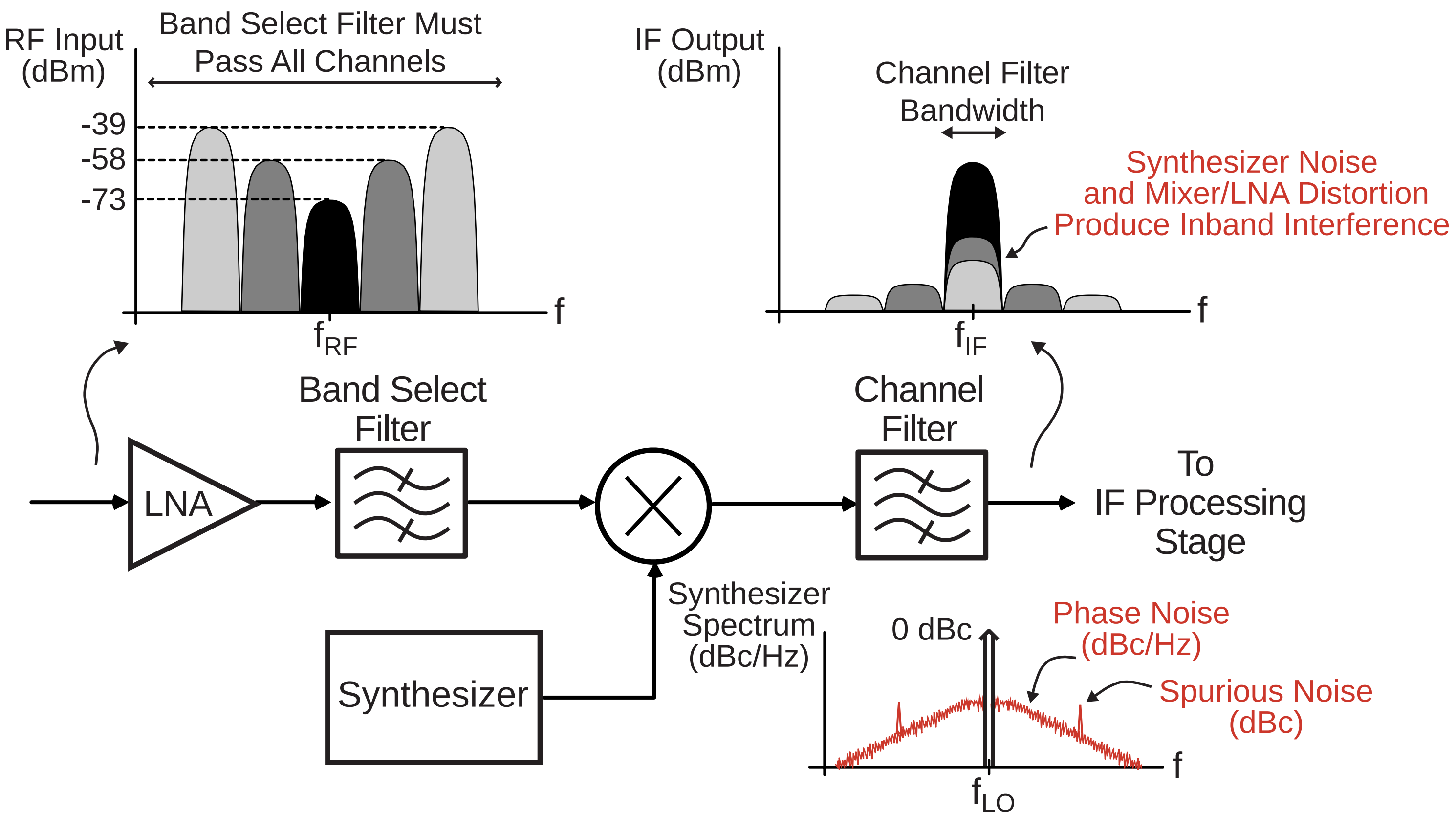


Receiver Blocking Performance



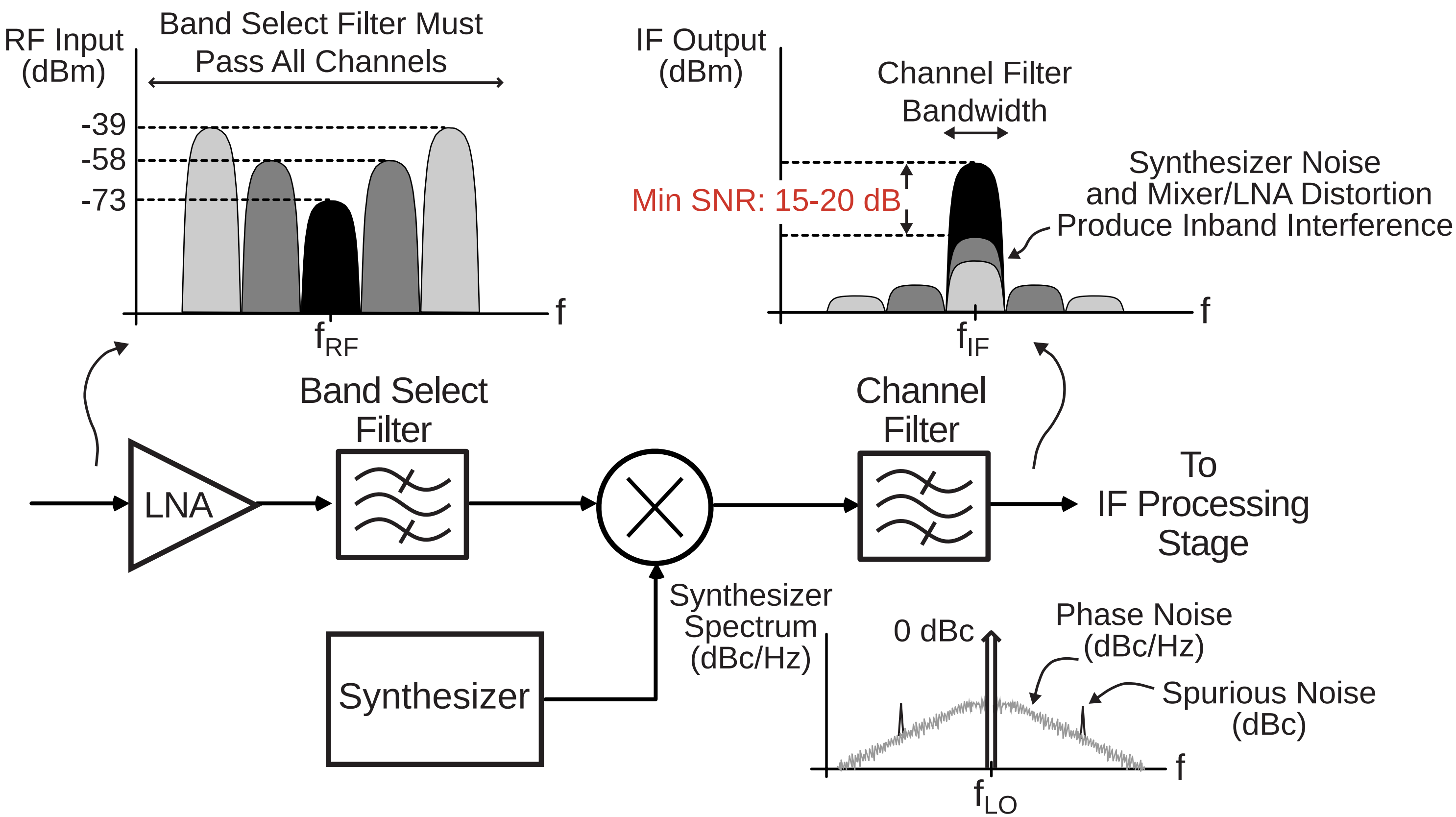
- **Radio receivers must operate in the presence of large interferers (called blockers)**
- **Channel filter plays critical role in removing blockers**
  - Passes desired signal channel, rejects interferers

Impact of Nonidealities on Blocking Performance



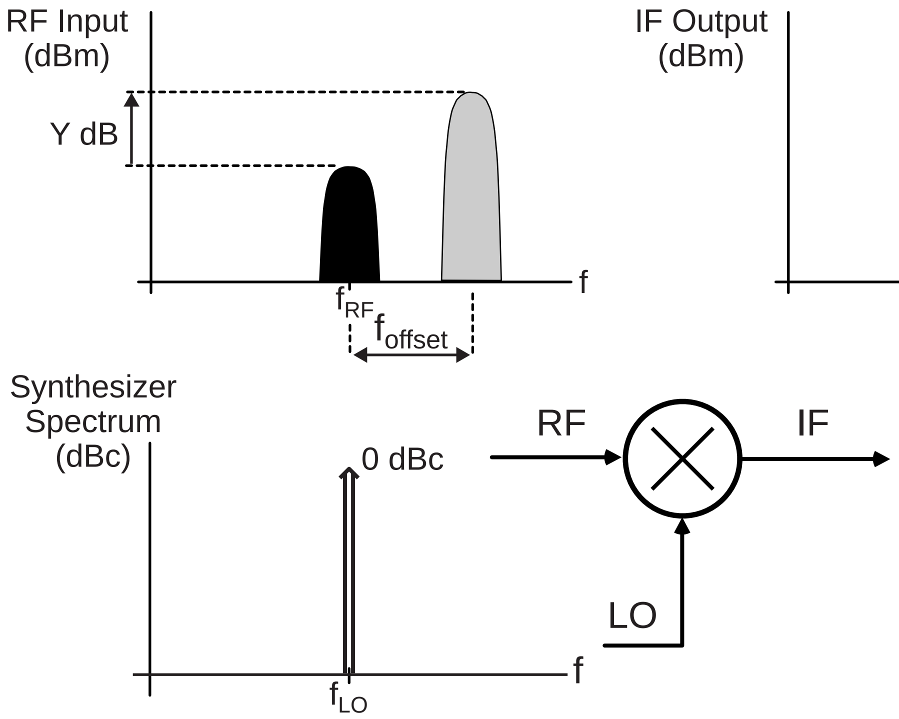
- **Blockers leak into desired band due to**
  - **Nonlinearity of LNA and mixer (IIP3)**
  - **Synthesizer phase and spurious noise**
- **In-band interference cannot be removed by channel filter!**

Quantifying Tolerable In-Band Interference Levels



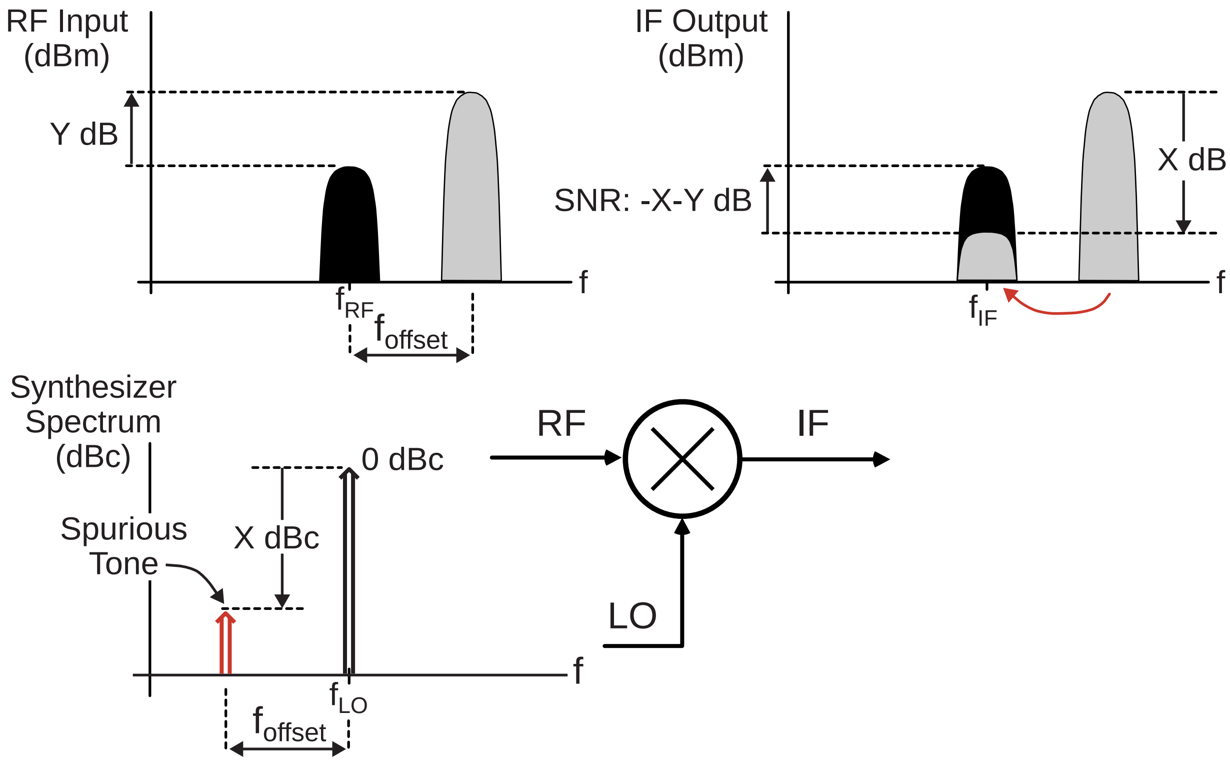
- Digital radios quantify performance with bit error rate (BER)
  - Minimum BER often set at 1e-3 for many radio systems
  - There is a corresponding minimum SNR that must be achieved
- Goal: design so that SNR with interferers is above SNR_{min}

Impact of Synthesizer on Blockers



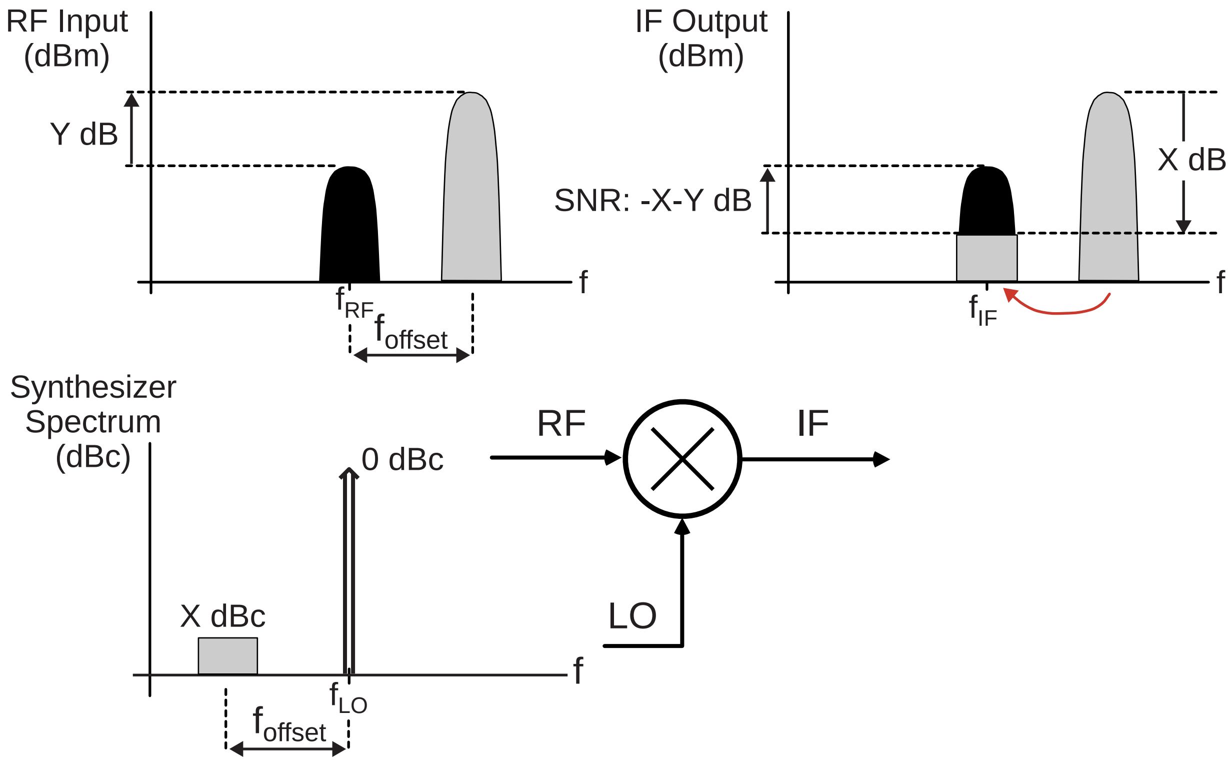
- **Synthesizer passes desired signal and blocker**
  - **Assume blocker is Y dB higher in signal power than desired signal**

Impact of Synthesizer Spurious Noise on Blockers



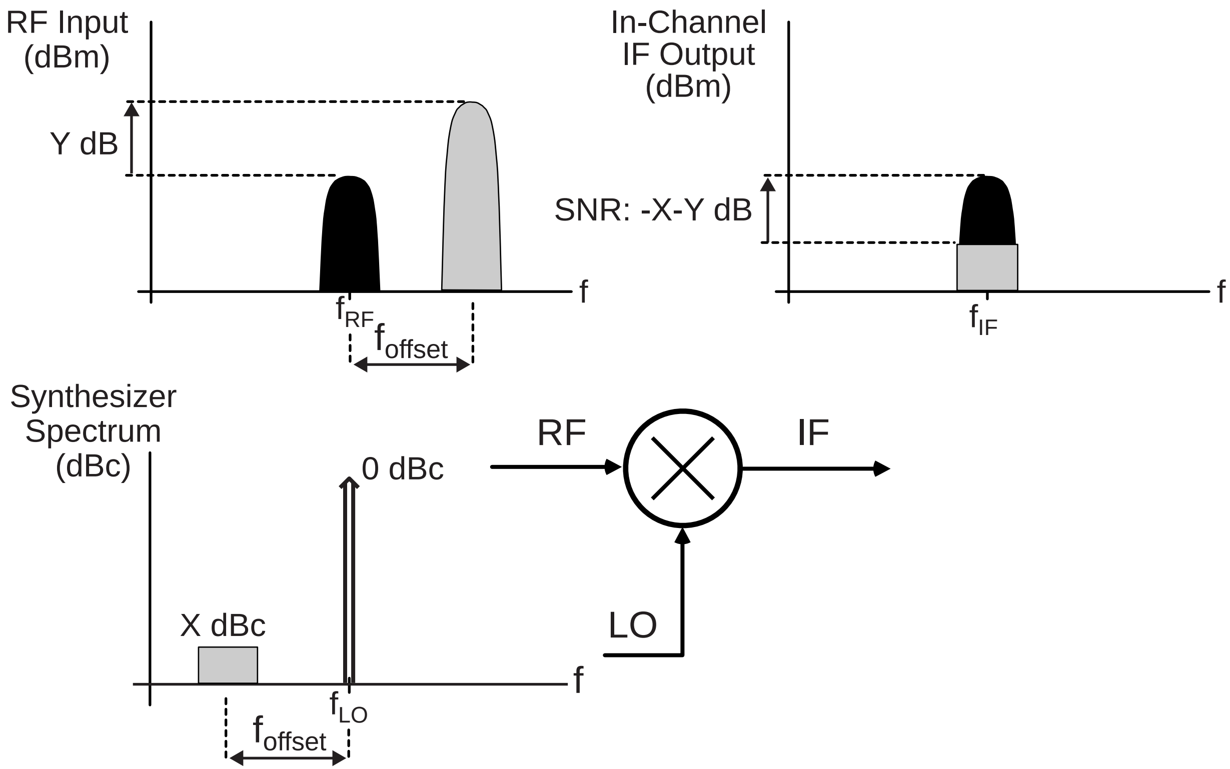
- **Spurious tones cause the blocker (Y dB) (and desired) signals to "leak" into other frequency bands**
  - **In-band interference occurs when spurious tone offset frequency is same as blocker offset frequency**
  - **Resulting SNR = -X-Y dB with spurious tone (X dBc)**

Impact of Synthesizer Phase Noise on Blockers



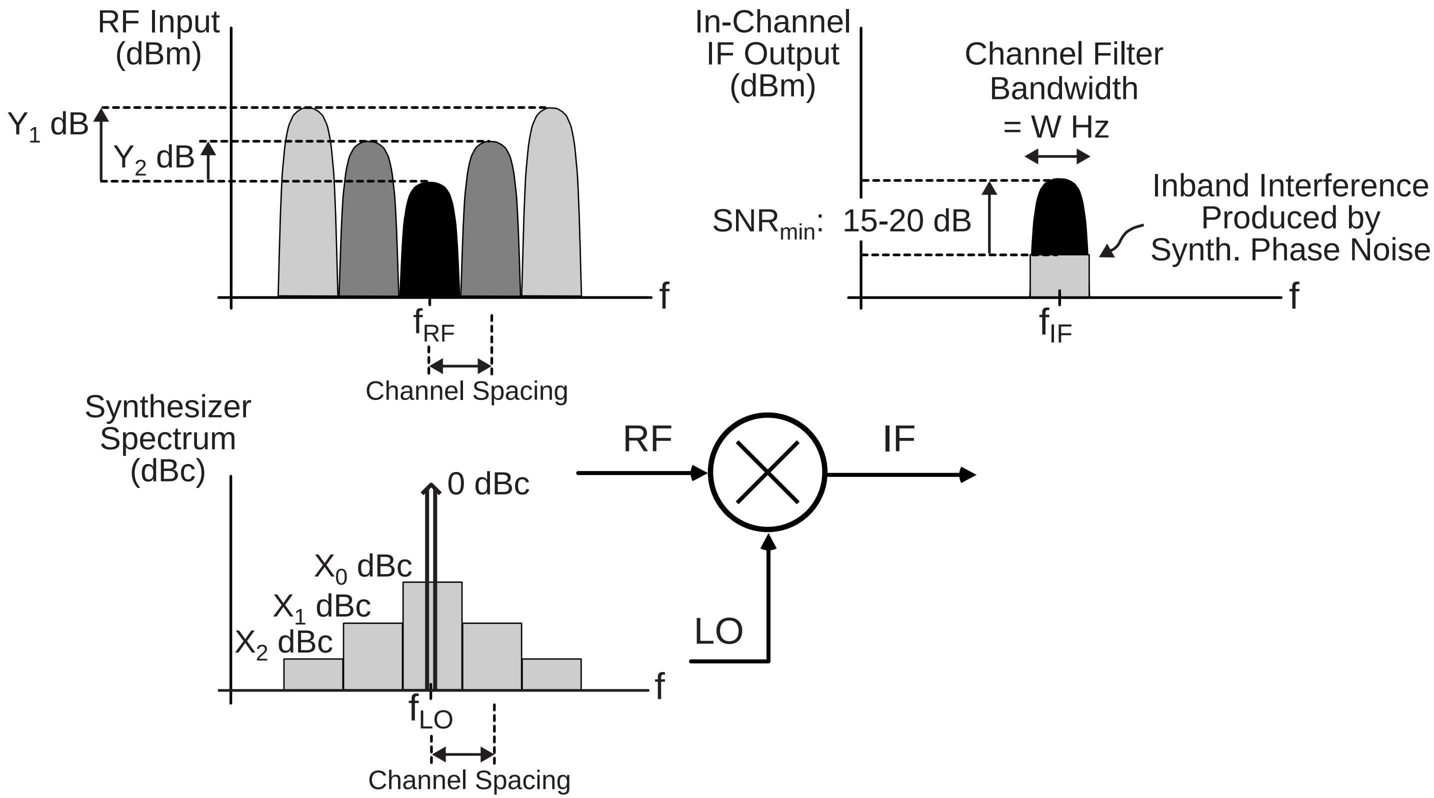
- **Same impact as spurious tone, but blocker signal is "smeared" by convolution with phase noise**
  - **For simplicity, ignore "smearing" and approximate as shown above**

Blocking Performance Analysis (Part 1)



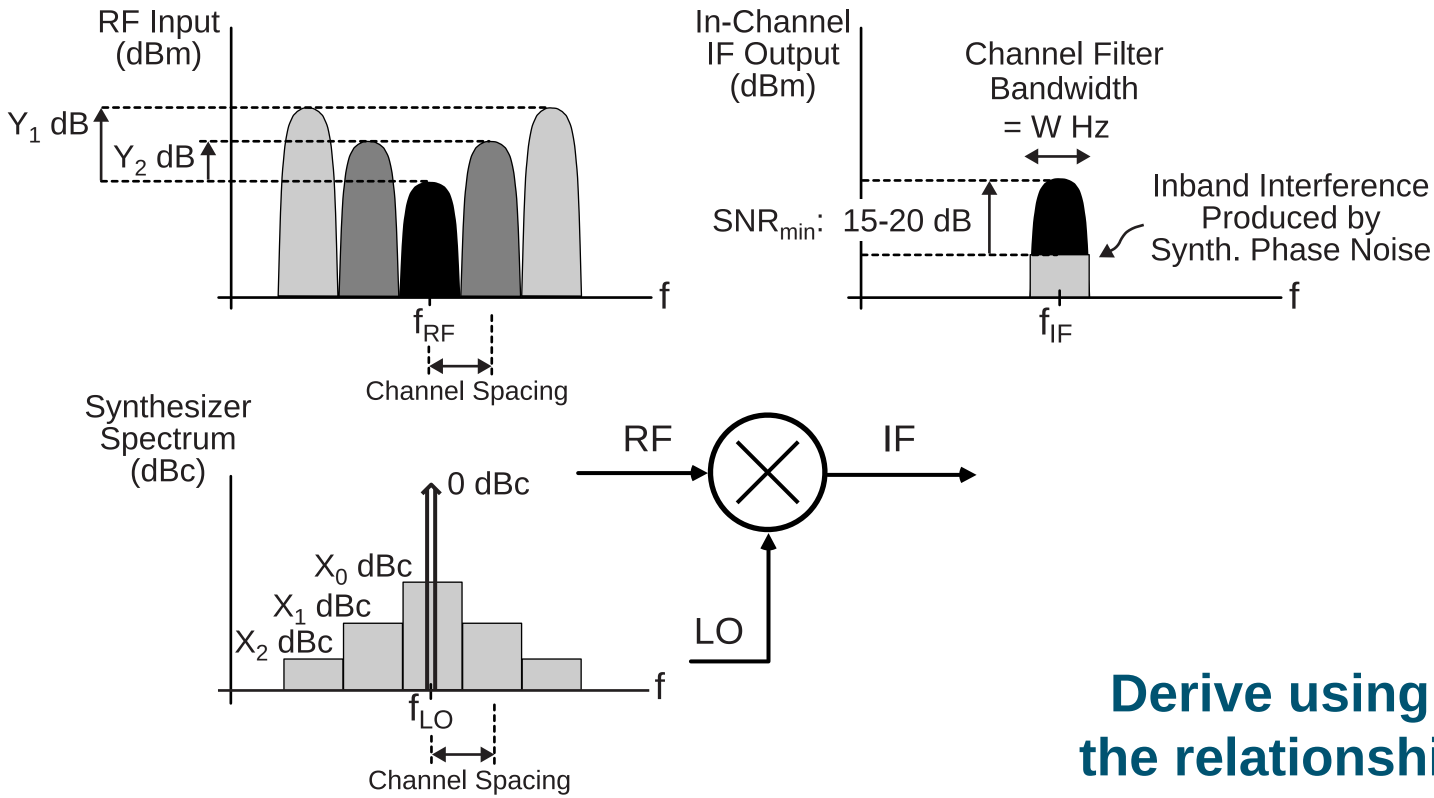
- **Ignore all out-of-band energy at the IF output**
  - **Assume that channel filter removes it**
  - **Motivation: simplifies analysis**

Blocking Performance Analysis (Part 2)



- **Consider the impact of blockers surrounding the desired signal with a given phase noise profile**
  - **SNR_{min} must be maintained**
  - **Evaluate impact on SNR one blocker at a time**

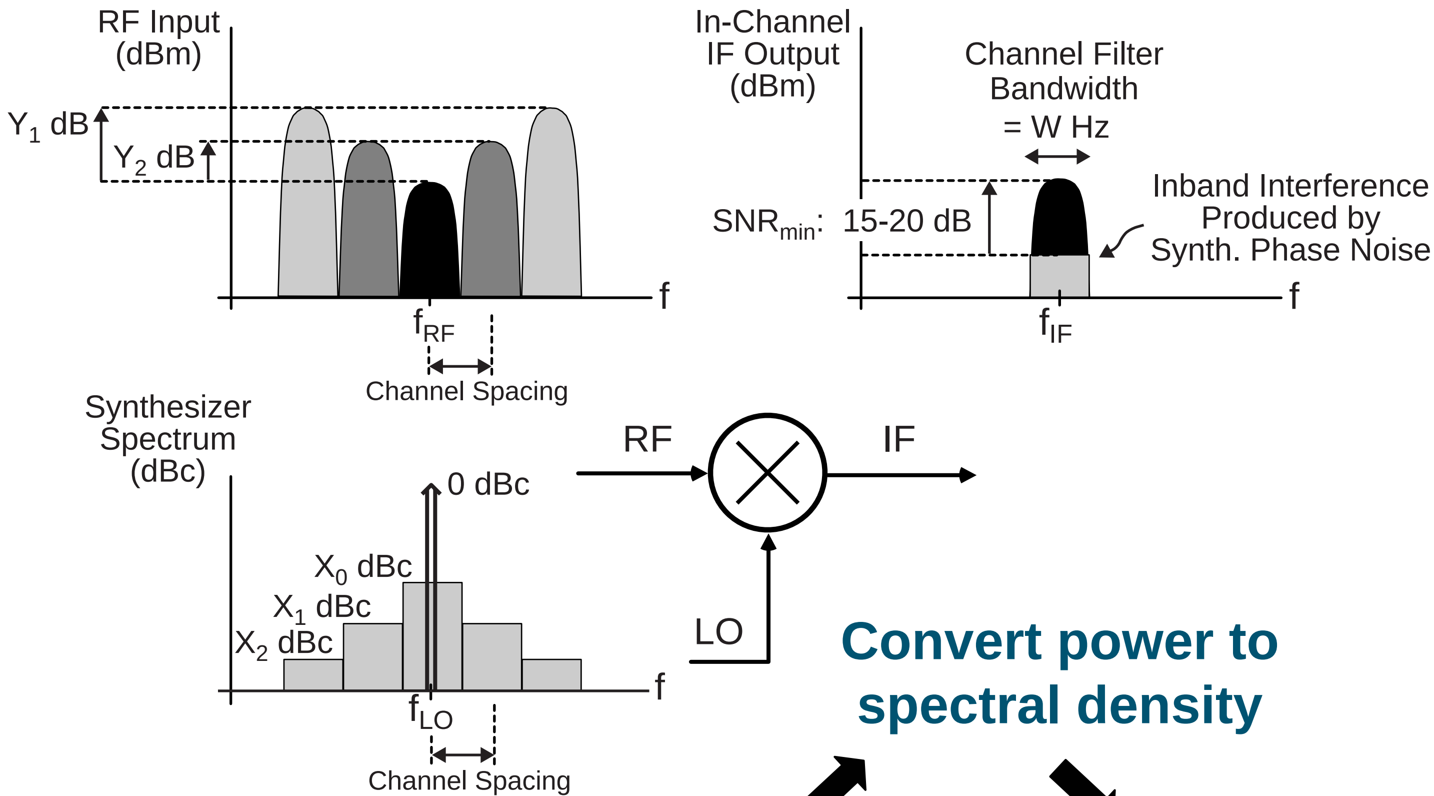
Blocking Performance Analysis (Part 3)



Derive using the relationship $SNR = -X-Y\ dB >= SNR_{min}$

Channel Offset	Relative Blocking Power	Maximum Synth. Noise Power at Channel Offset
0	0 dB	$X_0 = -SNR_{min}$ dBc
1	Y_1 dB	$X_1 = -SNR_{min}-Y_1$ dBc
2	Y_2 dB	$X_2 = -SNR_{min}-Y_2$ dBc
3	Y_3 dB	$X_3 = -SNR_{min}-Y_3$ dBc

Blocking Performance Analysis (Part 4)



Convert power to spectral density

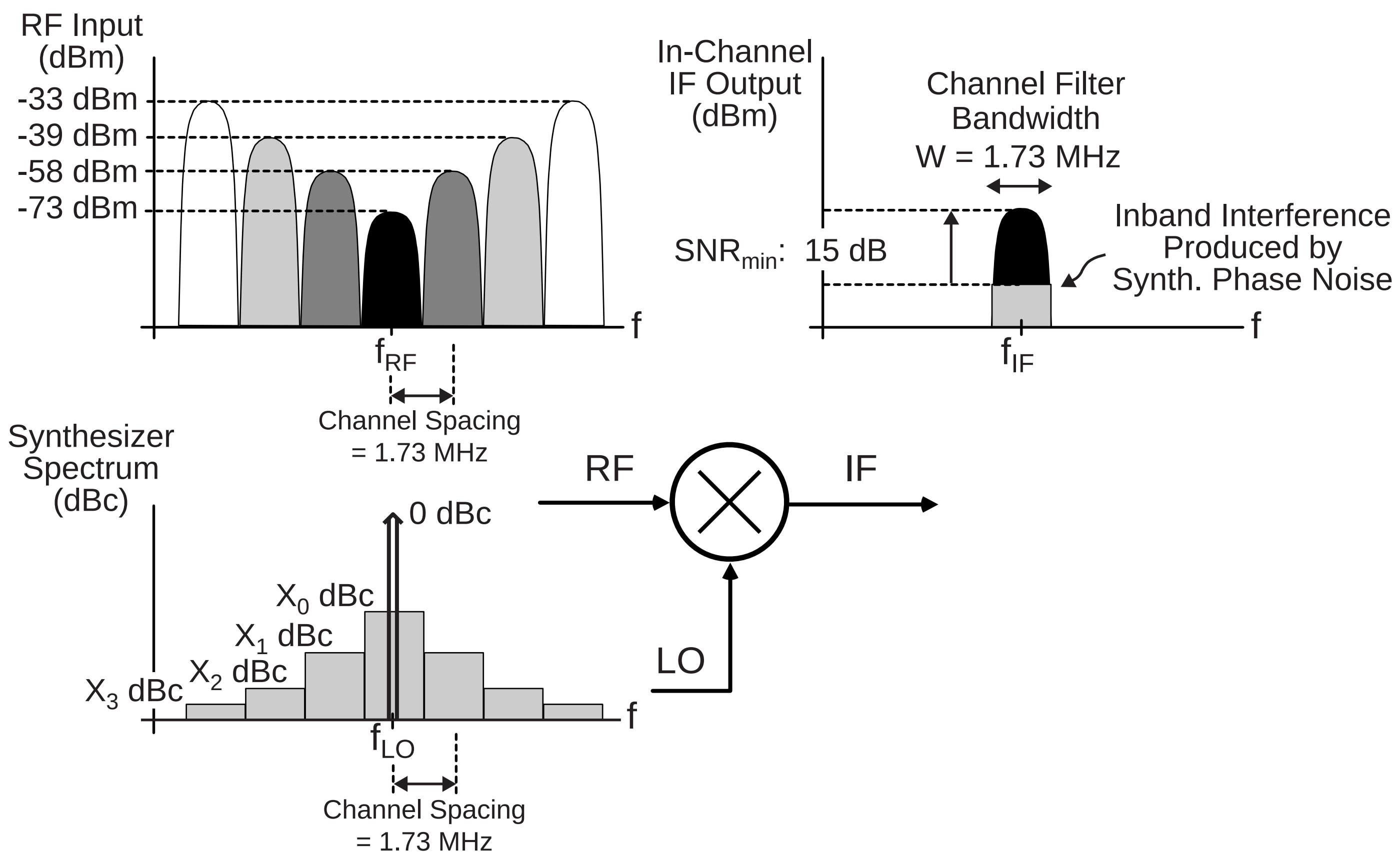
Channel Offset	Relative Blocking Power	Maximum Synth. Noise Power at Channel Offset	Maximum Synth. Phase Noise at Channel Offset
0	0 dB	X_0 = -SNR_{min} dBc	X_0 - dB(W) dBc/Hz
1	Y_1 dB	X_1 = -SNR_{min}-Y_1 dBc	X_1 - dB(W) dBc/Hz
2	Y_2 dB	X_2 = -SNR_{min}-Y_2 dBc	X_2 - dB(W) dBc/Hz
3	Y_3 dB	X_3 = -SNR_{min}-Y_3 dBc	X_3 - dB(W) dBc/Hz

Example – DECT Cordless Telephone Standard

- **Receiver blocking specifications**
  - **Channel spacing: W = 1.728 MHz**
  - **Power of desired signal for blocking test: -73 dBm**
  - **Minimum bit error rate (BER) with blockers: 1e-3**
    - Sets the value of SNR_{min}
      - Perform receiver simulations to determine SNR_{min}
    - Assume SNR_{min} = 15 dB for calculations to follow
  - **Strength of interferers for blocking test**

f_{offset} (MHz)	Blocker Power (dBm)	Relative Strength
1.728	-58 dBm	$Y_1 = 15$ dB
3.456	-39 dBm	$Y_2 = 34$ dB
5.184	-33 dBm	$Y_3 = 40$ dB

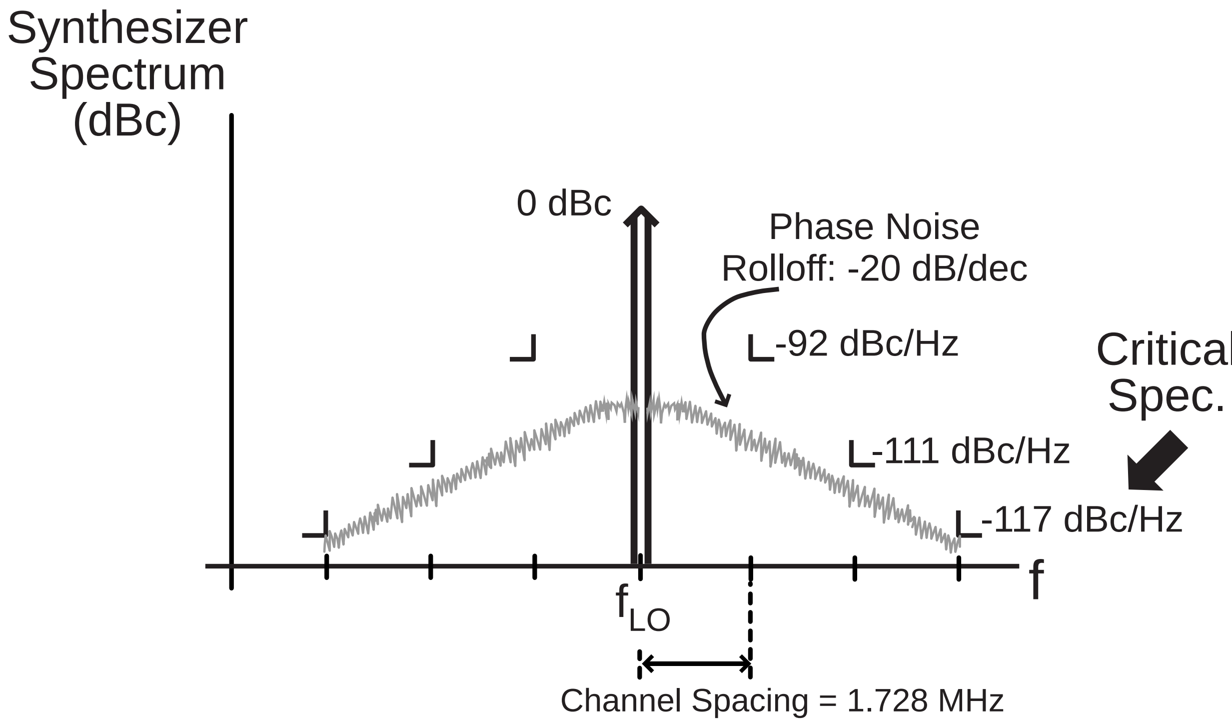
Synthesizer Phase Noise Requirements for DECT



Channel Offset	Relative Blocking Power	Maximum Synth. Noise Power at Channel Offset	Maximum Synth. Phase Noise at Channel Offset
0	0 dB	X_0 = -15 dBc	-77 dBc/Hz
1.728 MHz	Y_1 = 15 dB	X_1 = -30 dBc	-92 dBc/Hz
3.456 MHz	Y_2 = 34 dB	X_2 = -49 dBc	-111 dBc/Hz
5.184 MHz	Y_3 = 40 dB	X_3 = -55 dBc	-117 dBc/Hz

Graphical Display of Required Phase Noise Performance

- Mark phase noise requirements at each offset frequency



- Calculate critical specification for receive synthesizer
  - Critical specification is -117 dBc/Hz at 5.184 MHz offset
    - Lower performance demanded of receiver synthesizer than transmitter synthesizer in DECT applications!

Summary of Noise Analysis of Integer-N Synthesizers

- **Key PLL noise sources are**
  - **VCO noise (we will cover in detail tomorrow)**
  - **PFD-referred noise**
    - Charge pump noise, reference noise, etc.

- **Setting of PLL bandwidth has strong impact on noise**
  - **High PLL bandwidth suppresses VCO noise**
  - **Low PLL bandwidth suppresses PFD-referred noise**

- **Noise performance required of PLL depends on application**
  - **Wireless transmitter: must meek spectral mask**
  - **Wireless receiver: must suppress blockers and achieve good SNR for received signal**