A $4^{th}$ Order Continuous-Time ΔΣ ADC with VCO-Based Integrator and Quantizer

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Motivation

- A highly digital receive path is very attractive for achieving multi-standard functionality
- A key issue is achieving a wide bandwidth ADC with high resolution and low power
  - Minimal anti-alias requirements are desirable for simplicity

**Continuous-Time Sigma-Delta ADC structures have very attractive characteristics for this space**
A Basic Continuous-Time Sigma-Delta ADC Structure

- Sampling occurs at the quantizer after filtering by $H(s)$
- Quantizer noise is shaped according to choice of $H(s)$
  - High open loop gain required to achieve high SNR

We will focus on achieving an efficient implementation of the multi-level quantizer by using a ring oscillator.
Application of Ring Oscillator as an ADC Quantizer

Input: analog tuning of ring oscillator frequency
Output: count of oscillator cycles per Ref clock period

Similar approaches:
Alon, Stojanovic, Horowitz
JSSC 2005
Kim, Cho, ISCAS 2006
VCO-Based Quantizer Also Shapes Delay Mismatch

- Barrel shifting through delay elements
  - Mismatch between delay elements is first order shaped
Benefits of VCO-based Quantization

- Much more digital implementation
  - No resistor ladder or differential gain stages
- Offset and mismatch is not of critical concern
- Metastability behavior is improved

Implementation is high speed, low power, low area
Frequency Domain Model of VCO Quantizer

- VCO modeled as integrator and $K_v$ nonlinearity
- Sampling of VCO phase modeled as scale factor of $1/T$
- Quantizer modeled as addition of quantization noise

Key non-idealities:
- Quantization noise
- First order shaped!
- VCO noise
- VCO $K_v$ nonlinearity
Example SNDR with 20 MHz BW (1 GHz Sample Rate)

Simulated ADC Output Spectrum

<table>
<thead>
<tr>
<th>Conditions</th>
<th>SNDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal</td>
<td>68.2 dB</td>
</tr>
<tr>
<td>VCO Thermal Noise</td>
<td>65.4 dB</td>
</tr>
<tr>
<td>VCO Thermal + Nonlinearity</td>
<td>32.2 dB</td>
</tr>
</tbody>
</table>

VCO $K_v$ nonlinearity is key SNDR bottleneck

VCO noise: -100 dBc/Hz @ 10 MHz

$K_v$: ± 5% linearity

VCO Thermal Noise:

-20 dB/dec

Output Noise:

20 dB/dec
Place VCO-based quantizer within a continuous-time Sigma-Delta ADC structure
- Quantizer nonlinearity suppressed by preceding gain stage
A Second Order Continuous-Time Sigma-Delta ADC

- Third order noise shaping with a second order structure!

Peak SNDR limited by Kv non-linearity to 67 dB (20 MHz BW)
How Do We Overcome $K_v$ Nonlinearity to Improve SNDR?
In prior work, VCO frequency is desired output variable:
- Input must span the entire non-linear voltage-to-frequency ($K_v$) characteristic to exercise full dynamic range
- Strong distortion at extreme ends of the $K_v$ curve
**Proposed Voltage-to-Phase Approach (1st Order \( \Sigma-\Delta \))**

- VCO output *phase* is now the output variable
  - Small perturbation on \( V_{\text{tune}} \) allows large VCO phase shift
  - VCO acts as a CT integrator with *infinite* DC gain

High SNDR requires higher order \( \Sigma-\Delta \) …
Proposed 4th Order Architecture for Improved SNDR

- **Goal:** ~80 dB SNDR with 20 MHz bandwidth
  - Achievable with 4th order loop filter, 4-bit VCO-based quantizer
  - 4-bit quantizer: tradeoff resolution versus DEM overhead
- Combined frequency/phase feedback for stability/SNDR
Opamp-RC integrators
- Better linearity than Gm-C, though higher power
Schematic of Proposed Architecture

- Passive summation performed with resistors
  - Low power
  - Must design carefully to minimize impact of parasitic pole
DEM explicitly performed on phase feedback
- NRZ DAC unit elements

DEM implicitly performed on frequency feedback
- RZ DAC unit elements  (Note: Miller, US Patent (2004))
Behavioral Simulation (available at www.cppsim.com)

Key Nonidealities

- VCO Kv non-linearity
- Device noise
- Amplifier finite gain, finite BW
- DAC and VCO unit element mismatch

VCO nonlinearity is not the bottleneck for achievable SNDR!

FFT PLOT

Selected Noise, Non-Linearity: SNDR ~ 85 dB

Only VCO Kv Non-Linearity: SNDR ~ 95 dB

85 dB SNDR!

VCO nonlinearity is not the bottleneck for achievable SNDR!
Circuit Details
VCO Integrator Schematic

- 15 stage current starved ring-VCO
  - 7 stage ring-VCO shown for simplicity
  - Pseudo differential control
  - PVT variation accommodated by enable switches on PMOS/NMOS

- Rail-to-rail VCO output phase signals (VDD to GND)

Straayer, VLSI 2007
VCO Quantizer Schematic

- Phase quantization with sense-amp flip-flop
  - Single phase clocking

- Rail-to-rail quantizer output signals (VDD to GND)

Nikolic et al, JSSC 2000
**Phase Quantizer, Phase and Frequency Detector**

- **Highly digital implementation**
  - Phase sampled & quantized by SAFF
  - XOR phase and frequency detection with FF and XOR

- **Automatic DWA for frequency detector output code**
  - Must explicitly perform DWA on phase detector output code
Main Feedback DAC Schematic

- **Low-swing buffers**
  - Keeps switch devices in saturation
  - Fast “on” / Slow “off” reduces glitches at DAC output
  - Uses external Vdd/Vss

- **Resistor degeneration** minimizes 1/f noise

Yan et al
JSSC 2004
**Bit-Slice of Minor Loop RZ DAC**

- RZ DAC unit elements transition every sample period
  - Breaks code-dependency of transient mismatch (ISI)
  - Uses full-swing logic signals for switching
Opamp Schematic

Mitteregger et al, JSSC 2006

- **Modified nested Miller opamp**
  - 4 cascaded gain stages, 2 feedforward stages
  - Behaves as 2-stage Miller near cross-over frequencies
  - Opamp 1 power is 2X of opamps 2 and 3 (for low noise)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>63 dB</td>
</tr>
<tr>
<td>Unity-Gain Frequency</td>
<td>4.0 GHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>55°</td>
</tr>
<tr>
<td>Input Referred Noise Power (20 MHz BW)</td>
<td>11 uV (rms)</td>
</tr>
<tr>
<td>Power (V_{DD} = 1.5 V)</td>
<td>22.5 mW</td>
</tr>
</tbody>
</table>
**DEM Architecture (3-bit example)**

- Achieves low-delay to allow 4-bit DEM at 900 MHz
  - Code through barrel shift propagates in half a sample period

See also: Yang ISSCC 2008
Die Photo (0.13μ CMOS)

- **Active area**: 0.45 mm²
- **Sampling Freq**: 900 MHz
- **Input BW**: 20 MHz
- **Supply Voltage**: 1.5 V
- **Analog Power**: 69 mW
- **Digital Power**: 18 mW
**Measured Results**

- **78 dB Peak SNDR performance in 20 MHz**
  - Bottleneck: transient mismatch from main feedback DAC
- **Architecture robust to VCO $K_v$ non-linearity**

**Figure of Merit:** 330 fJ/Conv with 78 dB SNDR
Beahavioral Model Reveals Key Performance Issue

- Amplifier nonlinearity degrades SNDR to 81 dB
- DAC transient mismatch degrades SNDR to 78 dB
  - DEM does not help
  - Could be improved with dual RZ structure

Transient DAC mismatch is likely the key bottleneck
Conclusion

- VCO-based quantization is a promising component to achieve high performance $\Sigma-\Delta$ ADC structures
  - High speed, low power, low area implementation
  - First order shaping of quantization noise and mismatch
  - Kv non-linearity was a limitation in previous approaches

- Demonstrated a 4$^{th}$-order CT $\Delta\Sigma$ ADC with a VCO-based integrator and quantizer
  - Proposed voltage-to-phase conversion to avoid distortion from Kv non-linearity
  - Achieved 78 dB SNDR in 20 MHz BW with 87 mW power
    - Key performance bottleneck: transient DAC mismatch