Analysis and Design of Analog Integrated Circuits
Lecture 7

Differential Amplifiers

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Review Proposed Thevenin CMOS Transistor Model

Hybrid-π Model

Key Small-Signal Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Strong Inversion</th>
<th>Weak Inversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>$\sqrt{2\mu_mC_{ox}(W/L)}I_D$</td>
<td>$qI_D/nkT$</td>
</tr>
<tr>
<td>$g_{mb}$</td>
<td>$\frac{\gamma g_m}{2\sqrt{2</td>
<td>\Phi_F</td>
</tr>
</tbody>
</table>

Thevenin Resistances

Exact

$R_{th_d} = r_o (1 + (g_m + g_{mb})R_S) + R_S$

$R_{th_g} = \infty$

$R_{th_s} = (1 + R_D/r_o)(r_o \| \frac{1}{g_m + g_{mb}})$

Approximation ($g_{mb} \ll g_m, g_m r_o \gg 1$)

$R_{th_d} = r_o (1 + g_m R_S)$

$R_{th_g} = \infty$

$R_{th_s} = \frac{1 + R_D}{g_m} \approx \frac{1}{g_m}$ \hspace{1cm} ($R_D \ll r_o$)

Proposed Small Signal Transistor Model

Exact

$A_v = g_m r_o \frac{g_m}{g_m + g_{mb}}$

$\alpha = 1 + R_D/R_{th_d}$

Approximation

$A_v = 1 (g_{mb} \ll g_m, g_m r_o \gg 1)$

$\alpha = 1 (R_D \ll r_o)$
Key Observations

- For calculations focusing on signal flow from gate or source to the drain
  - Observe that current through $R_d$ equals $i_s$
    - True since $\alpha \cdot \frac{R_{thd}}{R_d + R_{thd}} = 1$
    - You can avoid doing calculations involving $\alpha$ or $R_{thd}$
  - For calculations focusing on signal flow from the drain
    - Drain simply looks like impedance $R_{thd}$
Basic Single-Stage Amplifiers and Current Mirrors

Common Source

\[ V_{in} \rightarrow M_1 \xrightarrow{\frac{W_1}{L}} \quad Z_L \rightarrow V_{out} \downarrow i_d \]

Common Source with Source Degeneration

\[ V_{in} \rightarrow M_1 \xrightarrow{\frac{W_1}{L}} \quad Z_L \rightarrow V_{out} \downarrow i_d \]

Common Gate

\[ Z_L \rightarrow V_{out} \downarrow i_d \]

Source Follower

\[ V_{in} \rightarrow M_1 \xrightarrow{\frac{W_1}{L}} Z_L \xrightarrow{V_{out}} \]

Current Mirror

\[ \xrightarrow{i_{in}} \xrightarrow{i_{out}} \]

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Today We Will Look At Differential Amplifiers

Common Source

```
Source
V_in
\[ \frac{W_1}{L} \]
M_1
```

```
Z_L
V_{in}
\[ \frac{W_1}{L} \]
M_1
```

```
\[ i_d \]
```

\[ V_{out} \]

Common Source with Source Degeneration

```
Source
V_in
\[ \frac{W_1}{L} \]
M_1
```

```
Z_L
V_{in}
\[ \frac{W_1}{L} \]
M_1
```

```
\[ i_d \]
```

\[ V_{out} \]

Common Gate

```
Source
Vin+
Vin-
```

```
Z_L
V_{in}
\[ \frac{W_1}{L} \]
M_1
```

```
\[ i_d \]
```

\[ V_{out} \]

Source Follower

```
Source
\[ V_{in} \]
M_1
W_1
L
V_{out}
```

```
Z_L
```

Current Mirror

```
V_{in+}
Vin-
```

```
Z_L
V_{o-}
V_{o+}
```

```
I_{bias}
```

Differential Amplifier

```
Z_L
```

```
W_2
L
\[ M_2 \]
W_1
L
\[ M_1 \]
```

```
V_{in+}
V_{in-}
```
Consider positive and negative input terminal signals $V_{i^+}$ and $V_{i^-}$

Define differential signal as: $V_{id} = V_{in^+} - V_{in^-}$

Define common mode signal as: $V_{ic} = (V_{in^+} + V_{in^-})/2$

We can create arbitrary $V_{i^+}$ and $V_{i^-}$ signals from differential and common mode components:

\[
V_{in^+} = V_{ic} + \frac{1}{2} V_{id} \quad V_{in^-} = V_{ic} - \frac{1}{2} V_{id}
\]

This also applies to differential output signals:

\[
V_{o^+} = V_{oc} + \frac{1}{2} V_{od} \quad V_{o^-} = V_{oc} - \frac{1}{2} V_{od}
\]
Differential Amplifier

- Useful for amplifying signals in the presence of noise
  - Common-mode noise is rejected
- Useful for high speed digital circuits
  - Low voltage swing allows faster gate/buffer performance
• Small signal analysis assumes linearity
  - Impact of M₄ on amplifier is to simply present its drain impedance to the diff pair transistors (M₁ and M₂)
  - Impact of V_{in+} and V_{in-} can be evaluated separately and then added (i.e., superposition)
    - By symmetry, we need only determine impact of V_{in+}
      - Calculation of V_{in-} impact directly follows
Calculate Impact of $V_{in+}$ using Thevenin Models

- Analysis follows fairly easily, but there is a simpler way!
Method 2 of Differential Amplifier Analysis

- Partition input signals into common-mode and differential components
- By superposition, we can add the results to determine the overall impact of the input signals
Differential Analysis

- **Key observations**
  - Inputs are equal in magnitude but opposite in sign to each other
  - By linearity and symmetry, $i_{s1}$ must equal $-i_{s2}$
    - This implies $i_R$ is zero, so that voltage drop across $r_{o4}$ is zero
      - The sources of $M_1$ and $M_2$ are therefore at incremental ground and decoupled from each other!
  - Analysis can now be done on identical “half-circuits”

- What is the **differential** DC gain?
Common Mode Analysis

- Key observations
  - Inputs are equal to each other
  - By linearity and symmetry, $i_{s1}$ must equal $i_{s2}$
    - This implies $i_R = 2i_{s1} = 2i_{s2}$
  - We can view $r_{o4}$ as two parallel resistors that have equal current running through them
- Analysis can also be done on two identical half-circuits

What is the common mode DC gain?
Useful Metric for Differential Amplifiers: CMRR

- **Common Mode Rejection Ratio (CMRR)**
  - Define: $a_{vd}$: differential gain, $a_{vc}$: common mode gain
  $$CMRR = \left( \frac{a_{vd}}{a_{vc}} \right)$$
  - CMRR corresponds to ratio of differential to common mode gain and is related to received signal-to-noise ratio

$$V_{od} = a_{vd} V_{sig} + a_{vc} V_{noise}$$

$$\Rightarrow \frac{Signal}{Noise} = \left( \frac{a_{vd}}{a_{vc}} \right) \left( \frac{V_{sig}}{V_{noise}} \right) = CMRR \left( \frac{V_{sig}}{V_{noise}} \right)$$
Another Useful Metric for Differential Amplifiers: PSRR

- **Power Supply Rejection Ratio (PSRR)**
  - $a_{vd}$: differential gain
  - $a_{vp+}$: positive power supply gain
  - $a_{vp-}$: negative power supply gain

\[
\text{PSRR}^+ = \left( \frac{a_{vd}}{a_{vp+}} \right) \quad \text{PSRR}^- = \left( \frac{a_{vd}}{a_{vp-}} \right)
\]
Example: Calculate CMRR and PSRR

- First determine $a_{vd}$, $a_{vc}$, $a_{vp+}$, and $a_{vp-}$
- Then calculate CMRR and PSRR
  - Note that CMRR and PSRR are often expressed in dB
    - Example: $\text{CMRR} = 20\log\left(\frac{a_{vd}}{a_{vc}}\right)$
While keeping all devices in saturation:

- What is the maximum common mode output range?
  - Assume $V_{id} = 0$

- What is the maximum common mode input range?
  - Assume $V_{od} = 0$
**Large Signal Behavior of Differential Mode Operation**

\[ \text{Note: above analysis assumes strong inversion} \]