

***Analysis and Design of Analog Integrated Circuits***  
***Lecture 6***

***Current Mirrors***

**Michael H. Perrott**

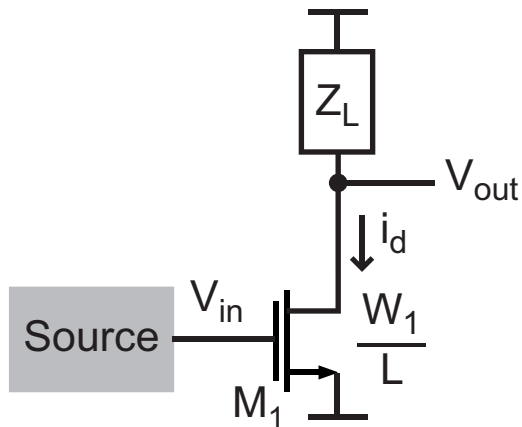
**February 9, 2011**

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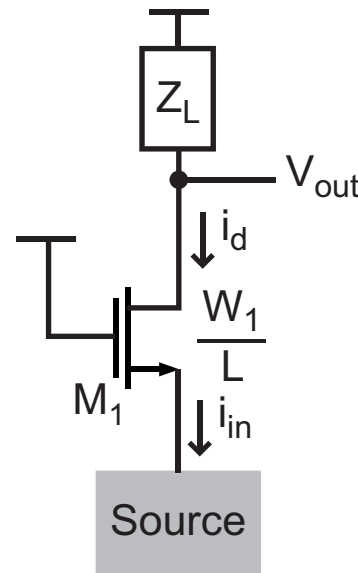
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# From Lecture 5: Basic Single-Stage CMOS Amplifiers

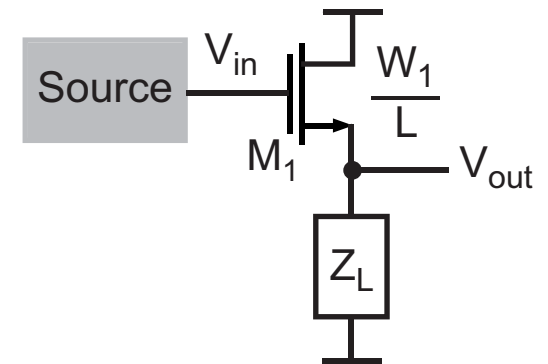
### Common Source



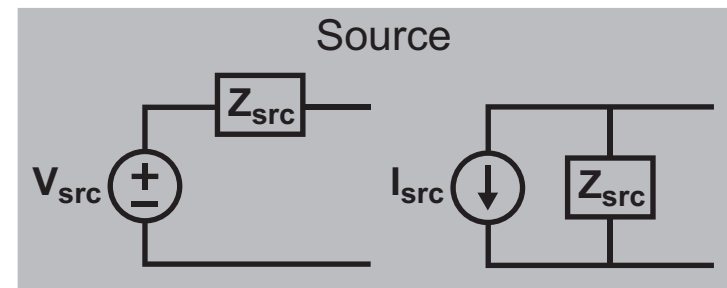
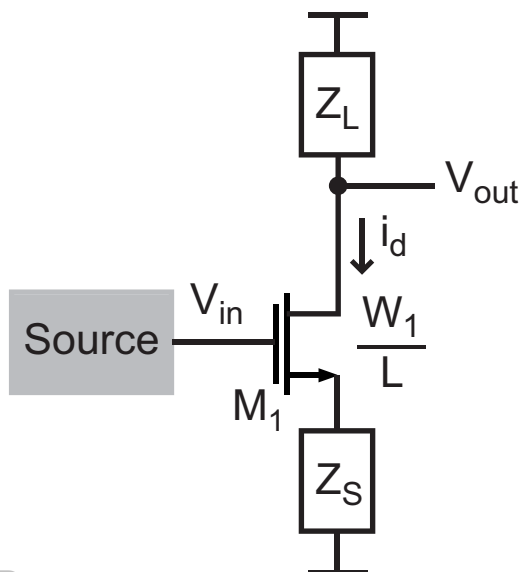
### Common Gate



### Source Follower

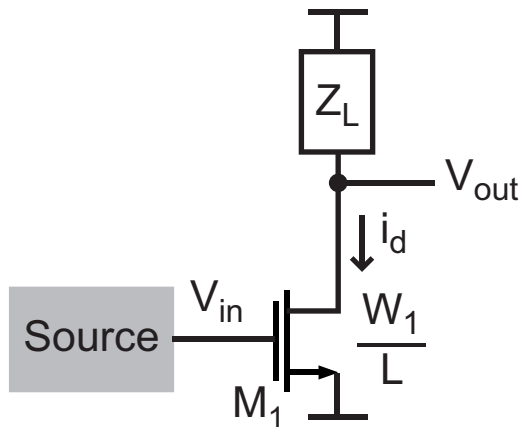


### Common Source with Source Degeneration

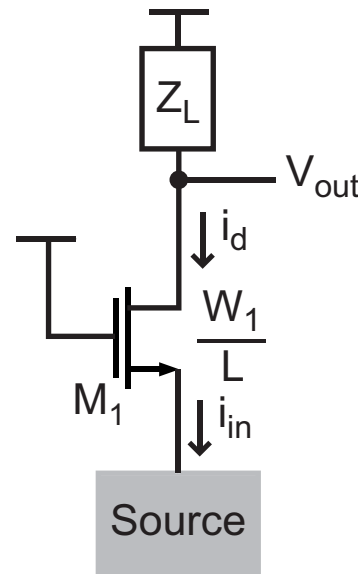


# A Closer Look at Load Impedance

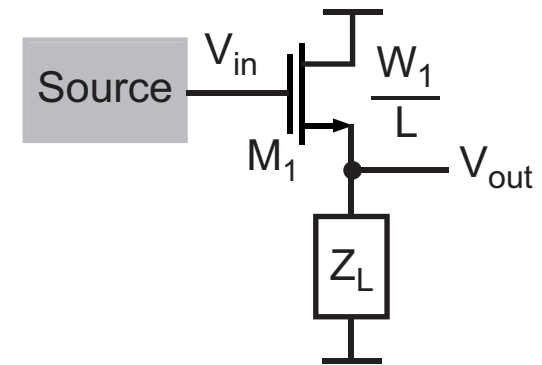
Common Source



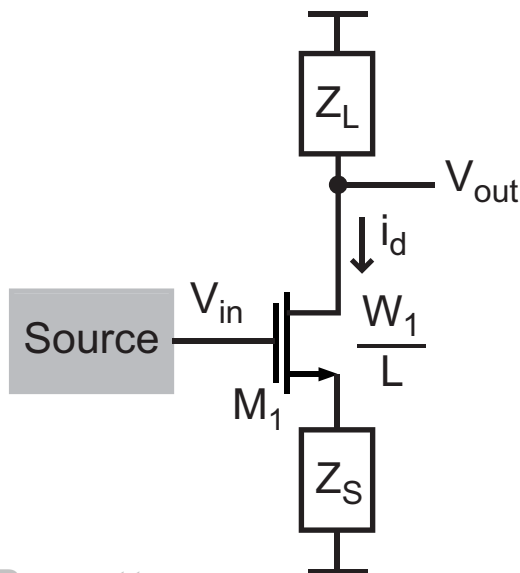
Common Gate



Source Follower

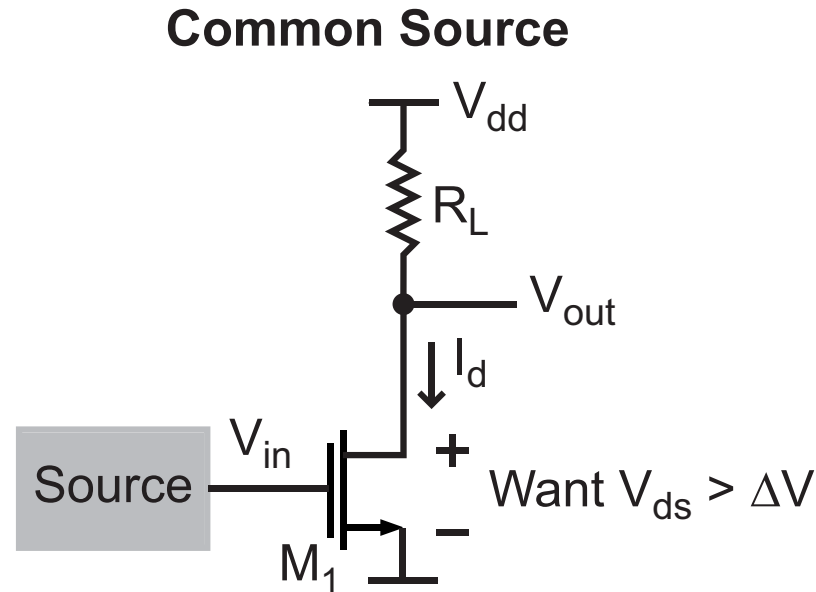


Common Source with Source Degeneration



- To achieve high gain (or low attenuation in the case of a source follower), it is very desirable to achieve high load impedance,  $Z_L$ 
  - Unfortunately, using a simple resistor of high value has issues
    - What are these issues?

# Issue #1: Headroom Limitations



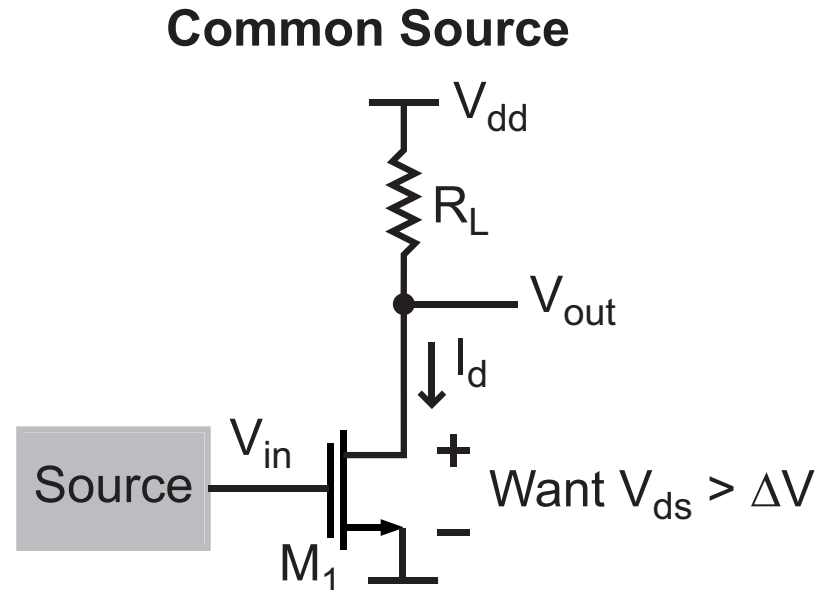
- The bias current of the device is a direct function of  $R_L$

$$I_d = \frac{V_{dd} - V_{ds}}{R_L}$$

- $V_{dd}$  is  $< 3.6V$  for most modern CMOS processes
- $V_{ds}$  must be greater than  $\Delta V$  to maintain device saturation

**Large  $R_L$  implies small  $I_d$   
(implies small  $g_m$ , poor frequency response, etc.)**

## Issue #2: Area of Circuit

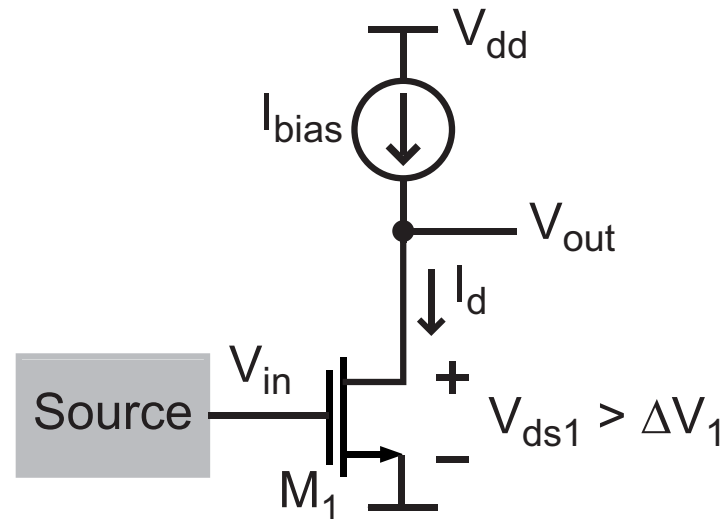


- The most common resistors for precision analog circuits are often based on unsilicided polysilicon layers
  - The sheet resistance of unsilicided polysilicon is often  $< 1\text{k}\Omega/\text{square}$

Large polysilicon  $R_L$  implies relatively large circuit area  
(implies high relative cost)

# An Elegant Approach to Achieving High Gain

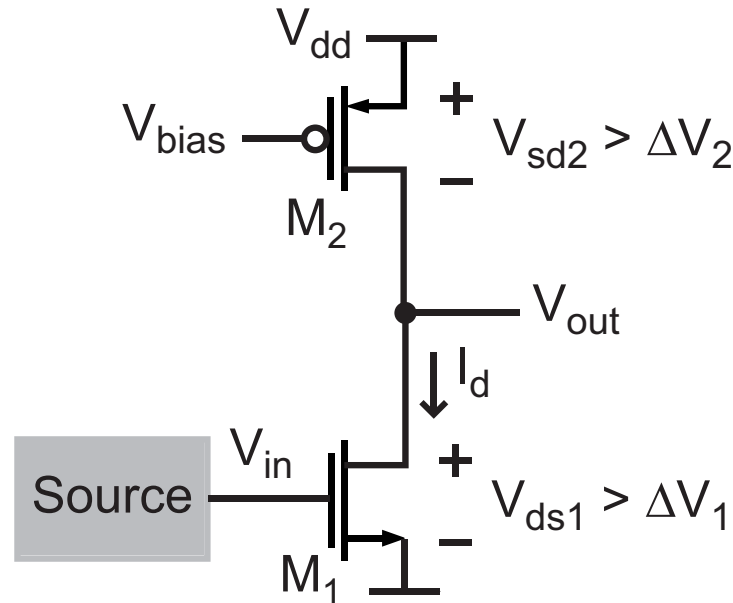
## Common Source



- Replacement of resistor load with a current source yields the highest possible DC gain out of the amplifier
  - Current source determines  $I_d$  of device
- We can make current sources out of transistors
  - Generally smaller area than polysilicon resistors

What is the small signal gain of the above circuit?

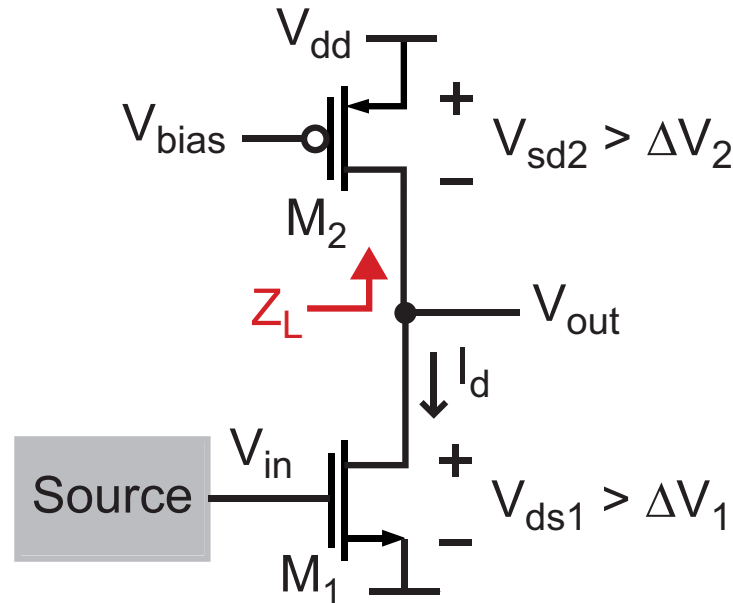
# A Simple Transistor Based Current Source



- **Simply use a PMOS load that is properly biased**
  - If we keep the PMOS in saturation, its current is relatively constant despite  $V_{sd}$  variations
    - This is the desired behavior of a current source

**What are the nonideal issues of the above approach?**

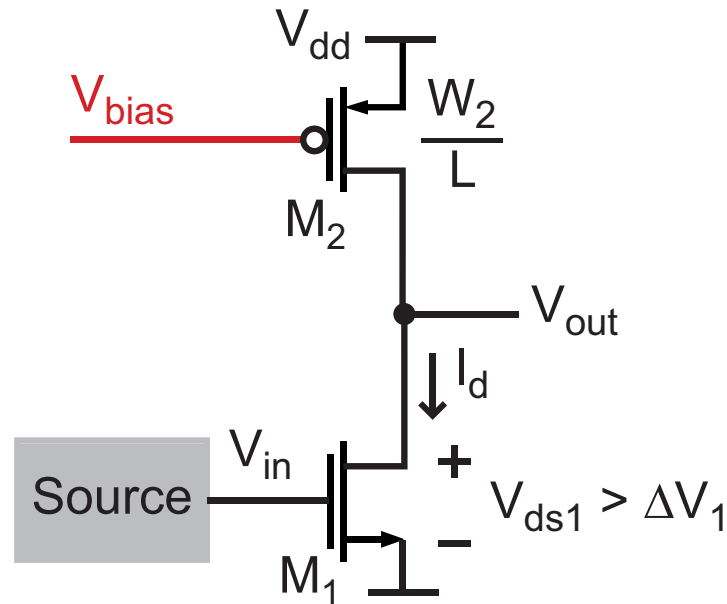
# Issue #1: Impedance of PMOS Device



- An ideal current source has infinite impedance
- PMOS devices have finite impedance
  - What is Z<sub>L</sub> in the above circuit?
  - How does finite Z<sub>L</sub> impact the gain of the circuit?

We will later examine techniques to increase Z<sub>L</sub>

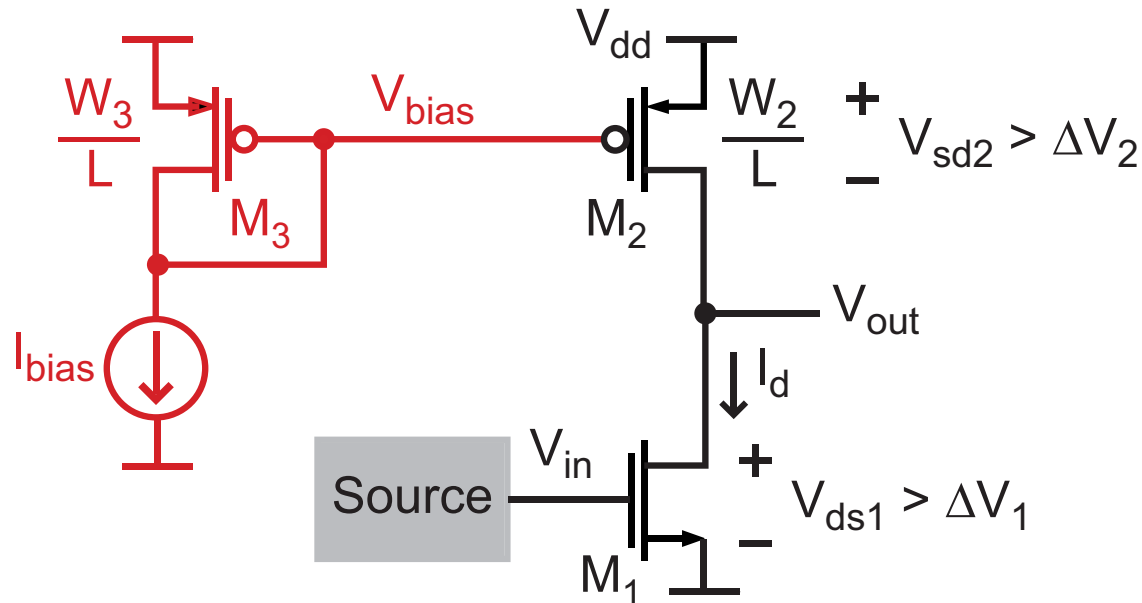
# Issue #1: High Bias Sensitivity



- The PMOS device current,  $I_d$ , is very sensitive to the value of  $V_{bias}$ 
  - We want  $I_d$  to be relatively constant across temperature and process variations

How can we achieve tighter control over  $I_d$  across temperature and process variations?

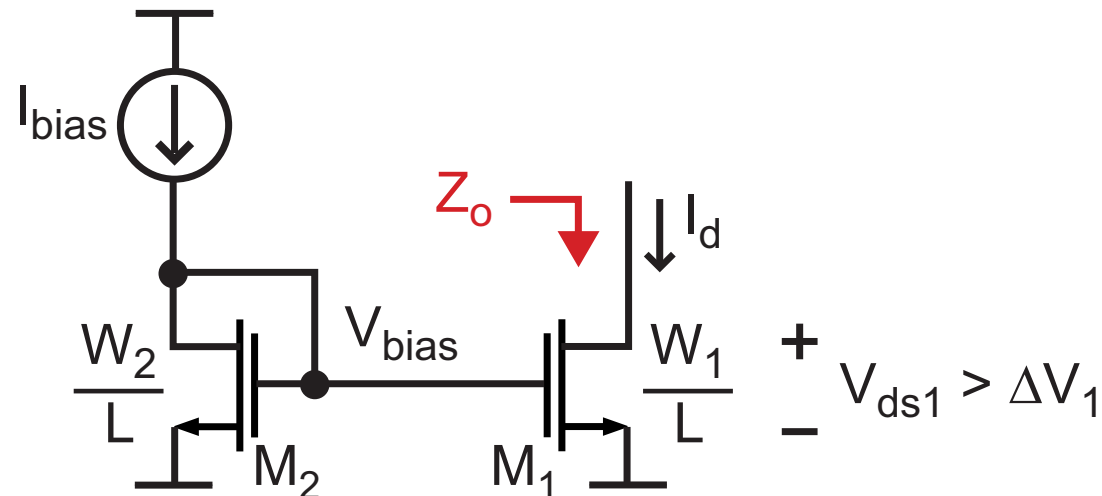
## Key Technique: Use Current Mirror



- **Key idea:** use a different PMOS device,  $M_3$ , to transform a bias current,  $I_{bias}$ , into bias voltage,  $V_{bias}$ 
  - $V_{bias}$  now yields a consistent current,  $I_d$ , in  $M_2$  (assumed to be in saturation) across temperature and process variations
  - Note that layout of  $M_2$  and  $M_3$  must be done properly to achieve good device matching

How does  $I_d$  relate to  $I_{bias}$ ?

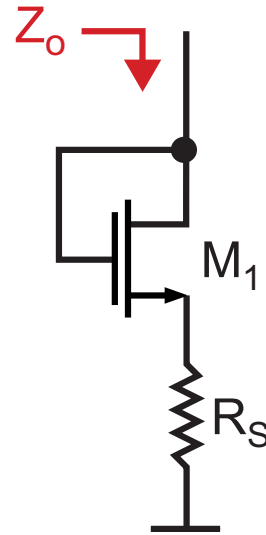
## NMOS Devices Can Also Be Used for Current Mirrors



- We often use both NMOS and PMOS versions in designs
  - We'll explore this issue further later in the semester
- General issue: current mirrors involve direct feedback between drain and gate

Can we apply proposed Thevenin modeling approach to current mirrors?

## Issue: Thevenin Impedances Are Not Adequate



- Looking as purely Thevenin impedances

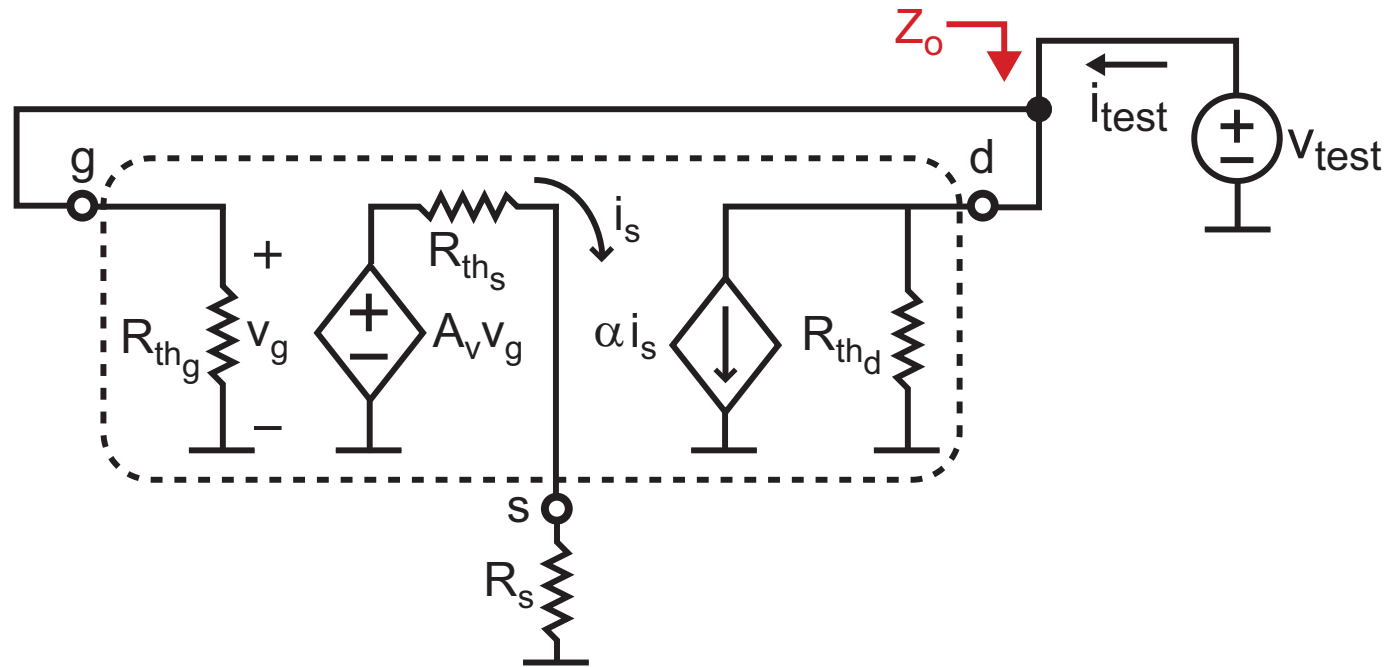
$$Z_o = R_{th_d} || R_{th_g} = r_o(1 + g_m R_s) || \infty = r_o(1 + g_m R_s)$$

- But, in reality

$$Z_o = \frac{1}{g_m} + \left( \frac{g_m + g_{mb}}{g_m} \right) R_s$$

- Issue: coupling between source, drain, or gate
  - Do we have to abandon the Thevenin method?

## Try Proposed Thevenin Model



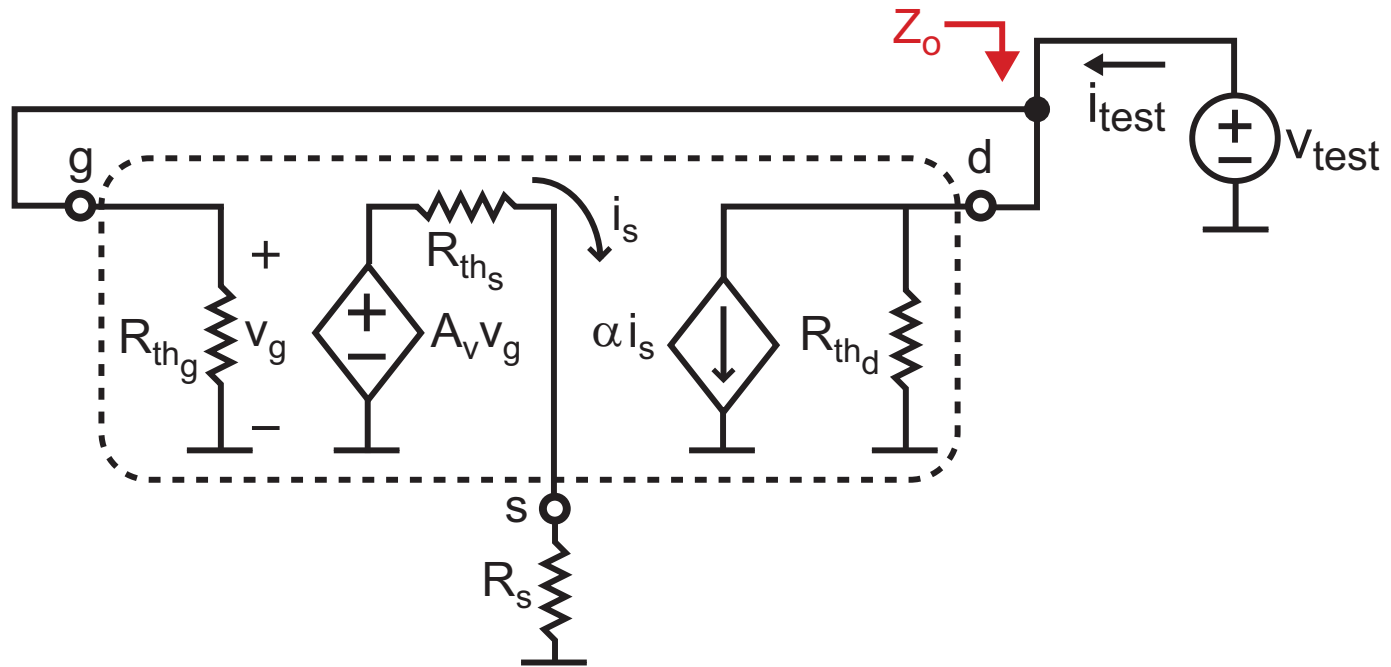
- **Key Calculations (ignore  $R_{thd}$  for now):**

$$R_{thg} = \infty, \quad R_{ths} \approx \frac{1}{g_m + g_{mb}}, \quad A_v \approx \frac{g_m}{g_m + g_{mb}}, \quad \alpha = 1$$

$$\Rightarrow i_{test} = \alpha i_s = v_{test} A_v \frac{1}{R_{ths} + R_s} = v_{test} \frac{g_m}{1 + R_s(g_m + g_{mb})}$$

$$\Rightarrow Z_o = \frac{v_t}{i_t} = \frac{1}{g_m} + \left( \frac{g_m + g_{mb}}{g_m} \right) R_s$$

# Proposed Thevenin Model Works!



## ■ Now include $R_{th_d}$ :

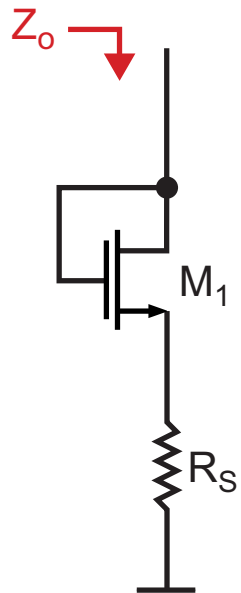
$$\Rightarrow Z_o = \left( \frac{1}{g_m} + \left( \frac{g_m + g_{mb}}{g_m} \right) R_s \right) \parallel R_{th_d}$$

However:  $R_{th_d} = r_o(1 + g_m R_s) \gg \frac{1}{g_m} + \left( \frac{g_m + g_{mb}}{g_m} \right) R_s$  for  $g_m r_o \gg 1$

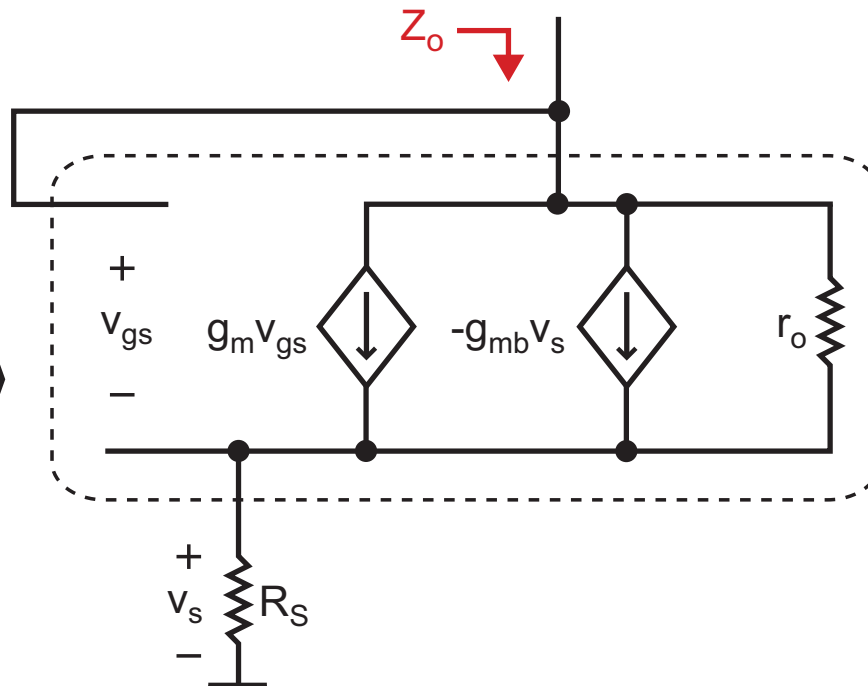
$$\Rightarrow Z_o = \frac{1}{g_m} + \left( \frac{g_m + g_{mb}}{g_m} \right) R_s$$

# Check Thevenin Resistance Calculation

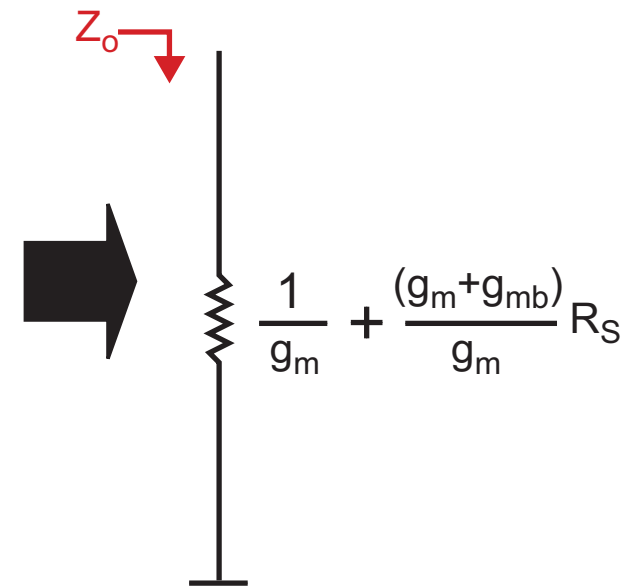
Diode-Connected Device



Derive  $Z_o$  Using Hybrid- $\pi$  Model



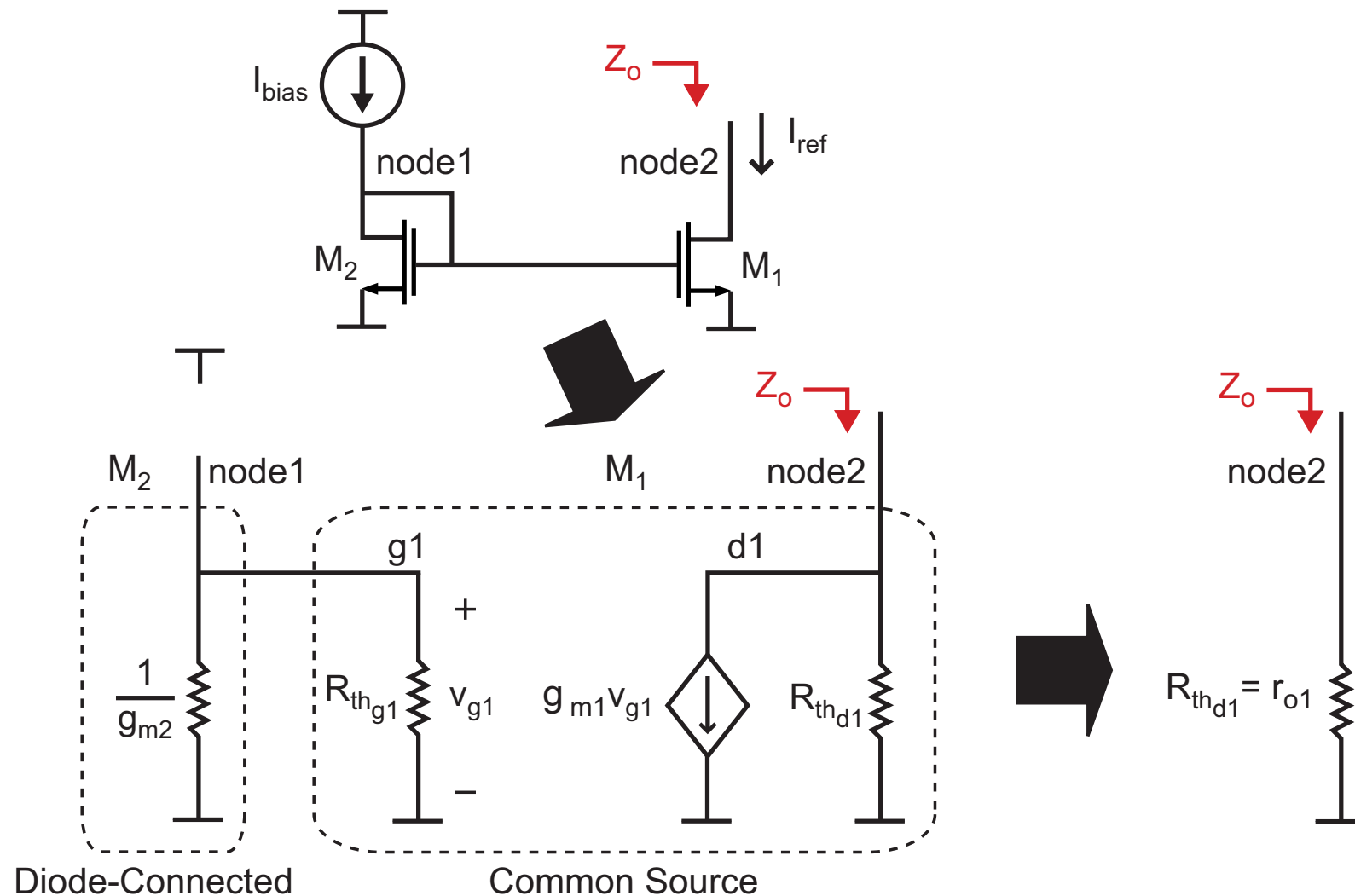
Resulting One-Port Model



- Plug in Hybrid- $\pi$  to do the analysis
  - Answer agrees with proposed Thevenin model approach
- Easiest to just memorize this result:

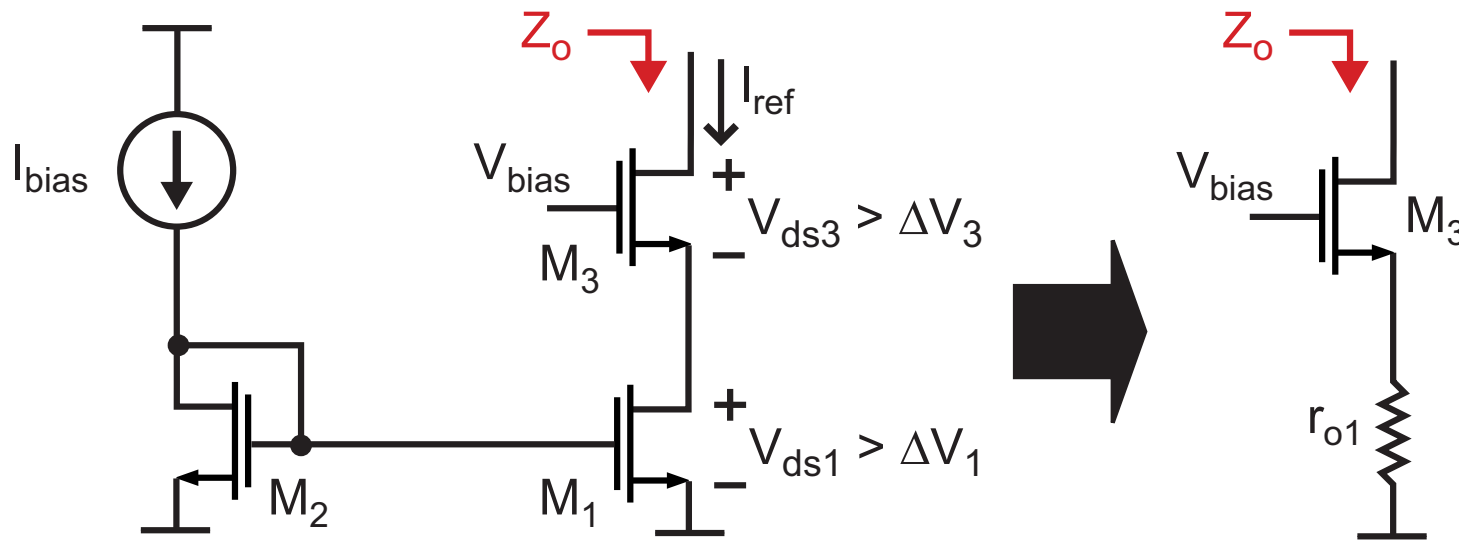
Diode connected MOS looks like a resistor of value  $1/g_m$

## Now Apply Thevenin Approach to the Current Mirror



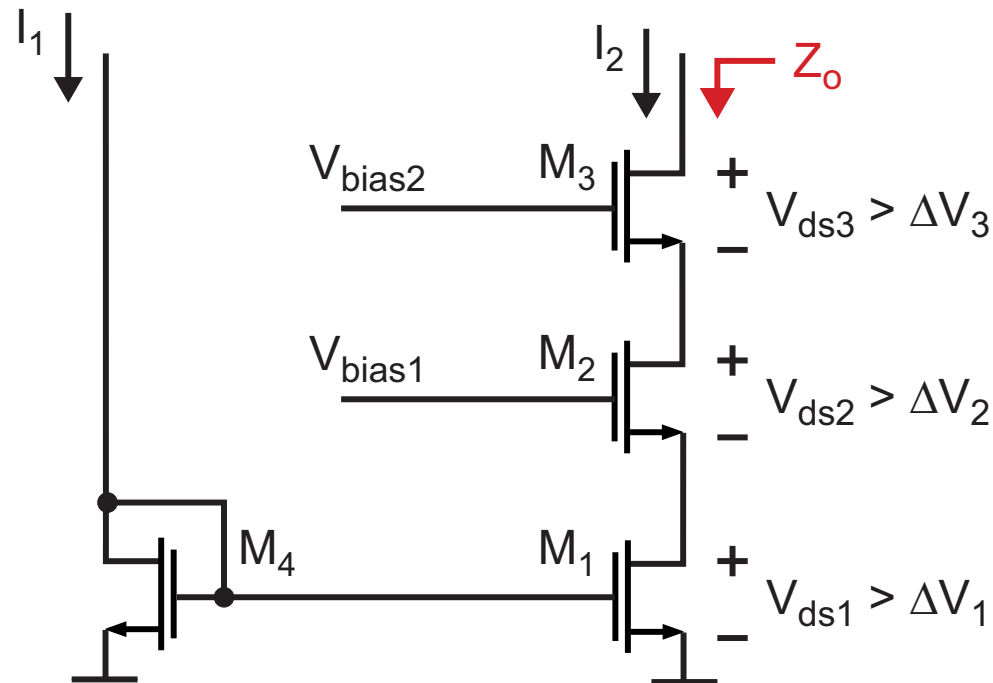
- **Key parameter of current source: output resistance**
  - Corresponds to  $r_o$  of device

# Cascode Current Source



- Offers increased output resistance
  - Calculate using Thevenin resistance method
  - How does  $I_{ref}$  compare to  $I_{bias}$ ?

# Double Cascode Current Source



- Offers *further* increased output resistance
  - Calculate using Thevenin resistance method
  - How does  $I_2$  compare to  $I_1$ ?