Analysis and Design of Analog Integrated Circuits
Lecture 4

Small Signal Modeling of CMOS Transistors

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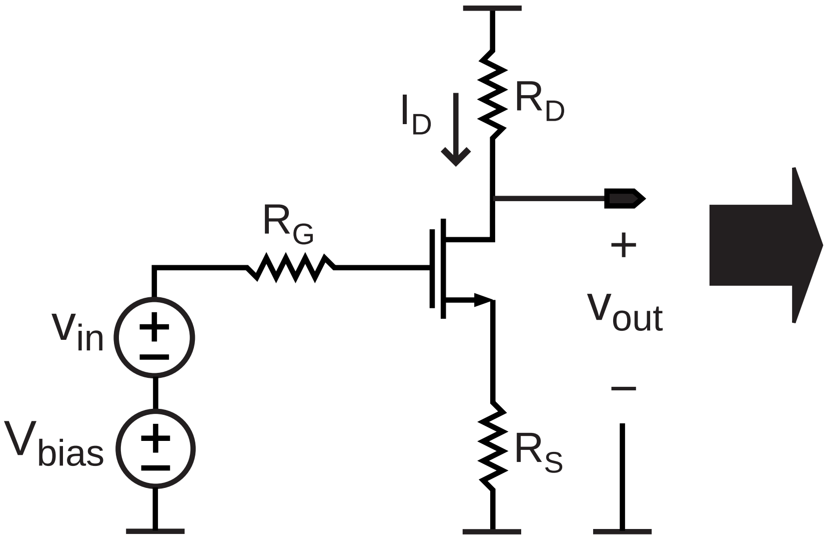
Lecture 3 Discussed Large Signal Calculations

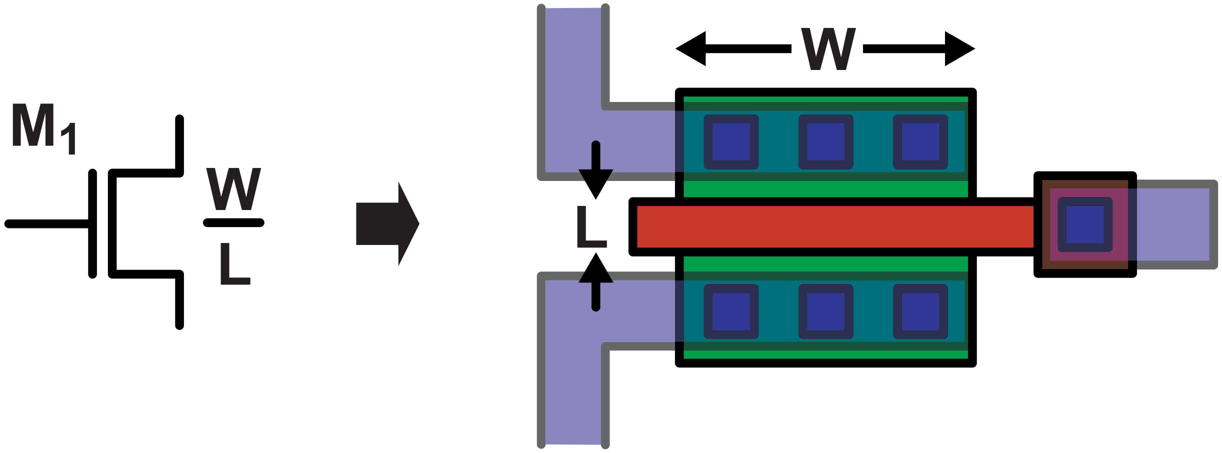
- **In analog circuits, we are often focused on amplifiers in which the small signal behavior is of high importance**
  - **Large signal calculations lead to the operating point information of the circuit which is used to determine the small signal model of the device**
- **Example amplifier circuit:**



Small Signal Analysis Steps

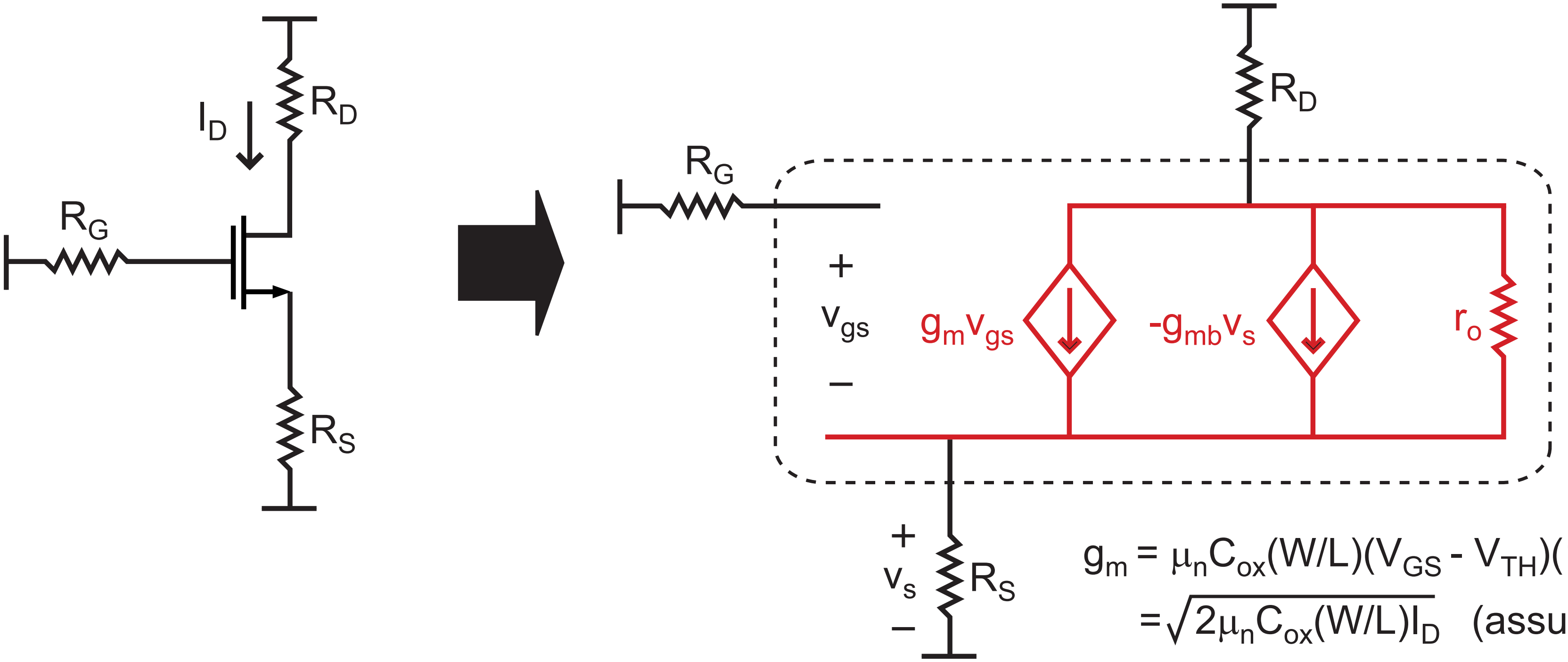
1) Solve for bias current I_d
2) Calculate small signal parameters (such as g_m, r_o)
3) Solve for small signal response using transistor hybrid-π small signal model

A Key Design Parameter is the Sizing of Devices



- **The designer is generally free to choose the width (W) and length (L) of the device**
  - **Wider width is often chosen to achieve higher channel current for a given gate bias voltage**
  - **Longer length is often avoided since it lowers the channel current and decreases the operating speed of the device**
    - The minimum length for the gate is often used to define the process name (i.e., 0.18u CMOS or 0.13u CMOS)
    - Longer length is used in cases where better matching or high resistance is desired

MOS DC Small Signal Model (Saturation Assumed)



$$g_m = \mu_n C_{ox}(W/L)(V_{GS} - V_{TH})(1 + \lambda V_{DS})$$

$$= \sqrt{2\mu_n C_{ox}(W/L) I_D} \quad \text{(assuming } \lambda V_{DS} << 1\text{)}$$

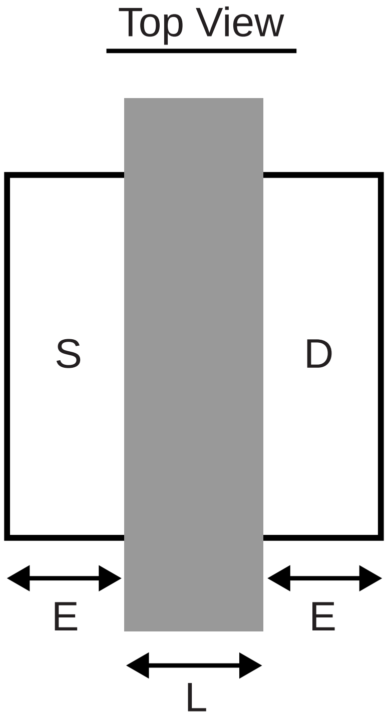
$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2|\Phi_F| + V_{SB}}} \quad \text{where } \gamma = \frac{\sqrt{2q\varepsilon_s N_A}}{C_{ox}}$$

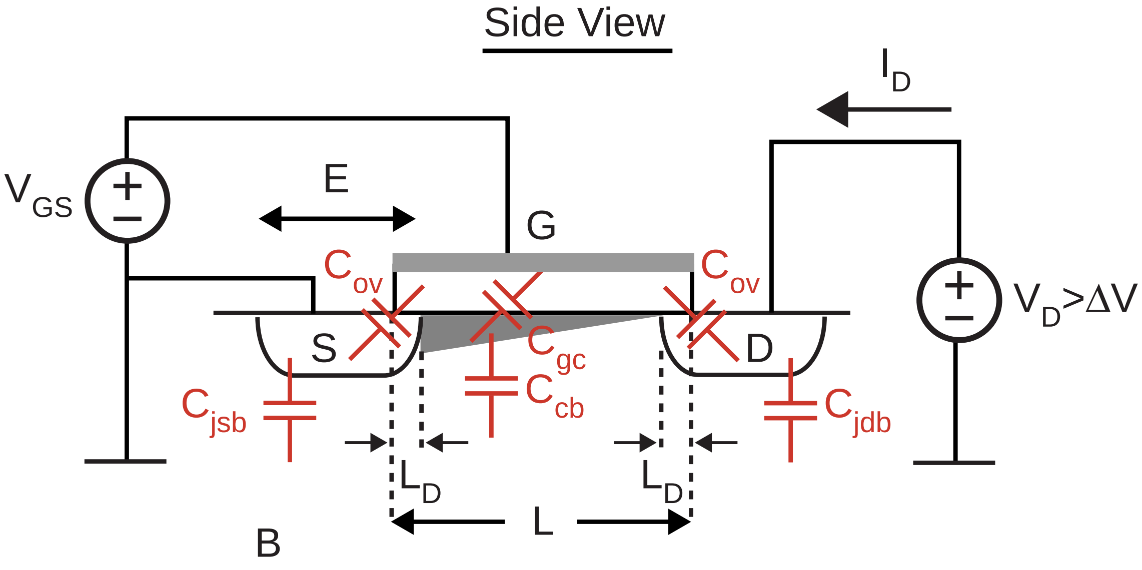
In practice: $g_{mb} = g_m/5$ to $g_m/3$

$$r_o = \frac{1}{\lambda I_D}$$

- **How do we model if device is in the triode region?**

CMOS Devices Also Have Capacitance





junction bottom wall cap (per area)

junction sidewall cap (per length)

source to bulk cap: $C_{jsb} = \frac{C_j(0)}{\sqrt{1+V_{SB}/|\Phi_B|}}WE + \frac{C_{jsw}(0)}{\sqrt{1+V_{SB}/|\Phi_B|}}(W+2E)$

(make 2W for "4 sided" perimeter in some cases)

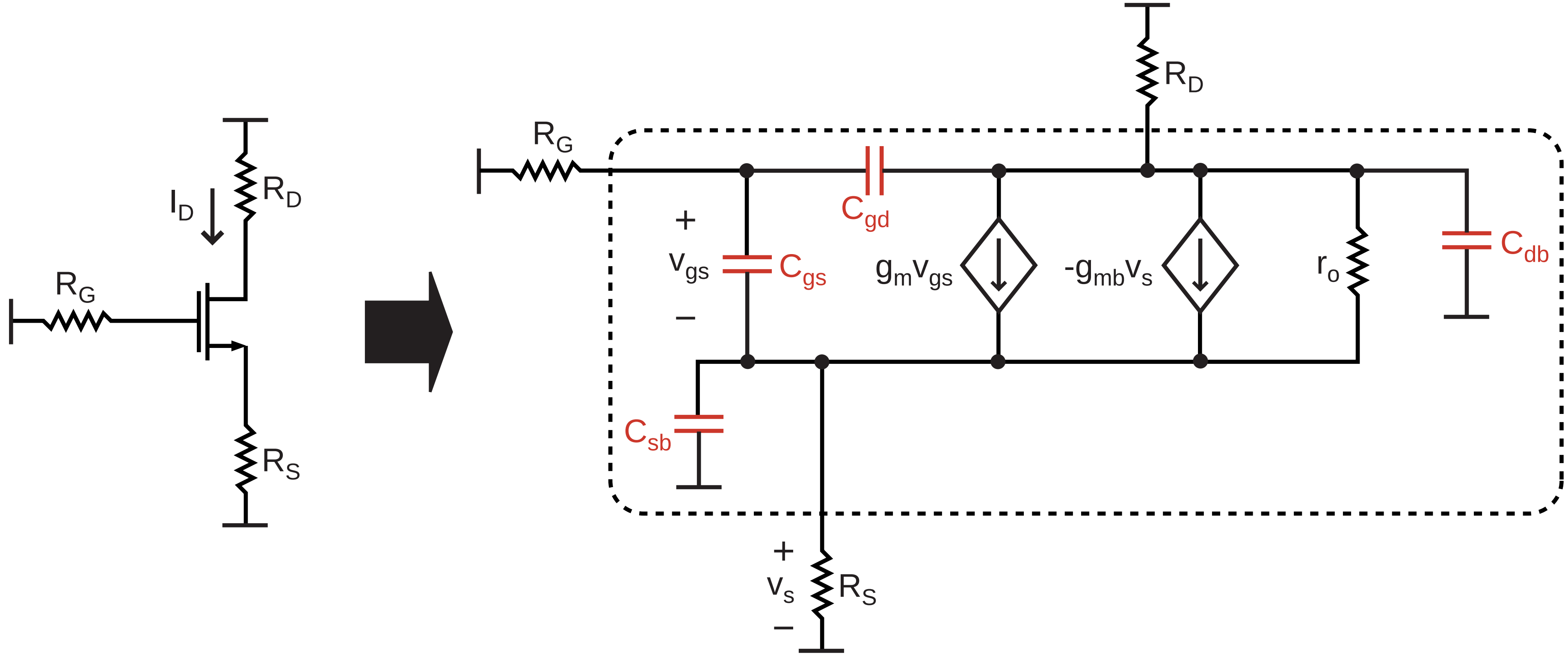
drain to bulk cap: $C_{jsd} = \frac{C_j(0)}{\sqrt{1+V_{DB}/|\Phi_B|}}WE + \frac{C_{jsw}(0)}{\sqrt{1+V_{DB}/|\Phi_B|}}(W+2E)$

overlap cap: $C_{ov} = WL_DC_{ox} + WC_{fringe}$

gate to channel cap: $C_{gc} = \frac{2}{3}C_{ox}W(L-2L_D)$

channel to bulk cap: C_{cb} - ignore in this class

MOS AC Small Signal Model (Device in Saturation)



$$C_{gs} = C_{gc} + C_{ov} = \frac{2}{3} C_{ox} W(L-2L_D) + C_{ov}$$

$$C_{gd} = C_{ov}$$

$C_{sb} = C_{jsb}$ (area + perimeter junction capacitance)

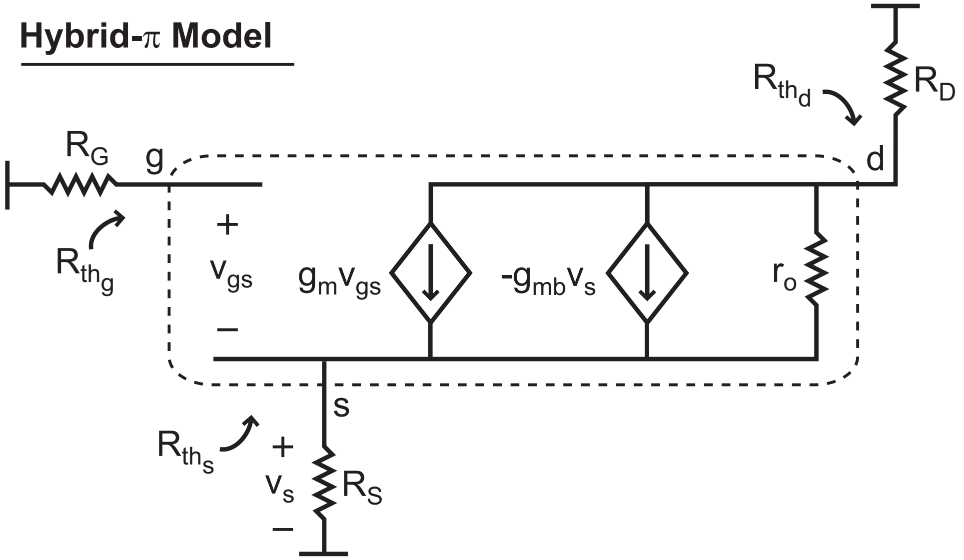
$C_{db} = C_{jdb}$ (area + perimeter junction capacitance)

Small Signal Modeling Strategy

- **We will focus on the DC Small Signal Model first**
  - **This will allow us to calculate the gain of amplifiers**
  - **This will also allow us to derive Thevenin resistances**
    - We will later combine this information with the capacitors within the AC Small Signal Model to estimate frequency response information
- **Homework 1 should have revealed to you how clumsy the DC Small Signal Model can be in calculations**
  - **We need a more streamlined approach**
    - Strategy: do not confine to general approach, but also focus on achieving a simpler model that fits a large number of circuit topologies that we will encounter

Thevenin Modeling of CMOS Transistors

Hybrid-π Model



Key Small-Signal Parameters

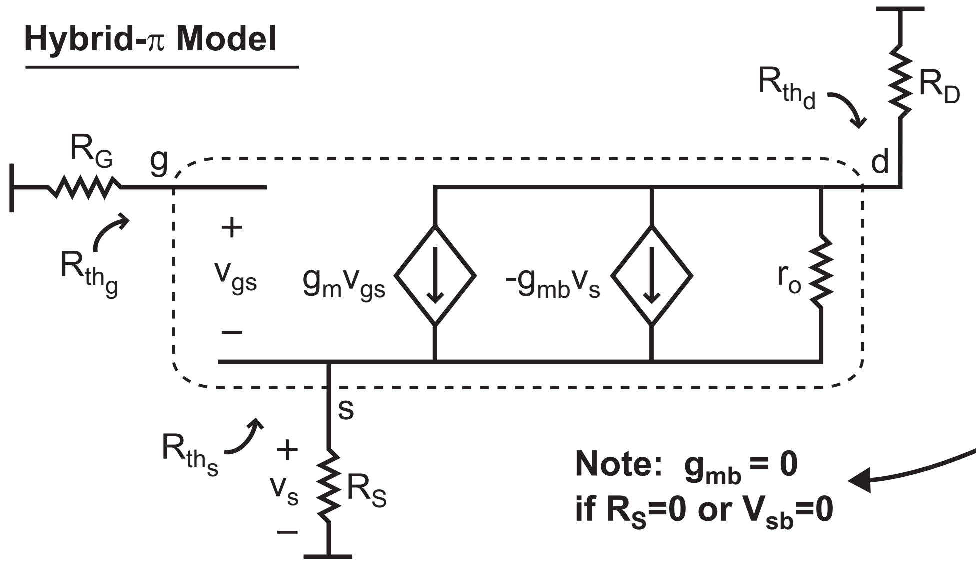
Parameter	Strong Inversion	Weak Inversion
g_m	$\sqrt{2\mu_n C_{ox}(W/L) I_D}$	$\frac{qI_D}{nkT}$
g_{mb}	$\frac{\gamma g_m}{2\sqrt{2\lvert\Phi_F\rvert + V_{SB}}}$	$\frac{(n-1)qI_D}{nkT}$
r_o	$\frac{1}{\lambda I_D}$	$\frac{1}{\lambda I_D}$

We will discuss weak inversion (i.e., subthreshold region) later

- Use the Hybrid-π model of transistor to calculate Thevenin resistances at each transistor node
- Use these Thevenin resistance calculations for many circuit topologies that we encounter

Thevenin Resistance Expressions

Hybrid-π Model



Note: $g_{mb} = 0$
if R_S=0 or V_{sb}=0

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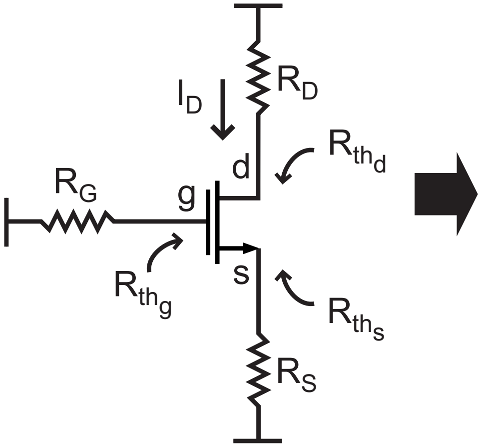
Thevenin Resistances



Exact

$R_{th_d} = r_o\,(1+(g_m+g_{mb})R_S)+R_S$

R_{th_g} = infinite

$R_{th_s} = (1+R_D/r_o)\left(r_o \,\Big\|\, \frac{1}{g_m+g_{mb}}\right)$

Approximation
($g_{mb} \ll g_m$, $g_m r_o \gg 1$)

$R_{th_d} = r_o\,(1+g_m R_S)$

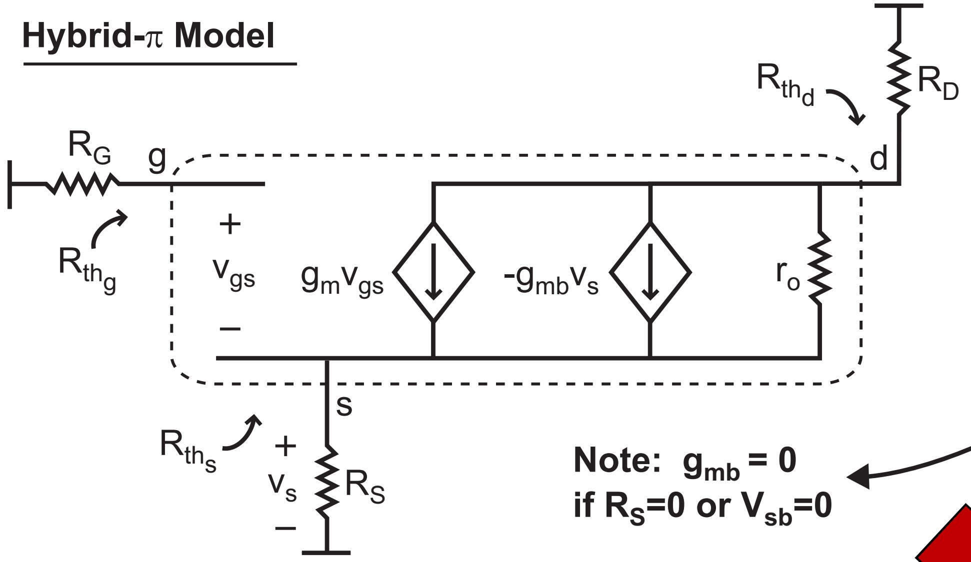
R_{th_g} = infinite

$R_{th_s} = \frac{1 + R_D/r_o}{g_m} \approx \frac{1}{g_m}$ **($R_D \ll r_o$)**

- Thevenin resistances useful for many calculations
- It would be nice to replace Hybrid-π model with a simpler alternative

Replace Hybrid-π Model with Proposed Thevenin Model

Hybrid-π Model



Note: $g_{mb} = 0$
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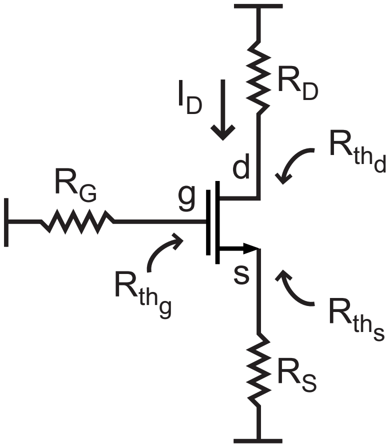
r_o	$\frac{1}{\lambda I_D}$	$\frac{1}{\lambda I_D}$

Thevenin Resistances



Exact

$R_{th_d} = r_o\,(1+(g_m+g_{mb})R_S)+R_S$

R_{th_g} = infinite

$R_{th_s} = (1+R_D/r_o)\left(r_o \,\Vert\, \frac{1}{g_m+g_{mb}}\right)$

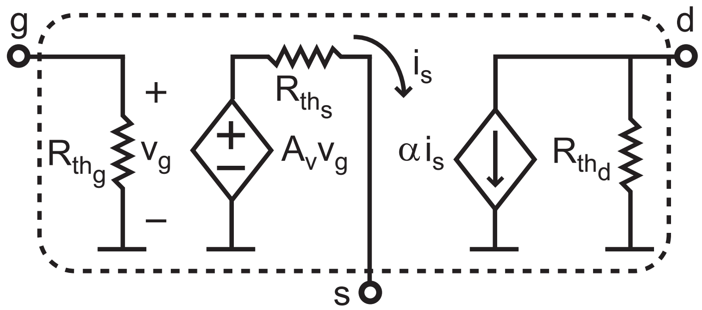
Approximation
($g_{mb} \ll g_m$, $g_m r_o \gg 1$)

$R_{th_d} = r_o\,(1+g_m R_S)$

R_{th_g} = infinite

$R_{th_s} = \frac{1 + R_D/r_o}{g_m} \approx \frac{1}{g_m}$ **($R_D \ll r_o$)**

Proposed Small Signal Transistor Model



Exact

$A_v = g_m r_o \,\Vert\, \frac{g_m}{g_m+g_{mb}}$

$\alpha = 1+R_D/R_{th_d}$

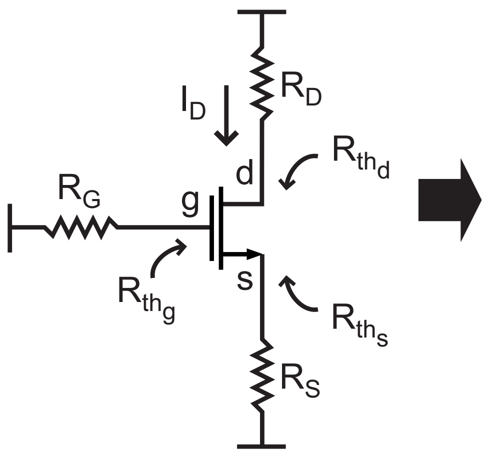
Approximation

$A_v = 1$ **($g_{mb} \ll g_m$, $g_m r_o \gg 1$)**

$\alpha = 1$ **($R_D \ll R_{th_d}$)**

Key Things to Know About the Proposed Thevenin Model

Thevenin Resistances



Exact

$R_{th_d} = r_o(1+(g_m+g_{mb})R_S)+R_S$

$R_{th_g} =$ infinite

$R_{th_s} = (1+R_D/r_o)\left(r_o \,\|\, \frac{1}{g_m+g_{mb}}\right)$

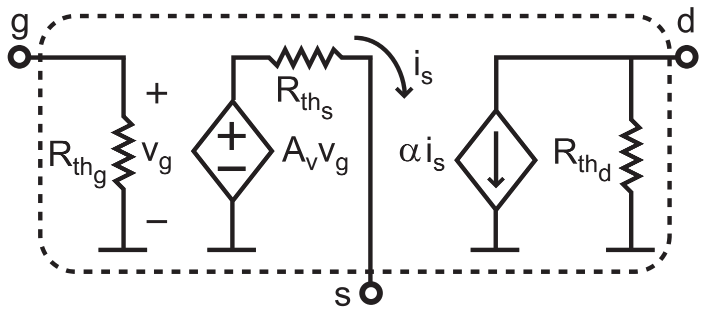
Approximation
($g_{mb} << g_m$, $g_m r_o >> 1$)

$R_{th_d} = r_o(1+g_m R_S)$

$R_{th_g} =$ infinite

$R_{th_s} = \frac{1 + R_D/r_o}{g_m} \approx \frac{1}{g_m}$ **($R_D << r_o$)**

Proposed Small Signal Transistor Model



Exact

$A_v = g_m r_o \,\|\, \frac{g_m}{g_m+g_{mb}}$

$\alpha = 1+R_D/R_{th_d}$

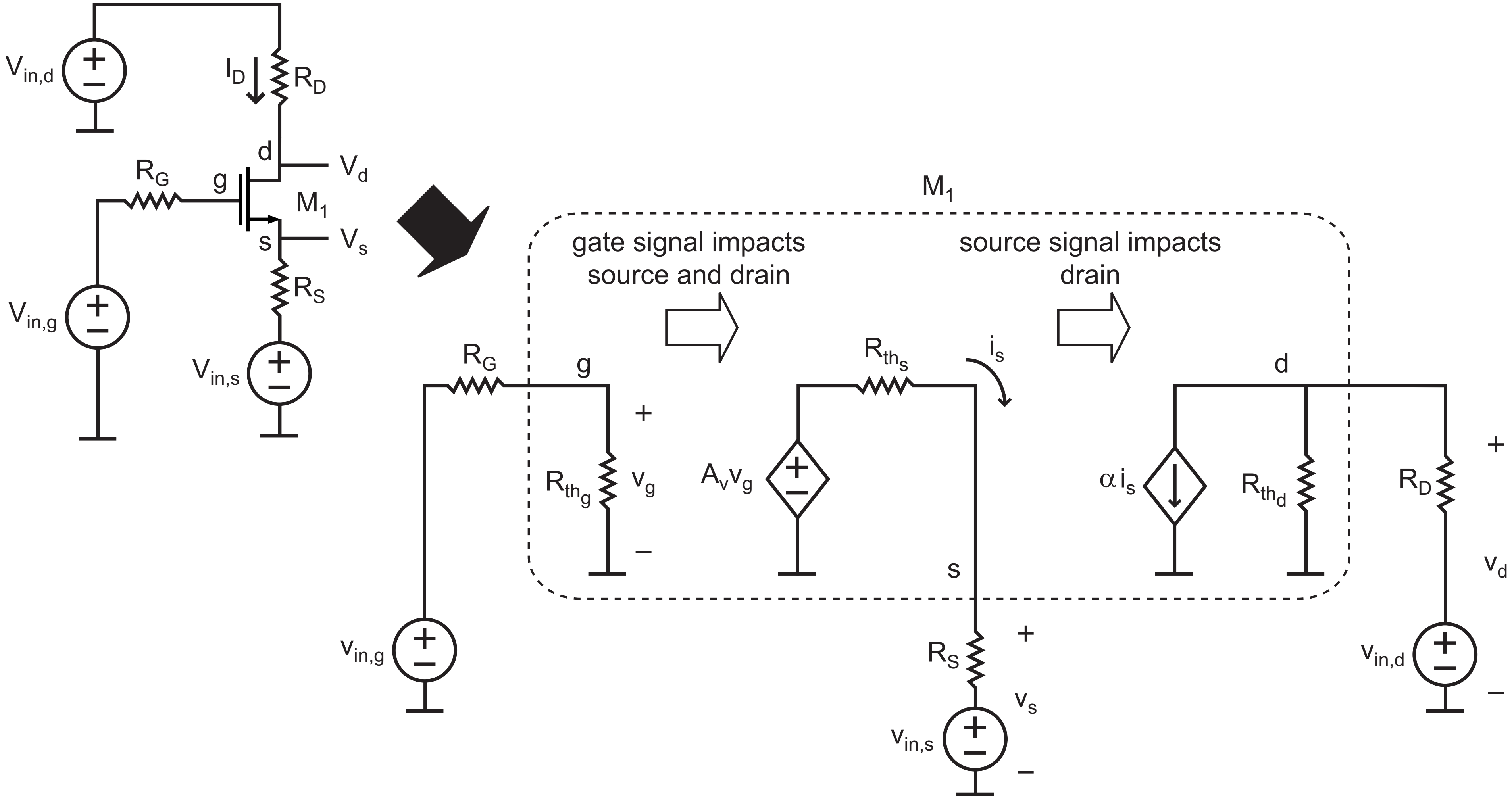
Approximation

$A_v = 1$ **($g_{mb} << g_m$, $g_m r_o >> 1$)**

$\alpha = 1$ **($R_D << R_{th_d}$)**

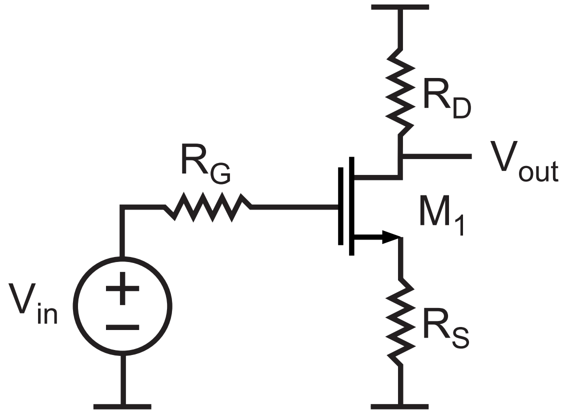
- This model may be generally applied in cases where the transistor is in saturation and where there is not strong interaction between the transistor terminals
  - Works well for open loop amplifier stages which will be our initial focus
- Proposed model is not commonly taught – I developed it

A General View of Signal Flow in an Open Loop Device



- **To first order, influence of signals go from gate to source or from gate and/or source to drain**
  - **This is only true when the device is in saturation**

Example: Small Signal Analysis of Amplifier Circuit



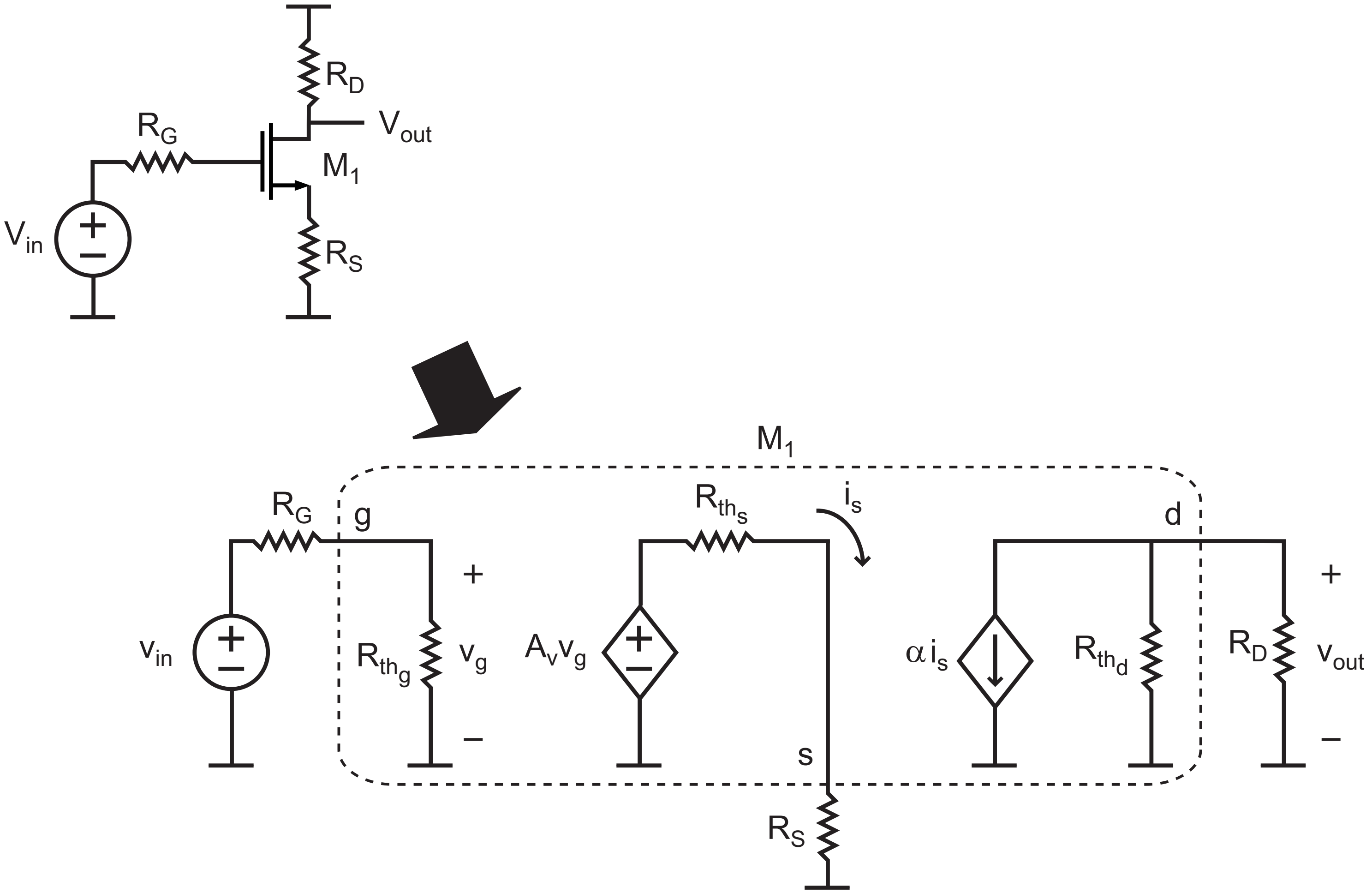
Key device characteristics that must be known:

For g_m, r_o: W, L, $\mu_n C_{ox}$, λ

For g_{mb}: g_m, γ, Φ_F, V_{SB}

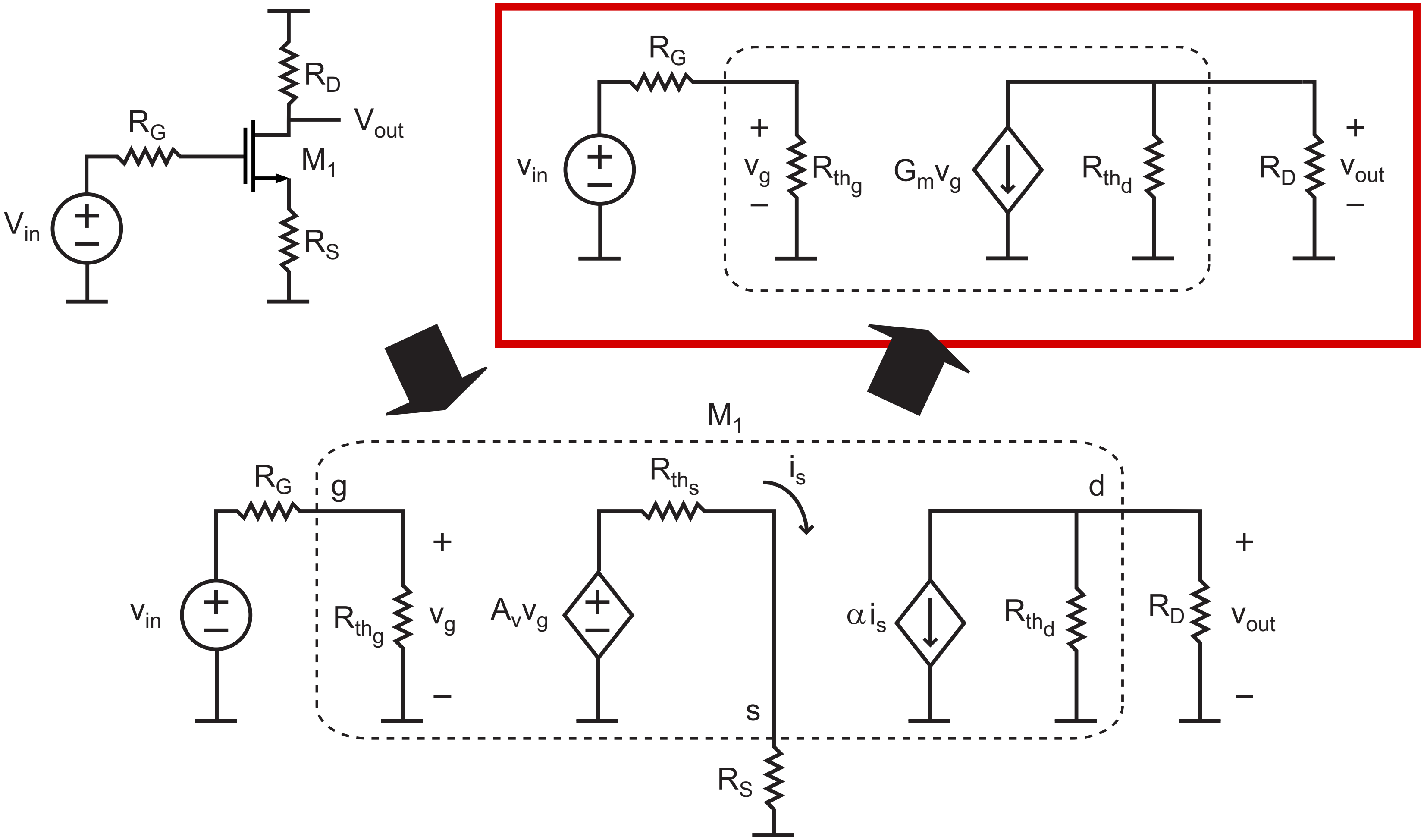
- **First step: determine the operating region of transistor**
  - **For triode region, approximate channel as a resistance**
    - I_d will usually be set primarily by drain and source network
  - **For subthreshold region, approximate channel as open**
    - Later on, we will take a more accurate view of this
  - **For saturation region, use proposed Thevenin model**
    - I_d will usually be set by gate voltage and source network (i.e., resistance and voltage)
    - Small signal parameters (g_m, r_o, etc.) can be calculated once I_d is known

Substitute Proposed Thevenin Model (Assumes Saturation)



- **Notice that all voltages and currents can be calculated without requiring simultaneous equations!**

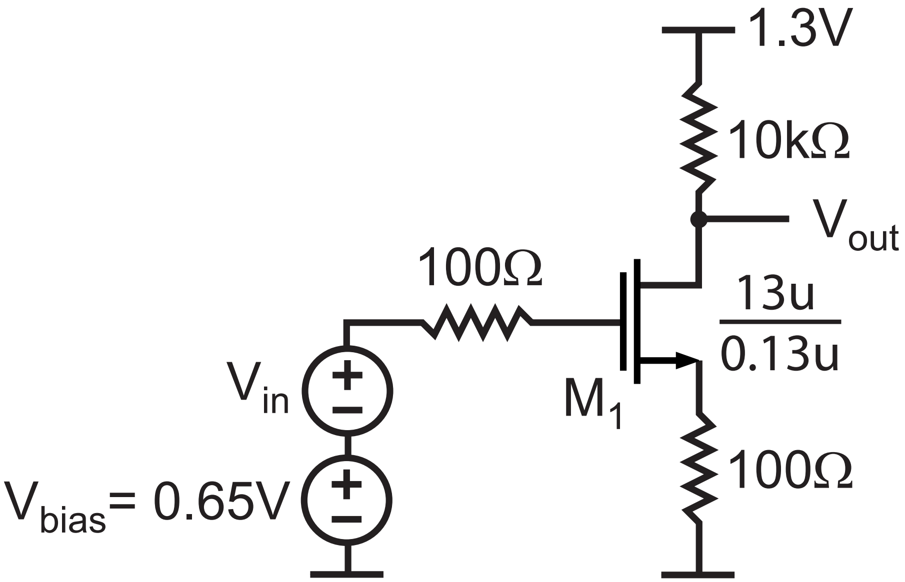
Reduce to Two-Port



- **Calculation of G_m:**

$$\alpha i_s = i_s = \frac{A_v}{R_{th_s} + R_s} v_g \approx \frac{1}{1/g_m + R_s} v_g = \frac{g_m}{1 + g_m R_s} v_g = G_m v_g$$

Detailed Example



Assumptions:

$\mu_n C_{ox}$ = 50μA/V², V_{THn} = 0.5V

λ = 1/(10V), γ = 0

- **Determine operating point conditions**
  - **Transistor operating region, I_d**
- **Determine small signal parameters of transistor model**
  - **If transistor is in saturation, this is g_m, r_o, etc.**
- **Determine gain of amplifier**