

Analysis and Design of Analog Integrated Circuits
Lecture 3

Large Signal Modeling of CMOS Transistors

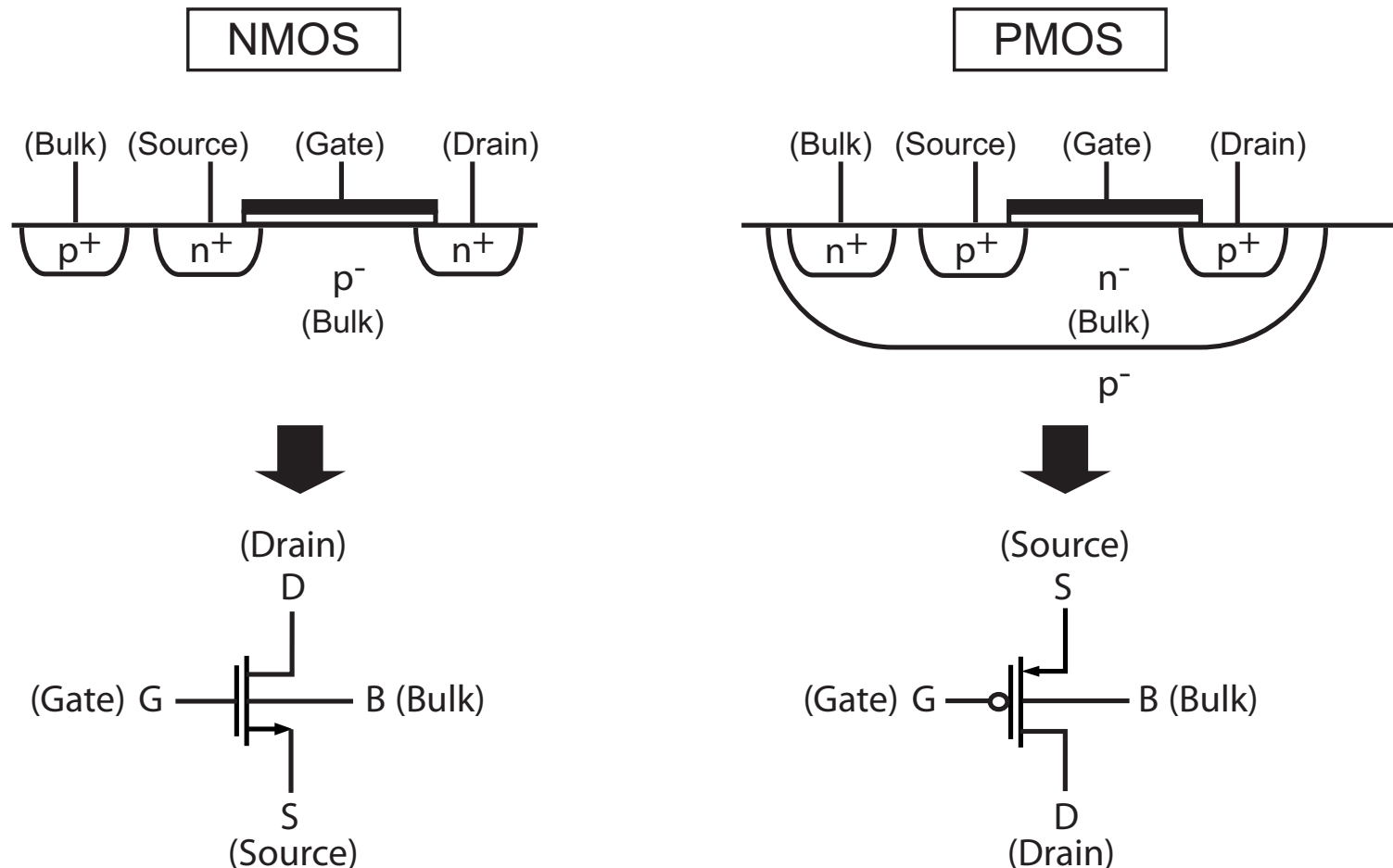
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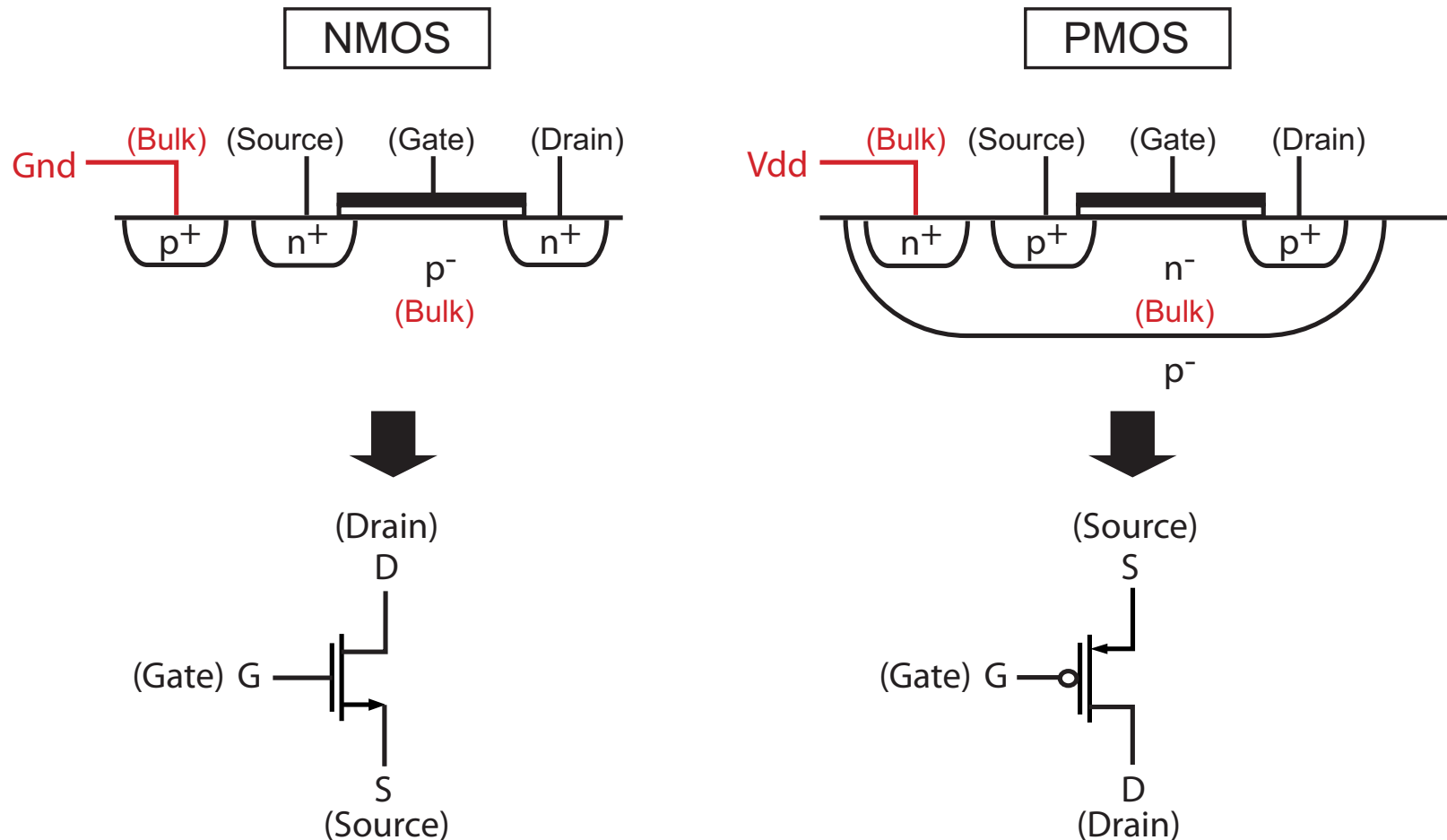
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Introducing CMOS Devices



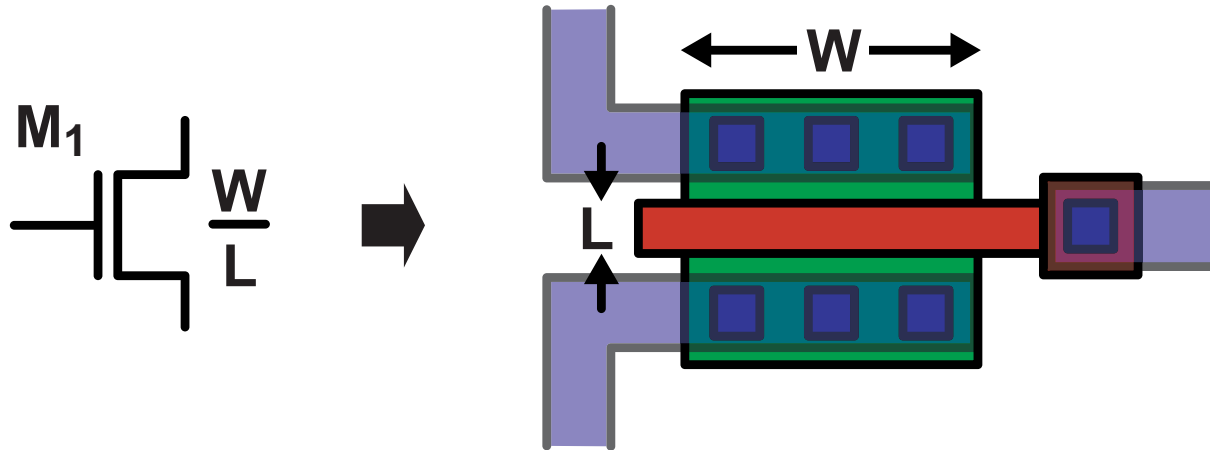
- **CMOS: Complementary Metal Oxide Semiconductor**
 - Current flow through channel between Drain and Source is controlled by Gate
 - Complementary: both PMOS and NMOS are available

Simplified MOS Symbol for Typical Bulk Connections



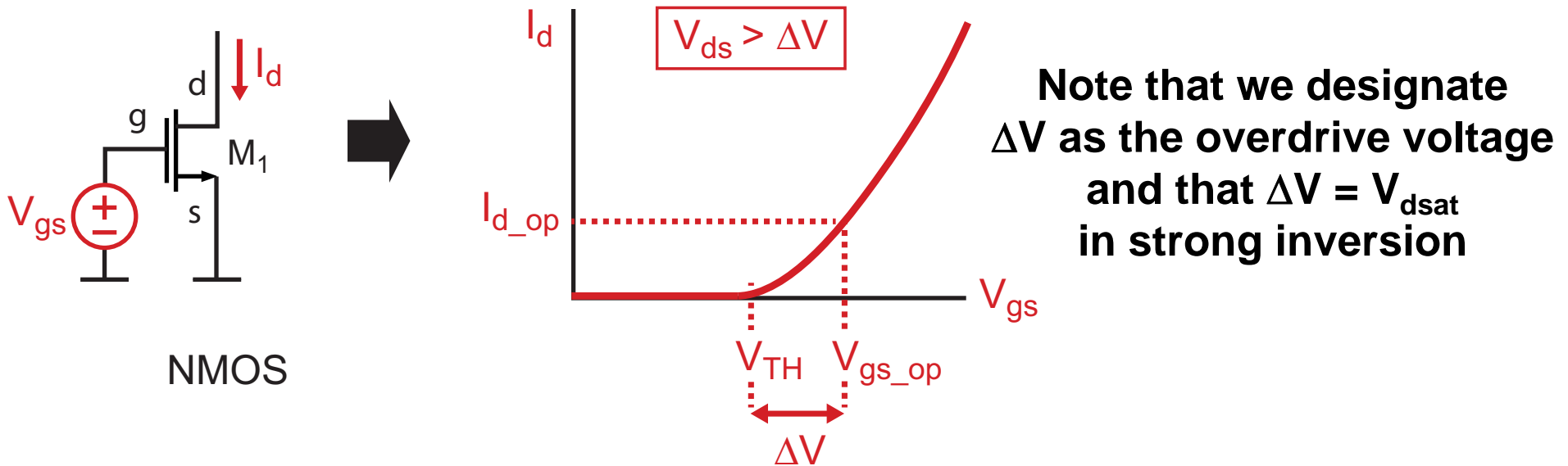
- **Bulk silicon below the channel under the gate also has an impact on the channel current**
 - We often tie the Bulk to Gnd/Vdd for NMOS/PMOS devices
 - In such case, the symbol does not include the bulk terminal

Symbol Notation Often Includes Size



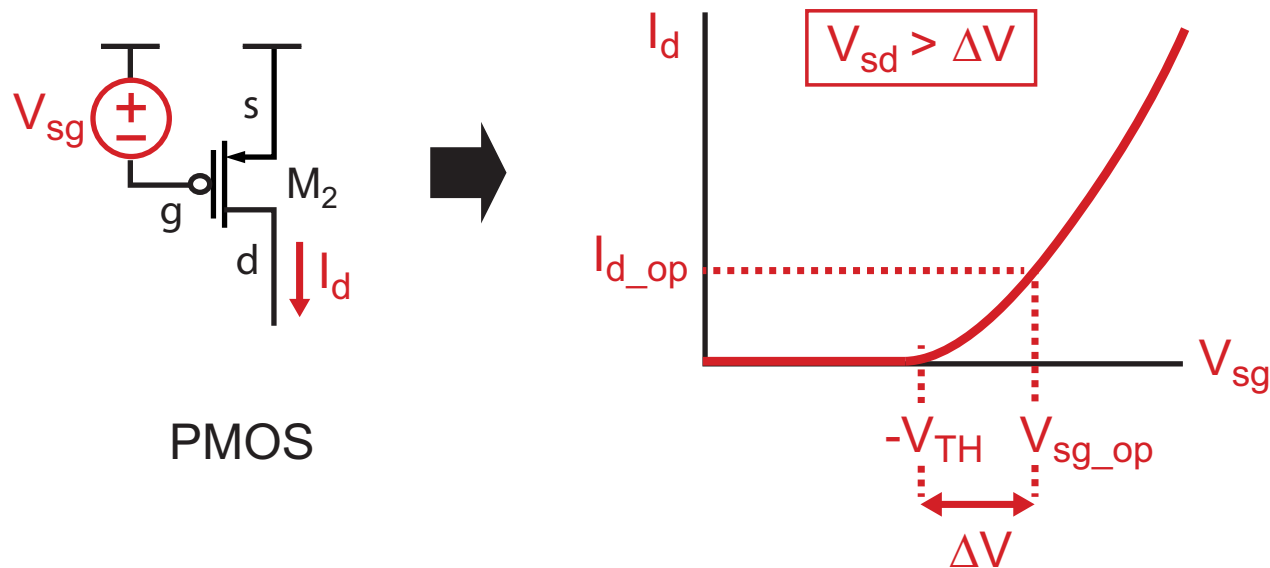
- The designer is generally free to choose the width (W) and length (L) of the device
 - Wider width is often chosen to achieve higher channel current for a given gate bias voltage
 - Longer length is often avoided since it lowers the channel current and decreases the operating speed of the device
 - The minimum length for the gate is often used to define the process name (i.e., 0.18u CMOS or 0.13u CMOS)
 - Longer length is used in cases where better matching or high resistance is desired

Channel Current as a Function of Gate Voltage



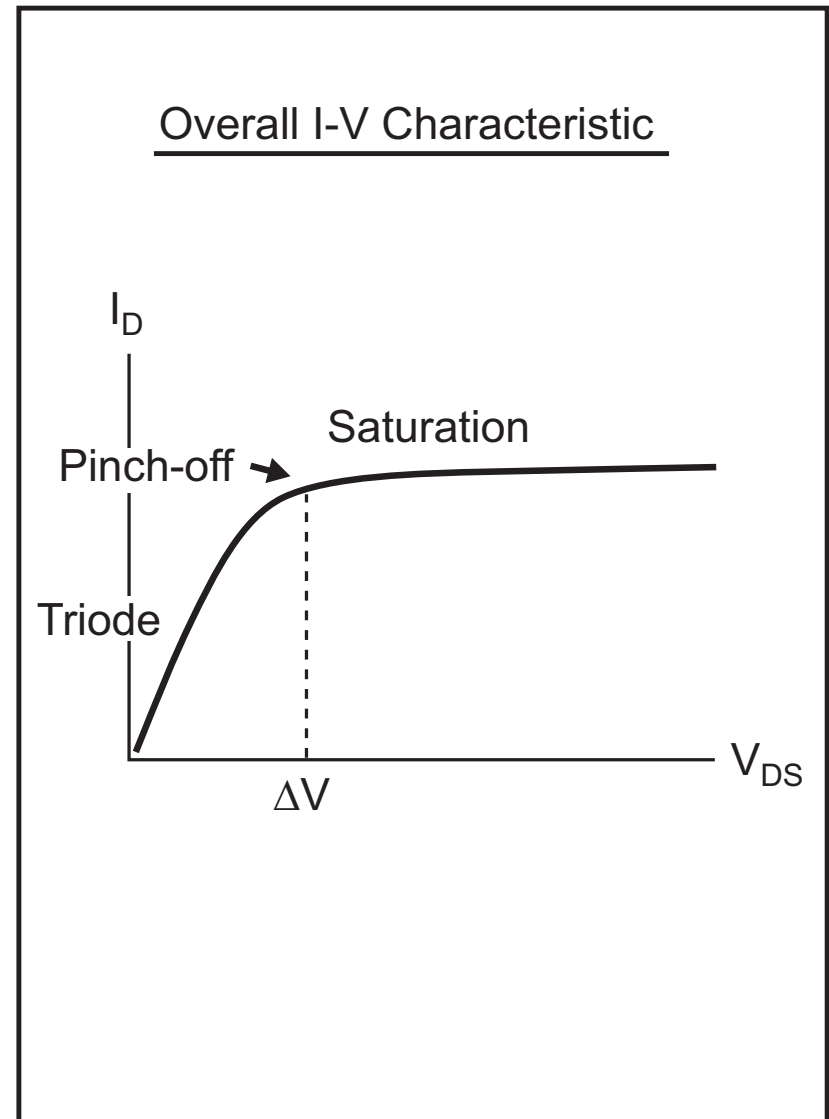
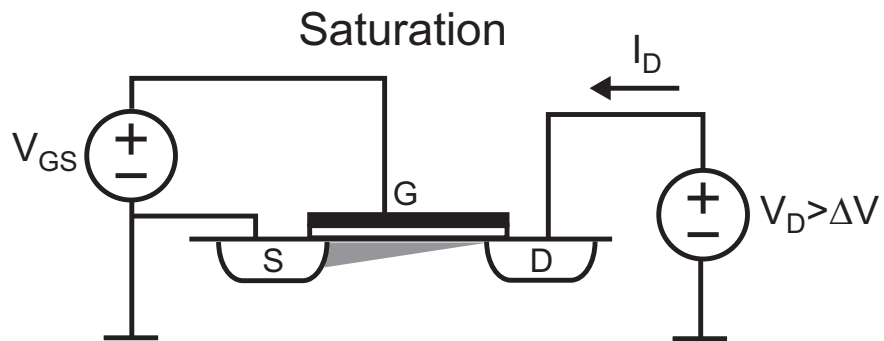
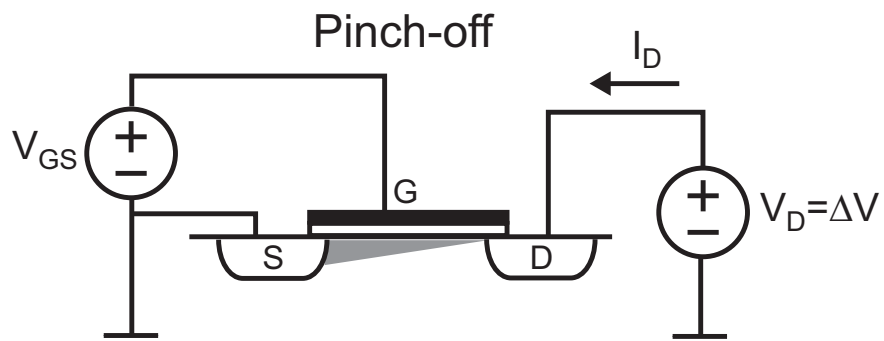
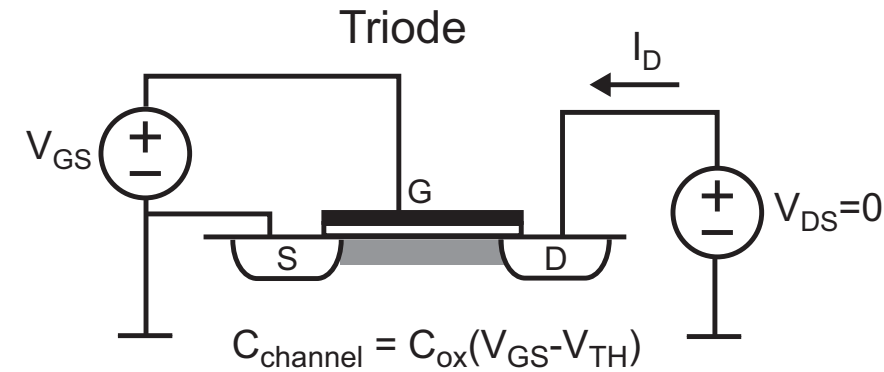
- If $V_{gs} < V_{TH}$, then current density I_d/W is small
 - The device is in the subthreshold operating region
- For $V_{gs} > V_{TH}$, then I_d/W is much larger
 - The device is in strong inversion
 - If $V_{ds} > \Delta V$, then I_d is relatively independent of V_{ds}
 - The device is in the saturation operating region
 - If $V_{ds} < \Delta V$, then I_d is strongly dependent on V_{ds}
 - The device is in the triode operating region

PMOS Devices are Complementary to NMOS Devices



- **Same observations and definitions apply to PMOS**
 - However, voltage and current signs are flipped
 - Note that $V_{sg} = -V_{gs}$, $V_{sd} = -V_{ds}$
 - Note that I_d as defined above for PMOS is in the opposite direction as for NMOS
 - Note that V_{TH} becomes negative

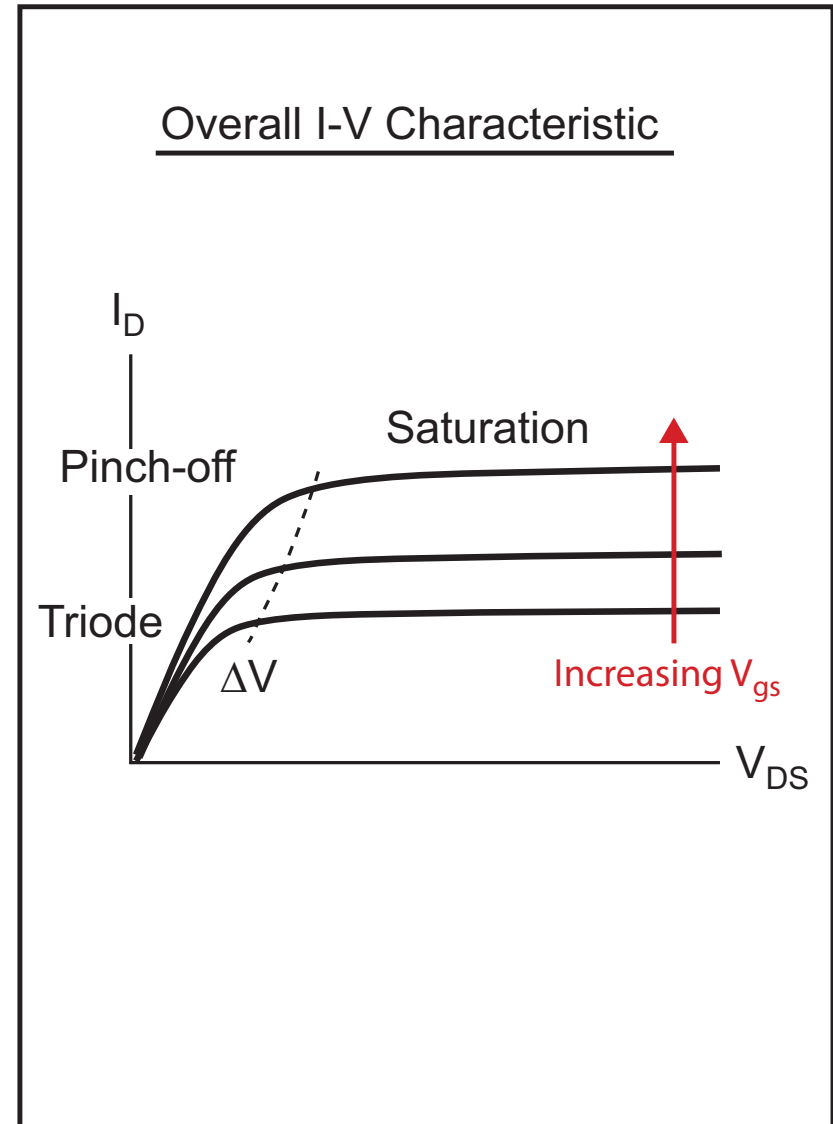
Examine MOS Behavior As V_{ds} is Increased



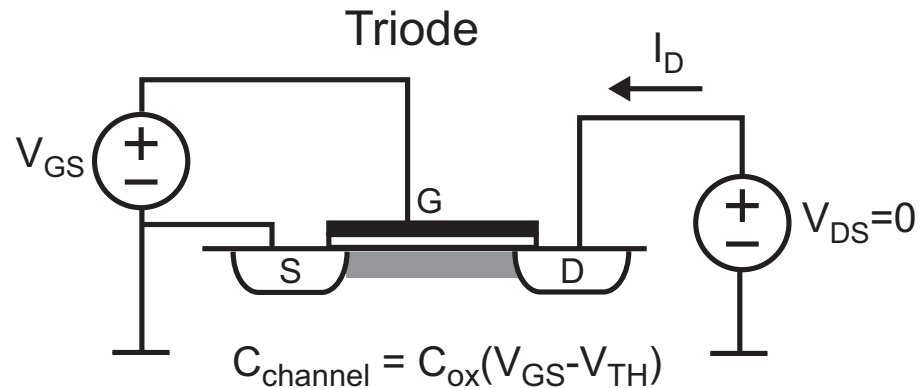
How does V_{GS} influence I_D in the above curve ?

MOS Behavior Is A Function of V_{gs} and V_{ds}

See page 15-23 of Razavi...



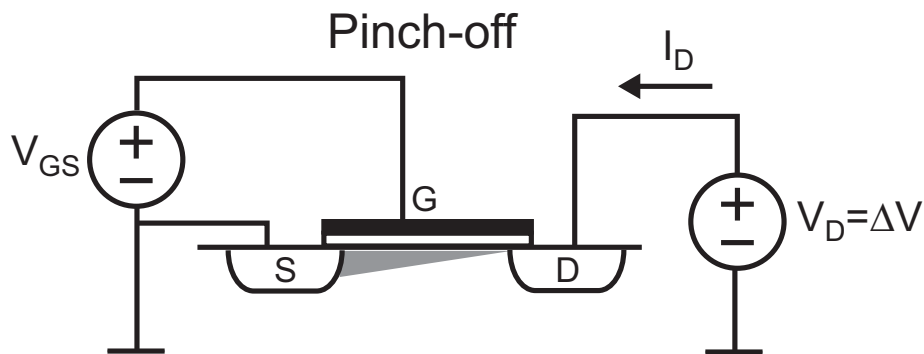
MOS Current Equations in Triode and Saturation Regions



$$I_{\text{D}} = \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}} - V_{\text{DS}}/2) V_{\text{DS}}$$

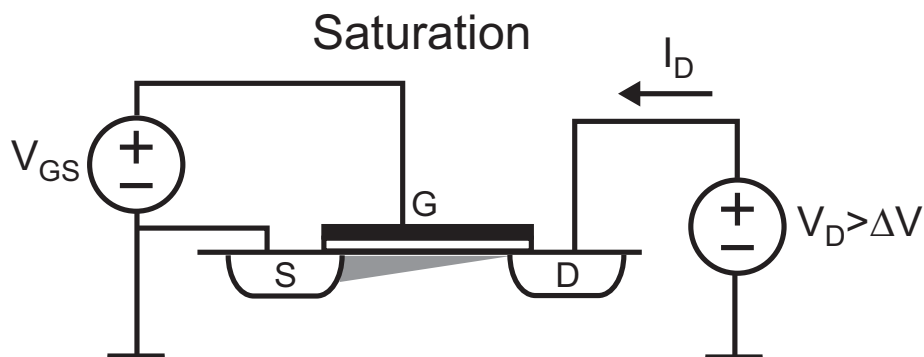
for $V_{\text{DS}} \ll V_{\text{GS}} - V_{\text{TH}}$

$$I_{\text{D}} \approx \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}}) V_{\text{DS}}$$



$$\Delta V = V_{\text{GS}} - V_{\text{TH}}$$

$$\Delta V = \sqrt{\frac{2I_{\text{D}}L}{\mu_{\text{n}}C_{\text{ox}}W}}$$



$$I_{\text{D}} = \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}})^2 (1 + \lambda V_{\text{DS}})$$

(where λ corresponds to channel length modulation)

The Issue of Velocity Saturation

- When in saturation, the MOS current is calculated as

$$I_D \approx \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_{TH})^2$$

- Which is really

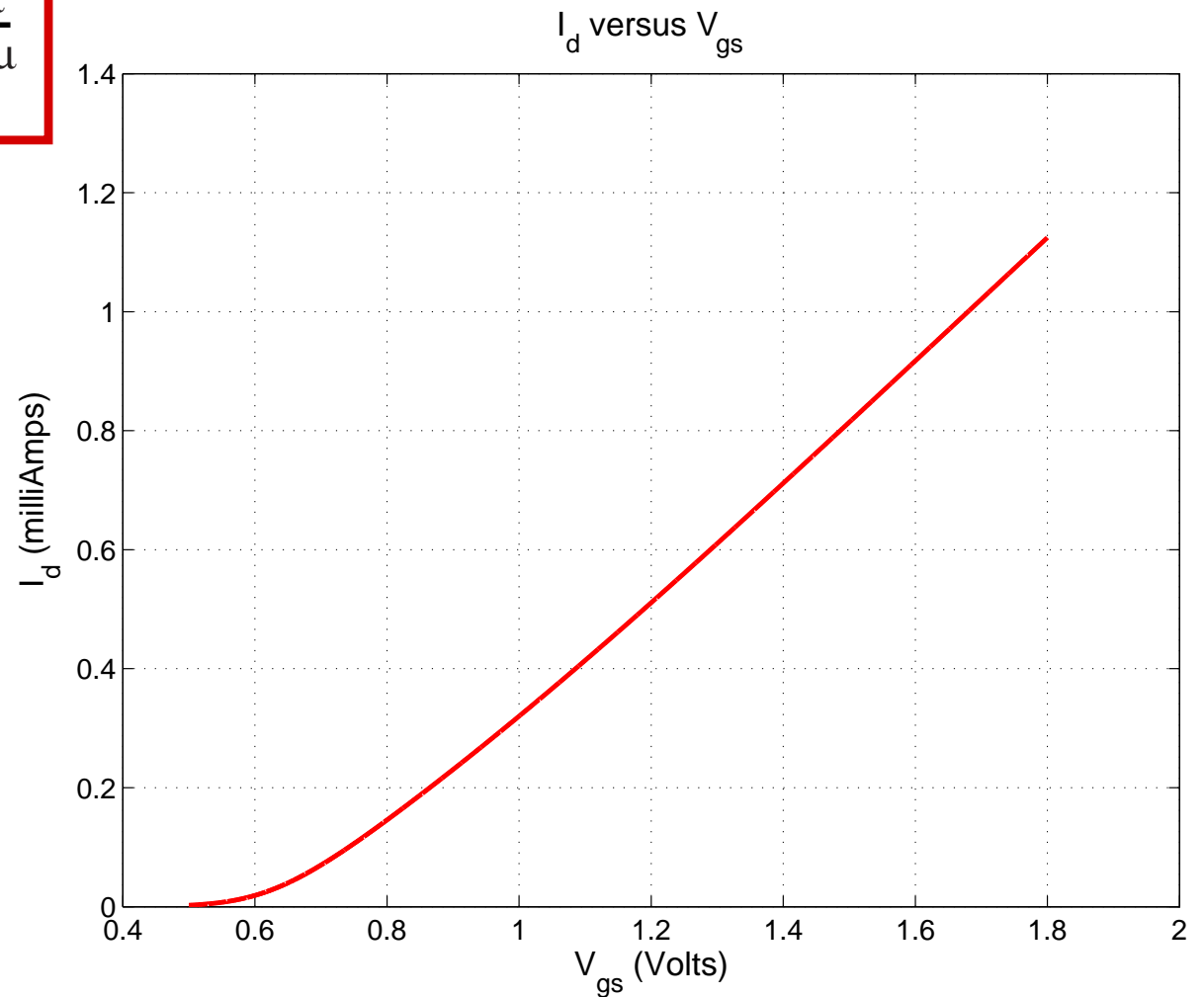
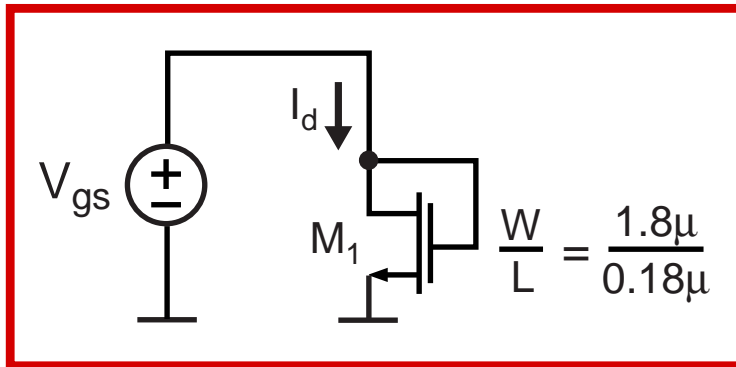
$$I_D \approx \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_{TH}) V_{dsat,l}$$

- Here $V_{dsat,l}$ is the saturation voltage at a given length
- It may be shown that

$$V_{dsat,l} \approx \frac{(V_{gs} - V_{TH})(LE_{sat})}{(V_{gs} - V_{TH}) + (LE_{sat})} = (V_{gs} - V_{TH}) || (LE_{sat})$$

- If $V_{gs} - V_{TH}$ approaches LE_{sat} in value, then
 - We say that the device is in velocity saturation
 - The current becomes *linearly* related to $V_{gs} - V_{TH}$

Example: Current Versus Voltage for 0.18 μ Device

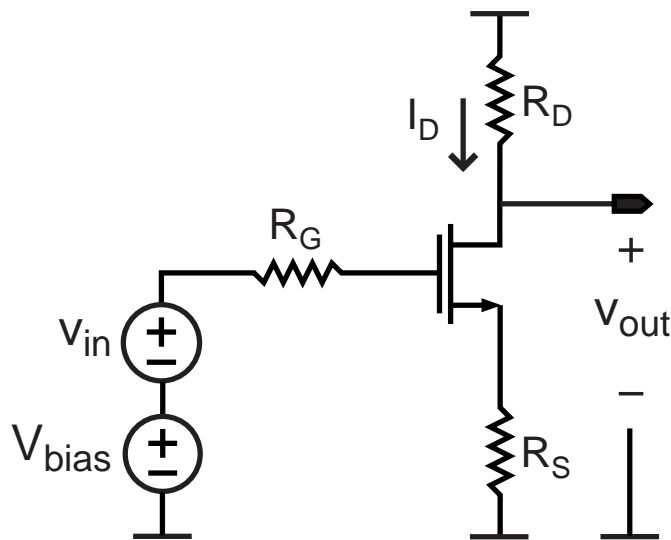


The Tricky Issue of Modeling MOS Devices

- **The device characteristics of modern CMOS devices lead to complicated analytical models**
 - This creates challenges for achieving accurate hand calculations with reasonable effort
- **Hand calculations are essential in achieving deeper understanding and intuition of circuit and device behavior**
 - Simple hand calculations lack accuracy
 - Detailed hand calculations often do not yield the desired insight and understanding to make them worthwhile
- **A typical compromise**
 - Assume simple models for hand calculations
 - Use SPICE to get a more accurate picture of the actual circuit and device characteristics and performance

What is the Key Role of Large Signal Calculations?

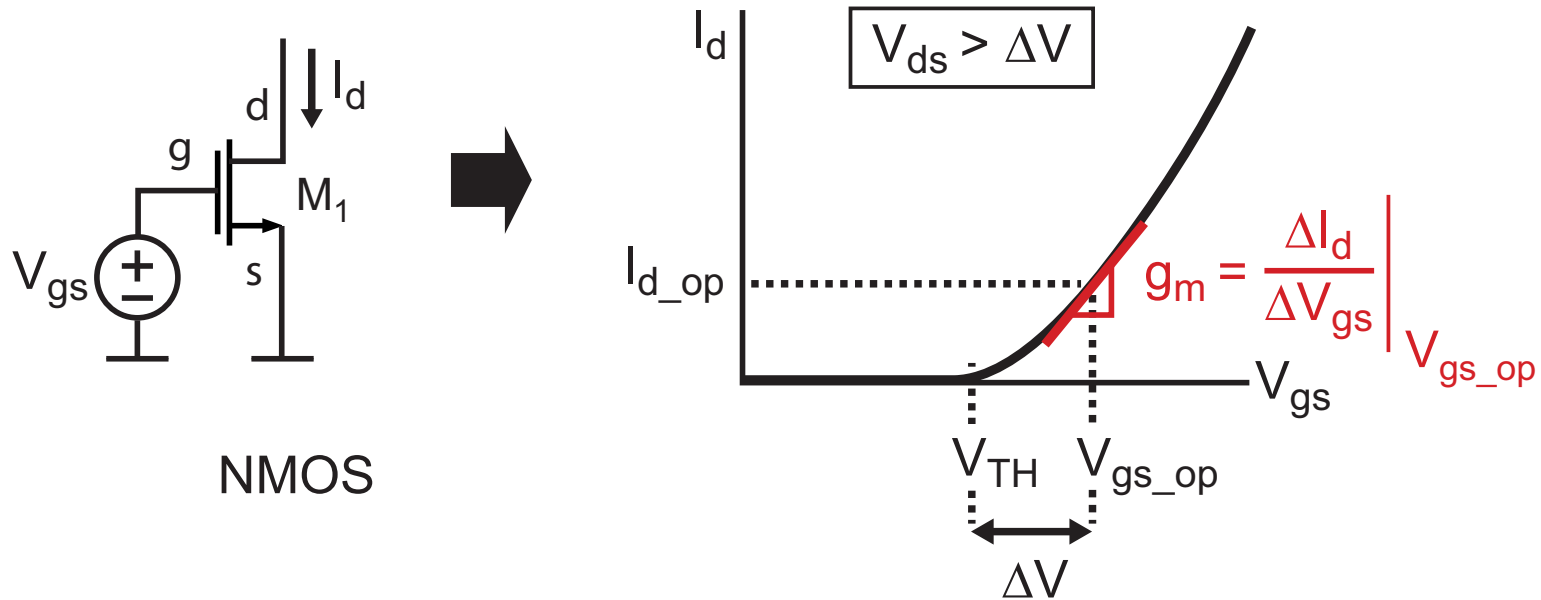
- In analog circuits, we are often focused on amplifiers in which the small signal behavior is of high importance
 - Large signal calculations lead to the operating point information of the circuit which is used to determine the small signal model of the device
- Example amplifier circuit:



Small Signal Analysis Steps

- 1) Solve for bias current I_D
- 2) Calculate small signal parameters (such as g_m , r_o)
- 3) Solve for small signal response using transistor hybrid- π small signal model

A Key Small Signal Parameter: Transconductance

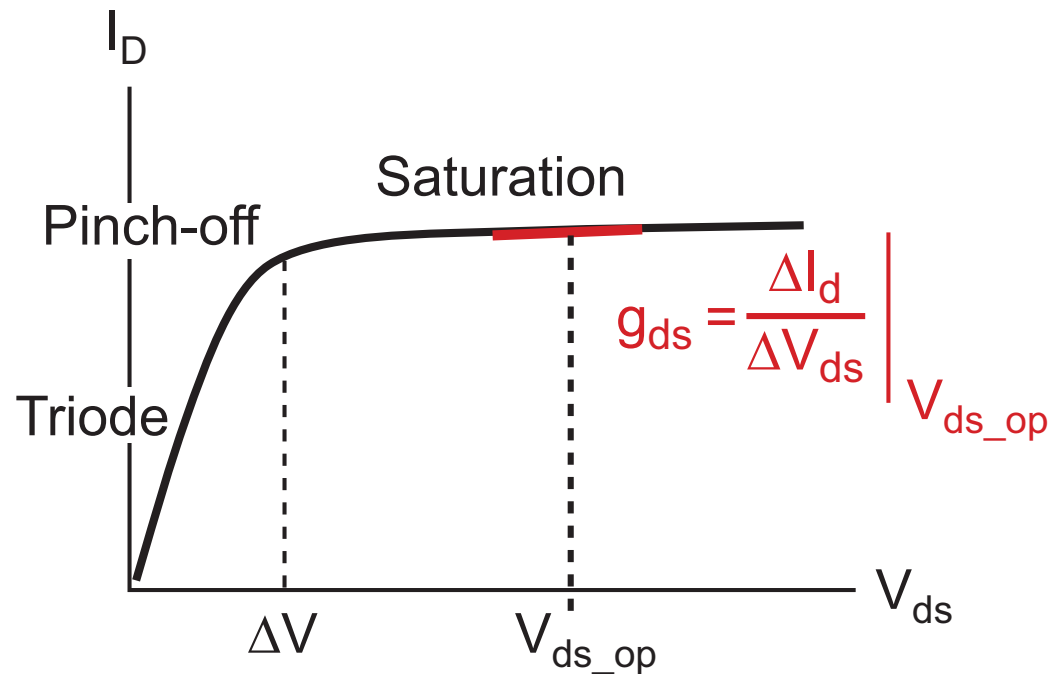


- Transconductance from input gate voltage, V_{gs} , to channel current, I_d , is very important for amplifier circuits
 - Assuming device is in saturation:

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_{TH})^2 (1 + \lambda V_{ds})$$

$$\Rightarrow g_m = \frac{\delta I_d}{\delta V_{gs}} \approx \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{TH}) \approx \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d}$$

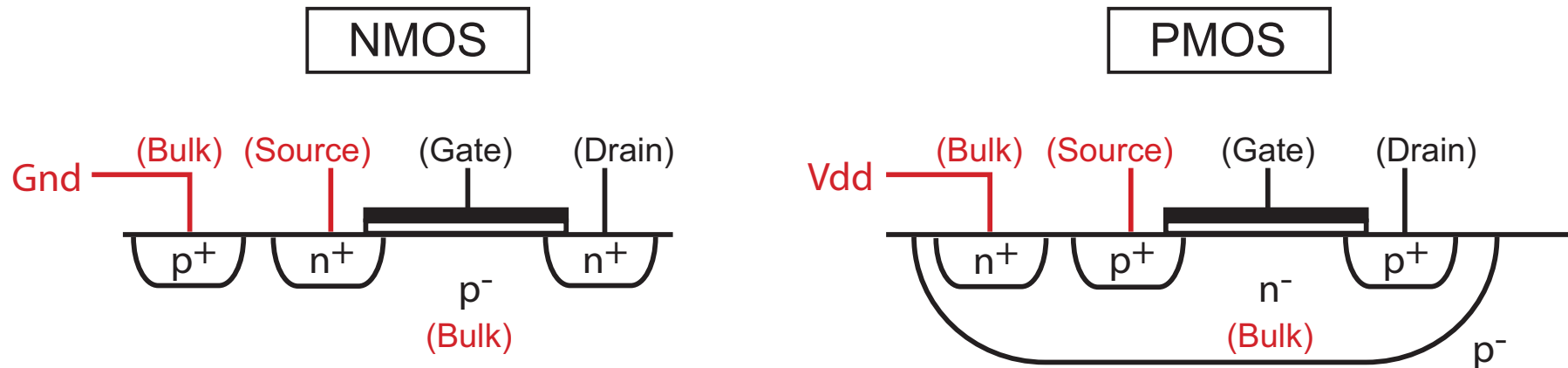
A Key Small-Signal Nonideality: Output Resistance



- Ideally, I_d would not change with V_{ds} when the device is in saturation
 - Practical CMOS transistors exhibit I_d dependence on V_{ds} due to channel length modulation
 - The parameter λ is often used to characterize this effect

$$r_o = \frac{1}{g_{ds}} = \frac{\delta V_{ds}}{\delta I_d} = \frac{1}{\lambda I_d}$$

Another Non-Ideality: Back-Gate Effect



- The threshold voltage of the device, V_{TH} , is dependent on the potential between the source and bulk

$$V_{TH} = ??$$

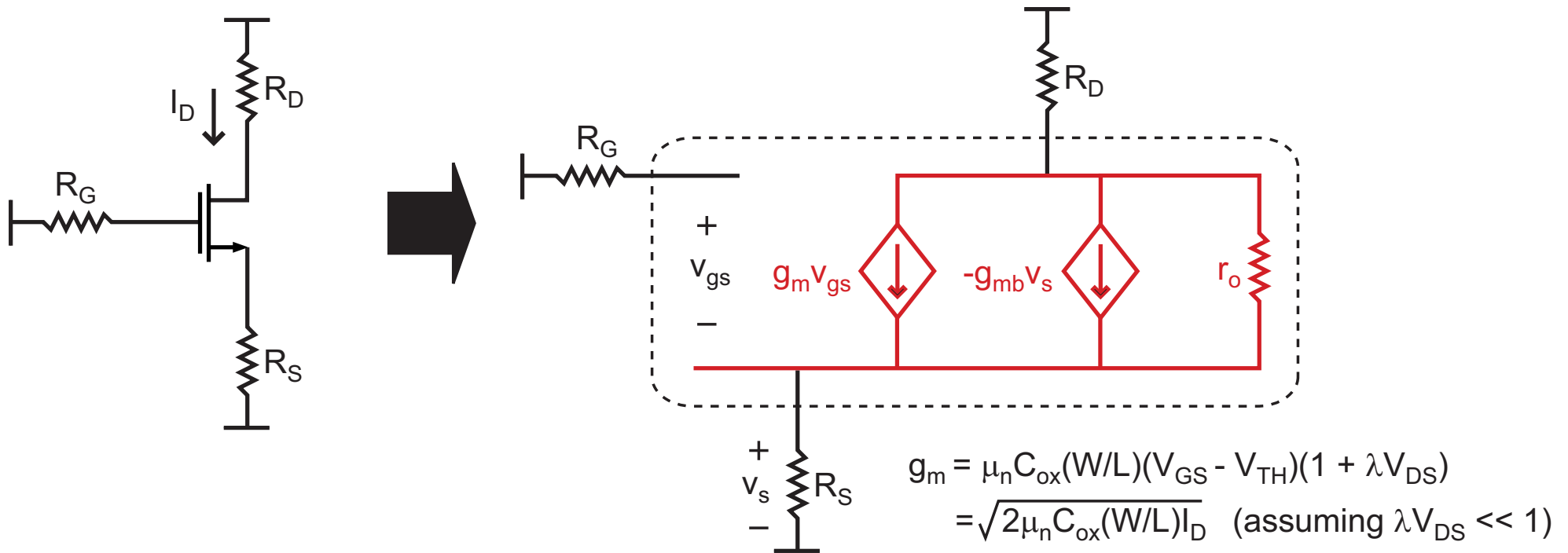
- This implies that changes in the source node voltage, V_s , lead to changes in the channel current, I_d
- We model this effect as backgate transconductance, g_{mb}

$$g_{mb} = \frac{\delta I_d}{\delta V_s}$$

- MIC503 will provide details (also see pages 34-36 of Razavi)

MOS DC Small Signal Model

- Assuming transistor is in saturation:
 - Note that designers often determine g_{mb} impact from SPICE



$$g_m = \mu_n C_{ox} (W/L) (V_{GS} - V_{TH}) (1 + \lambda V_{DS})$$

$$= \sqrt{2 \mu_n C_{ox} (W/L) I_D} \quad (\text{assuming } \lambda V_{DS} \ll 1)$$

$$g_{mb} = \frac{\gamma g_m}{2 \sqrt{2 |\Phi_F| + V_{SB}}} \quad \text{where } \gamma = \frac{\sqrt{2 q \epsilon_s N_A}}{C_{ox}}$$

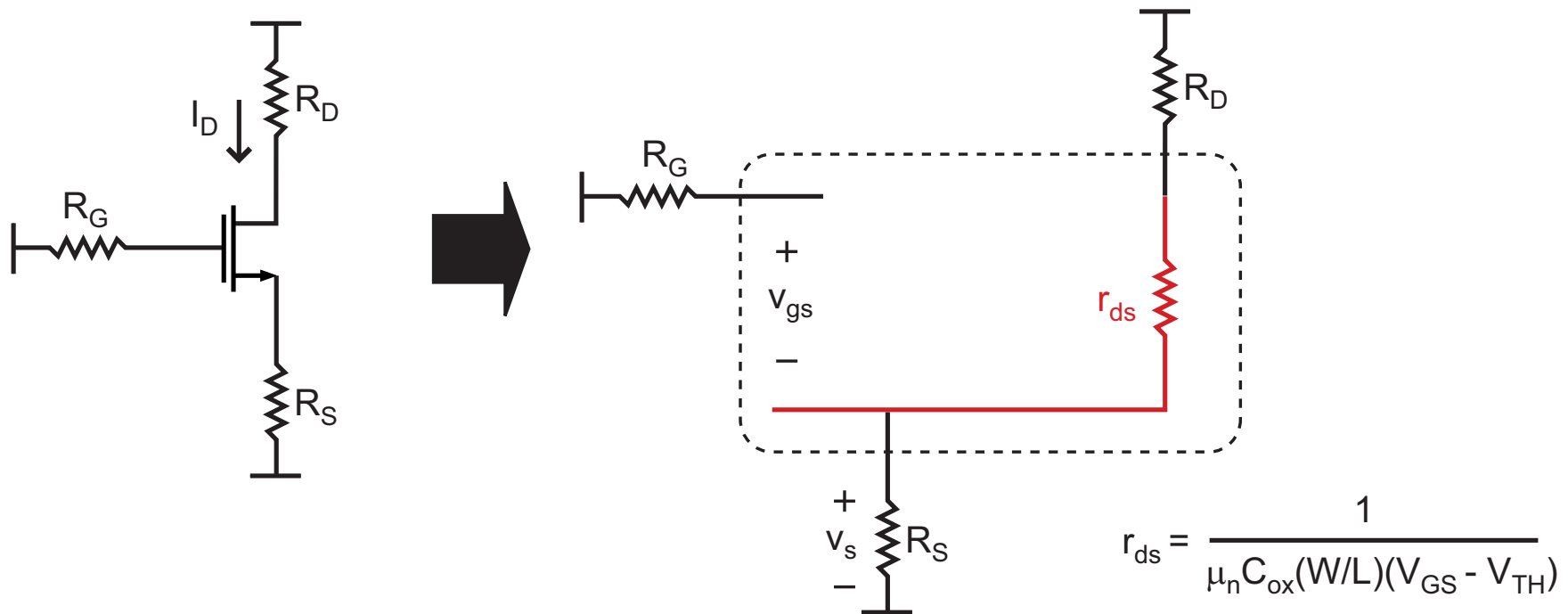
In practice: $g_{mb} = g_m/5$ to $g_m/3$

$$r_o = \frac{1}{\lambda I_D}$$

See Chapter 2 of Razavi for more discussion of these formulas

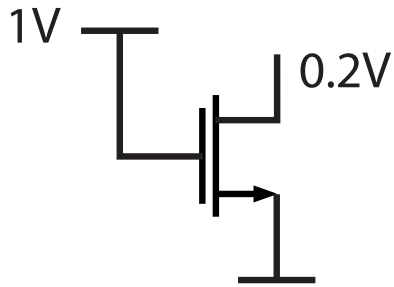
MOS DC Small Signal Model

- Assuming transistor is in triode region:
 - The channel of the device can be approximated as a resistor whose value depends on the DC operating point of V_{gs}



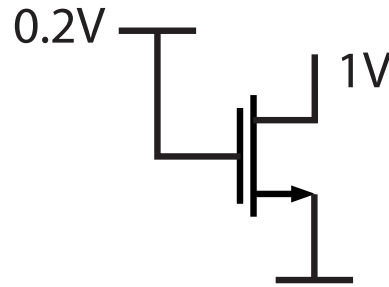
Example: Determine ΔV and Operating Region (NMOS)

- Assume $V_{THn} = 0.5V$



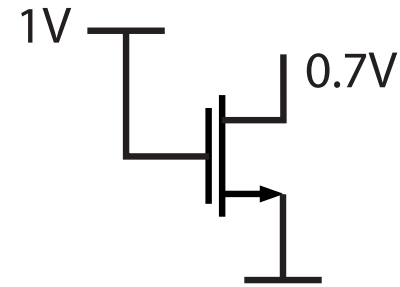
$\Delta V =$

Region =



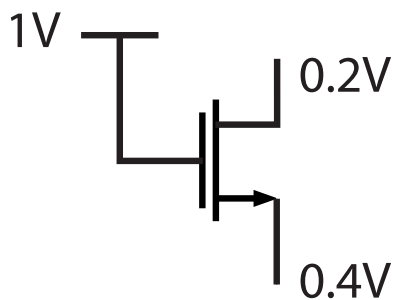
$\Delta V =$

Region =



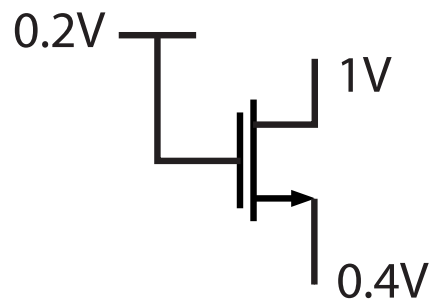
$\Delta V =$

Region =



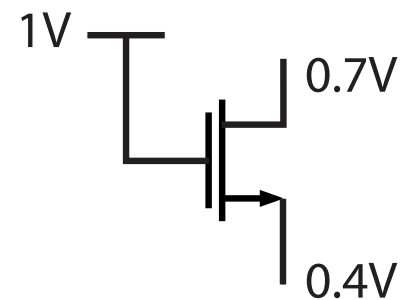
$\Delta V =$

Region =



$\Delta V =$

Region =

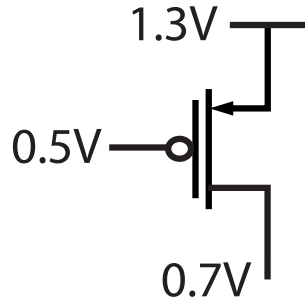


$\Delta V =$

Region =

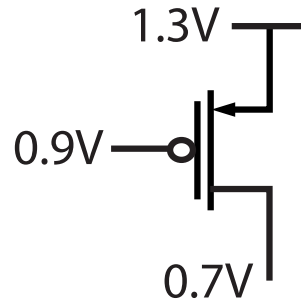
Example: Determine ΔV and Operating Region (PMOS)

- Assume $V_{THp} = -0.5V$



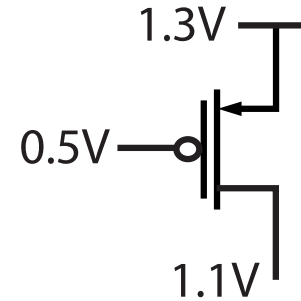
$\Delta V =$

Region =



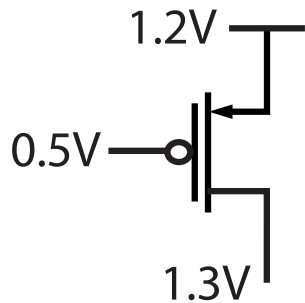
$\Delta V =$

Region =



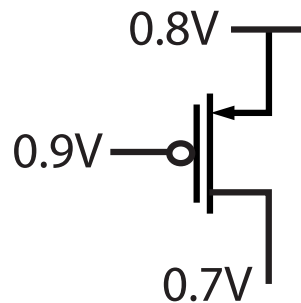
$\Delta V =$

Region =



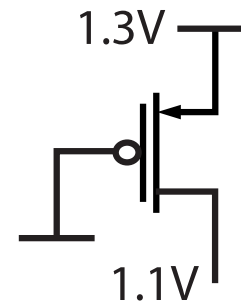
$\Delta V =$

Region =



$\Delta V =$

Region =

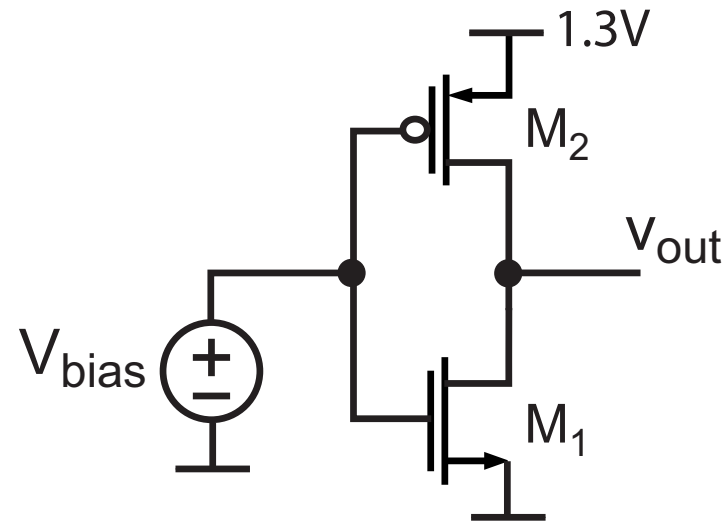


$\Delta V =$

Region =

Example: Determine Operating Region of M_1 and M_2

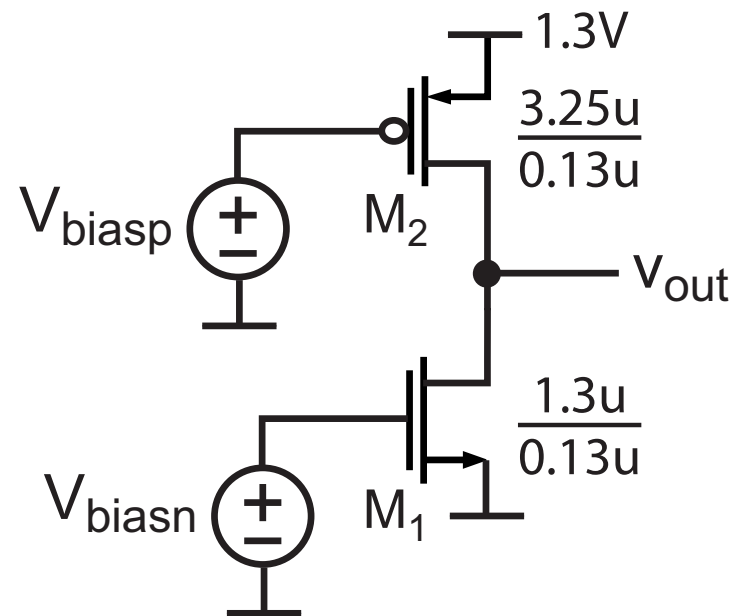
- Assume $V_{THn} = 0.5V$, $V_{THp} = -0.5V$, $\mu_n C_{ox} = 50\mu A/V^2$, $\mu_p C_{ox} = 20\mu A/V^2$, $\lambda = 0$, and M_1 and M_2 have the same value of W and L



- Determine operating region for M_1 and M_2 assuming:
 - $V_{bias} = 1.2$
 - $V_{bias} = 0.2$
 - $V_{bias} = 0.65$

Example: Determine ΔV and Operating Region

- Assume $V_{\text{biasp}} = 0.7\text{V}$, $V_{\text{THn}} = 0.5\text{V}$, $V_{\text{THp}} = -0.5\text{V}$,
 $\mu_n C_{\text{ox}} = 50\mu\text{A/V}^2$, $\mu_p C_{\text{ox}} = 20\mu\text{A/V}^2$, $\lambda = 0$



- Determine V_{biasn} such that $V_{\text{out}} = 0.5\text{V}$
 - Note that with $\lambda = 0$, a variety of V_{out} solutions will exist for the same V_{biasn} – I'm just trying to keep calculations simple
- Determine the resulting operating region of M_1 and M_2