

Analysis and Design of Analog Integrated Circuits
Lecture 23

Analog to Digital Conversion

Michael H. Perrott

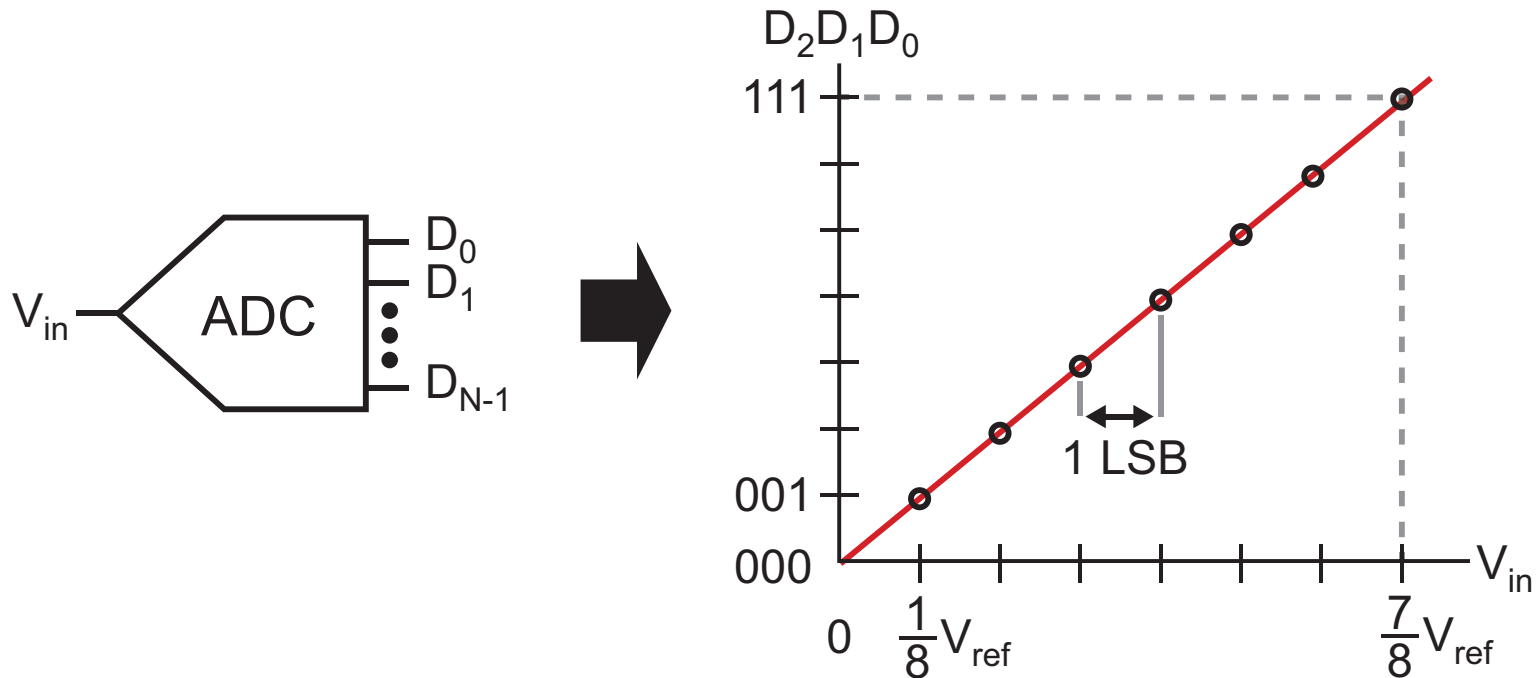
May 4, 2011

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Outline of Lecture

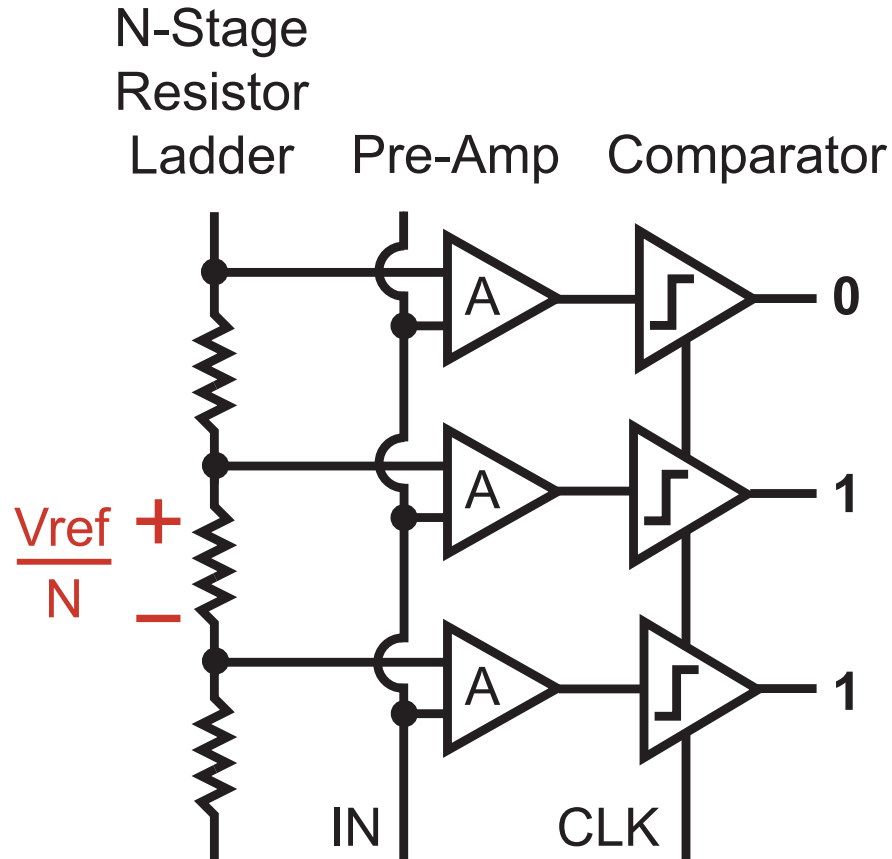
- **ADC Topologies**
 - Flash
 - SAR
 - Pipeline
 - Interleaved
 - Sigma-Delta
- **Special focus on the emerging area of VCO-based ADCs**

Analog to Digital Conversion



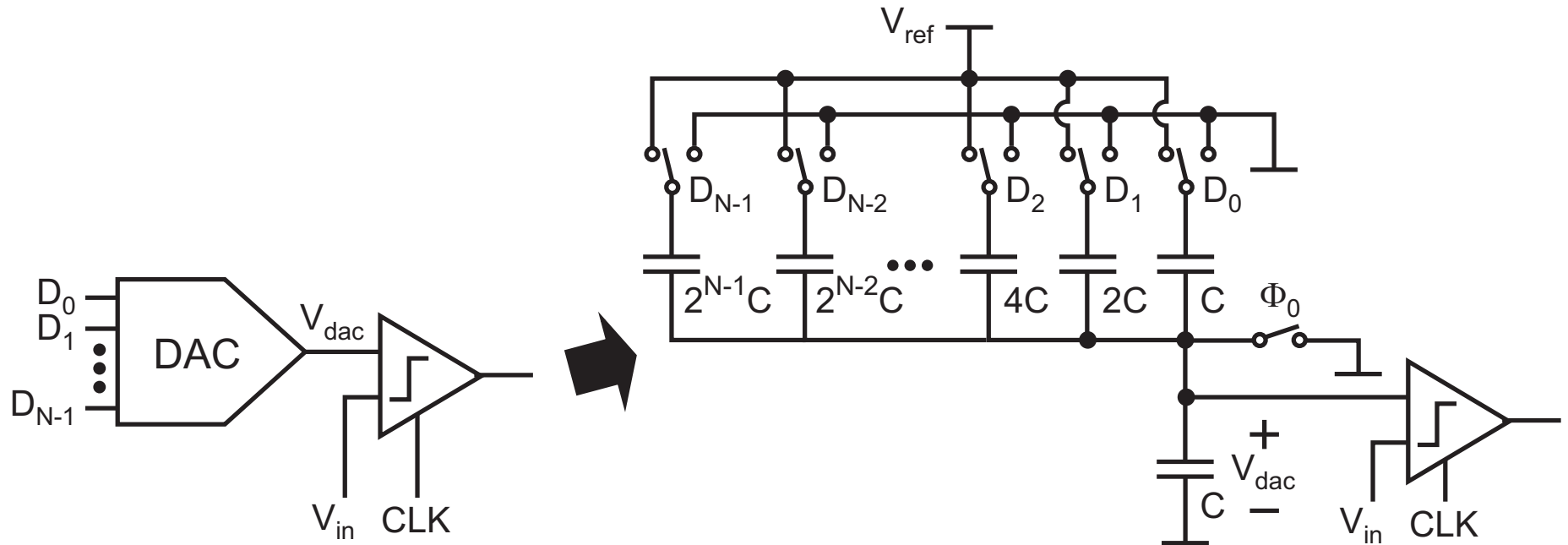
- Analog input is typically voltage
- Digital output consists of bits, D_k , with values 0 or 1
- Key characteristics similar to DAC
 - Full scale = V_{ref}
 - Resolution = $V_{ref}/2^N = 1 \text{ LSB}$
 - Nonlinearity measured with INL, DNL, Monotonicity

Flash ADC



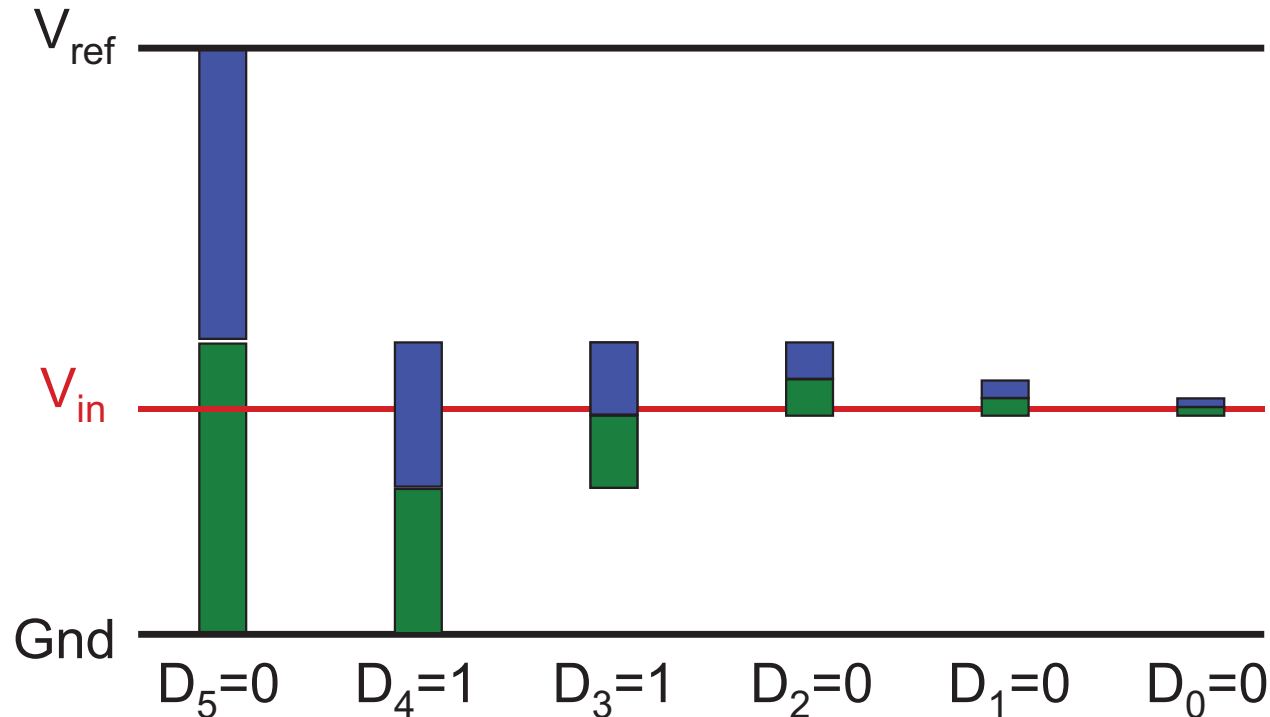
- **Fastest ADC structure (> 1 GHz)**
 - Performs direct comparison of an input signal to a set of voltage references using parallel comparators
 - Typically limited to 8-bit resolution
 - Relatively large area and power for higher resolution

SAR ADC



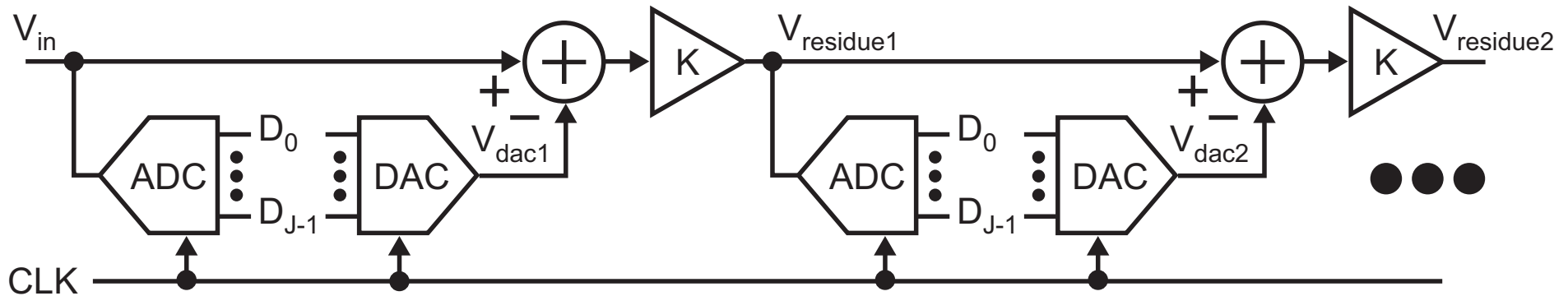
- **Leverages a DAC to sequentially compare its output values to the input voltage**
 - Minimal analog complexity - requires only one comparator and a capacitor DAC
 - Successive Approximation Algorithm (SAR) is efficient comparison algorithm for comparing DAC to input value
 - Has recently become very attractive in advanced CMOS for modest resolution (i.e., 8 to 10 bits) applications

SAR Algorithm



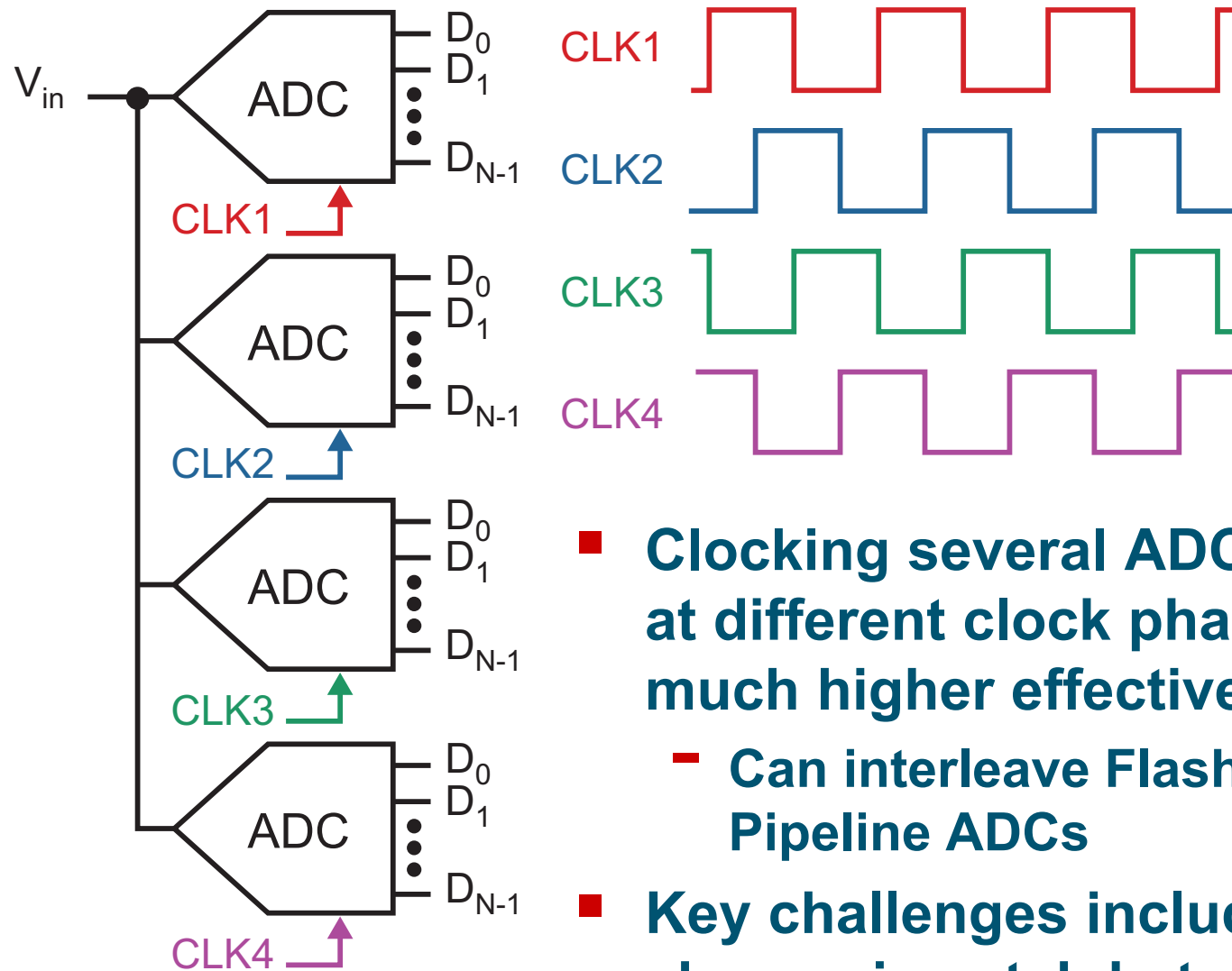
- We can efficiently compare the DAC output to the input voltage, V_{in} , by successively subdividing the range from MSB to LSB
 - Number of comparisons \approx number of bits
 - Example: 10-bit SAR ADC requires roughly 10 comparisons per sample

Pipeline ADC



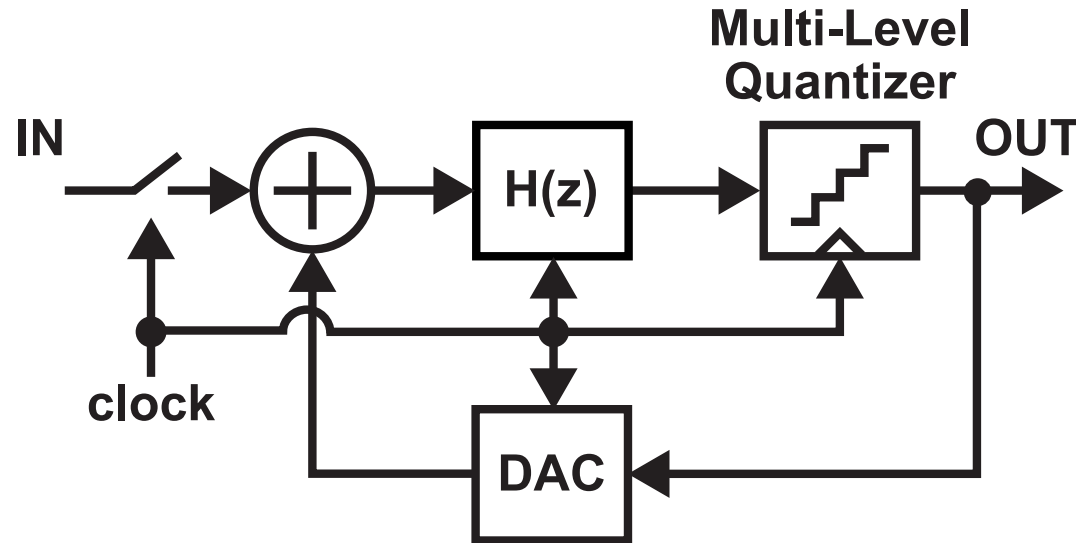
- **Resolves ADC bits in several stages**
 - Earlier stages resolve MSB bits
 - Calculate *residue* for later stages through subtraction of MSB estimate
 - Amplify residue so that all stages operate over similar voltage ranges
- **Pipeline trends**
 - 1-bit per stage in the past; now going to multi-bit per stage
 - For advanced CMOS, interleaved SAR architectures are starting to look more attractive than pipelines

Interleaved ADC



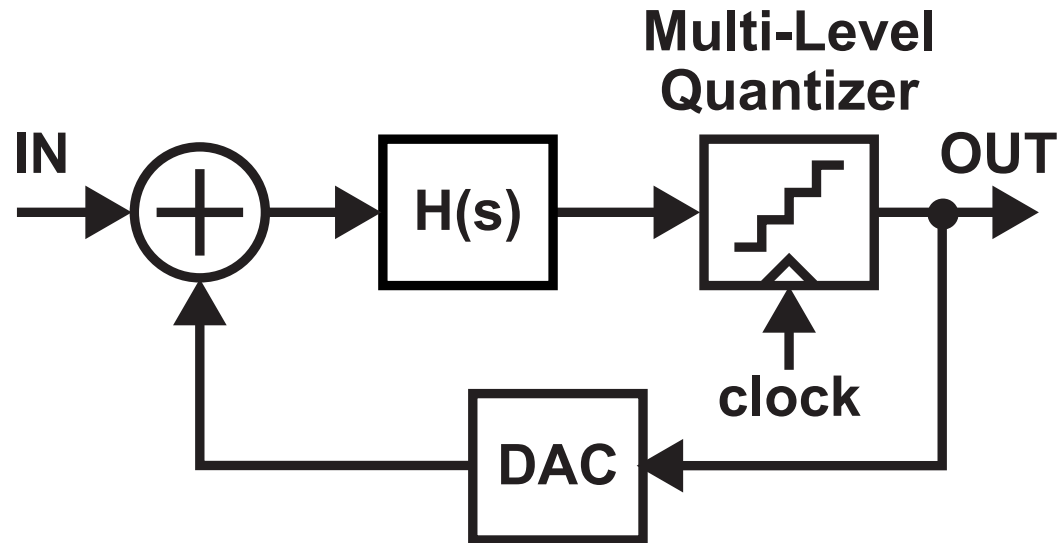
- **Clocking several ADC structures at different clock phases allows much higher effective sample rate**
 - Can interleave Flash, SAR, or Pipeline ADCs
- **Key challenges include clock skew, mismatch between ADCs, higher input capacitance**

Sigma-Delta ADC (Discrete-Time)



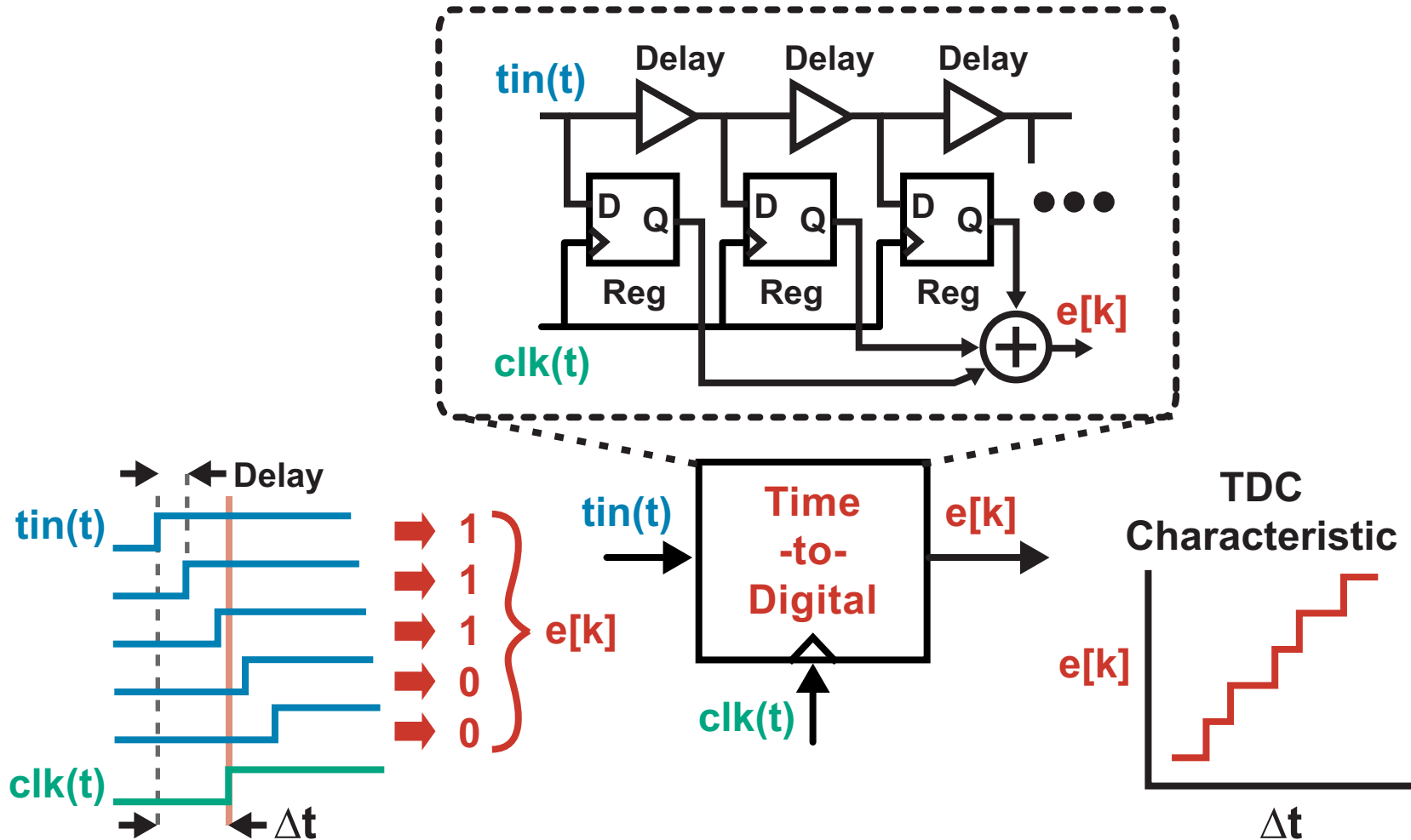
- **Oversampled input**
 - Clock rate is much higher than bandwidth of input signal
- **Noise shaped quantization noise**
 - Uses similar concepts as Sigma-Delta DAC considered in Lecture 22
 - Leads to high effective precision despite having a coarse quantizer

Sigma-Delta ADC (Continuous-Time)



- **Similar to Discrete-Time, but important differences**
 - **Sampler occurs after the filtering**
 - Allows removal of high frequency noise before sampling
 - **Only the quantizer and DAC need to settle during each sample**
 - Allows higher speed

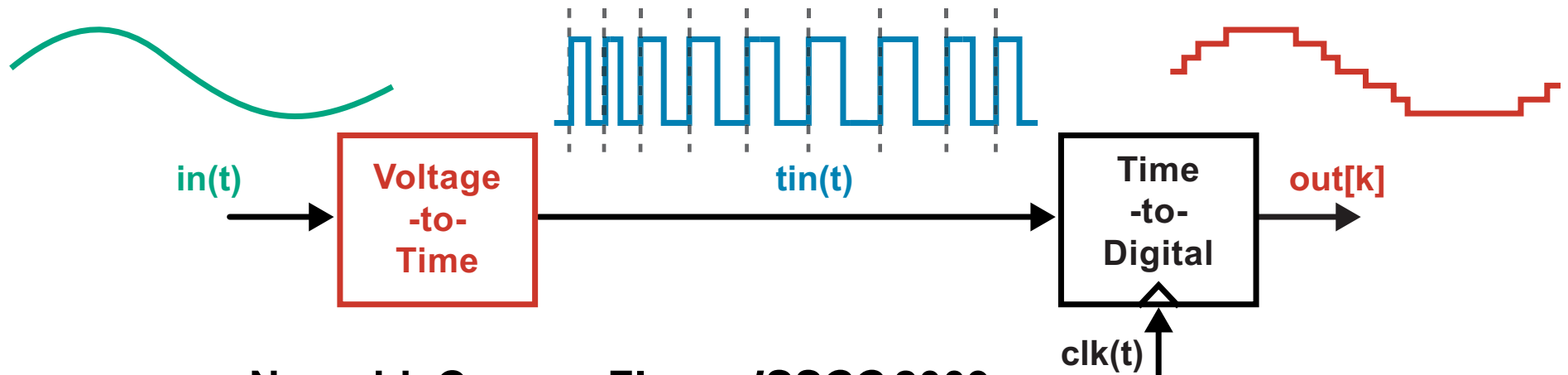
Time-to-Digital Conversion



- Quantization in time achieved with purely digital gates
 - Easy implementation, resolution improving with Moore's law

How can we leverage this for quantizing an analog voltage?

Adding Voltage-to-Time Conversion

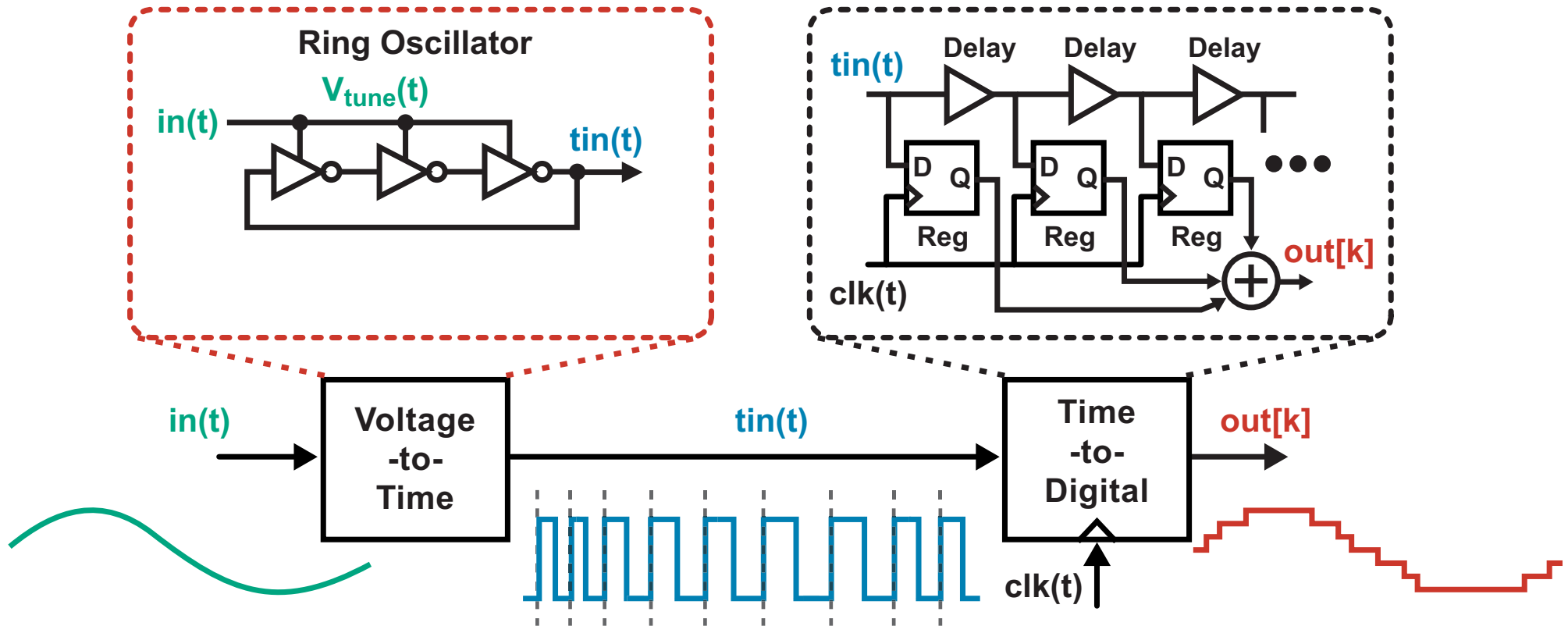


Naraghi, Courcy, Flynn, *ISSCC* 2009

- **Analog voltage is converted into edge times**
 - Time-to-digital converter then turns the edge times into digitized values
- **Key issues**
 - Non-uniform sampling
 - Noise, nonlinearity

Is there a simple implementation for the Voltage-to-Time Converter?

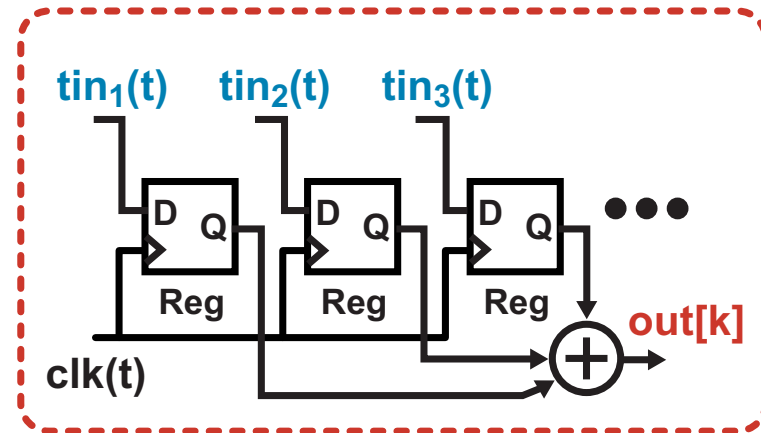
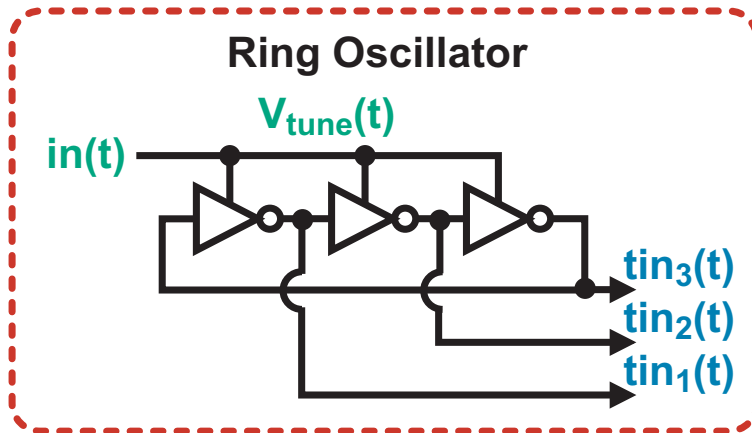
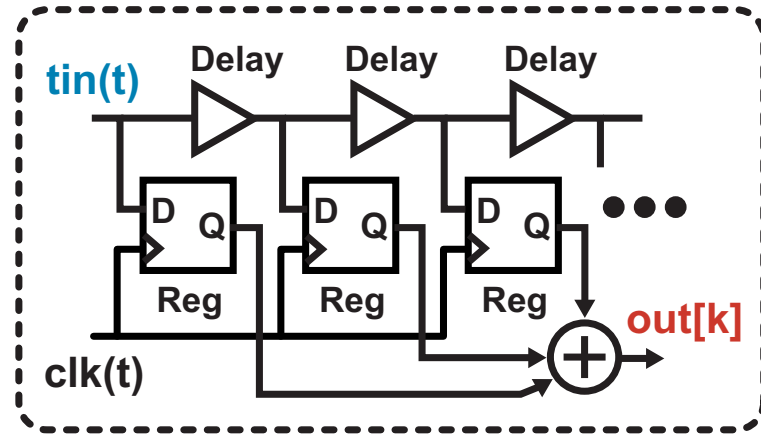
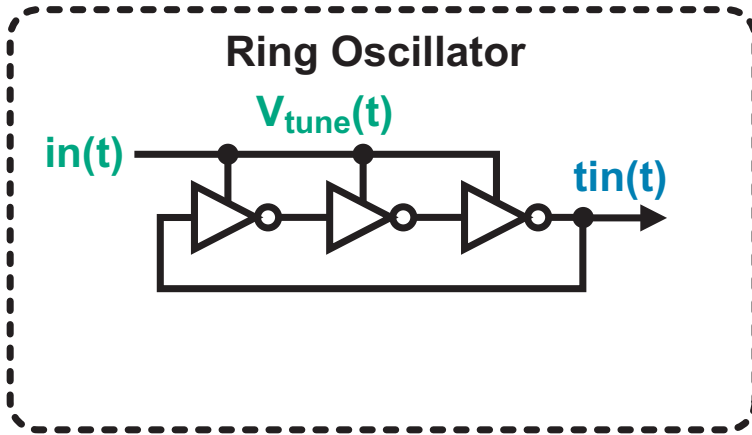
A Highly Digital ADC Implementation



- A voltage-controlled ring oscillator offers a simple voltage-to-time structure
 - Non-uniform sampling is still an issue

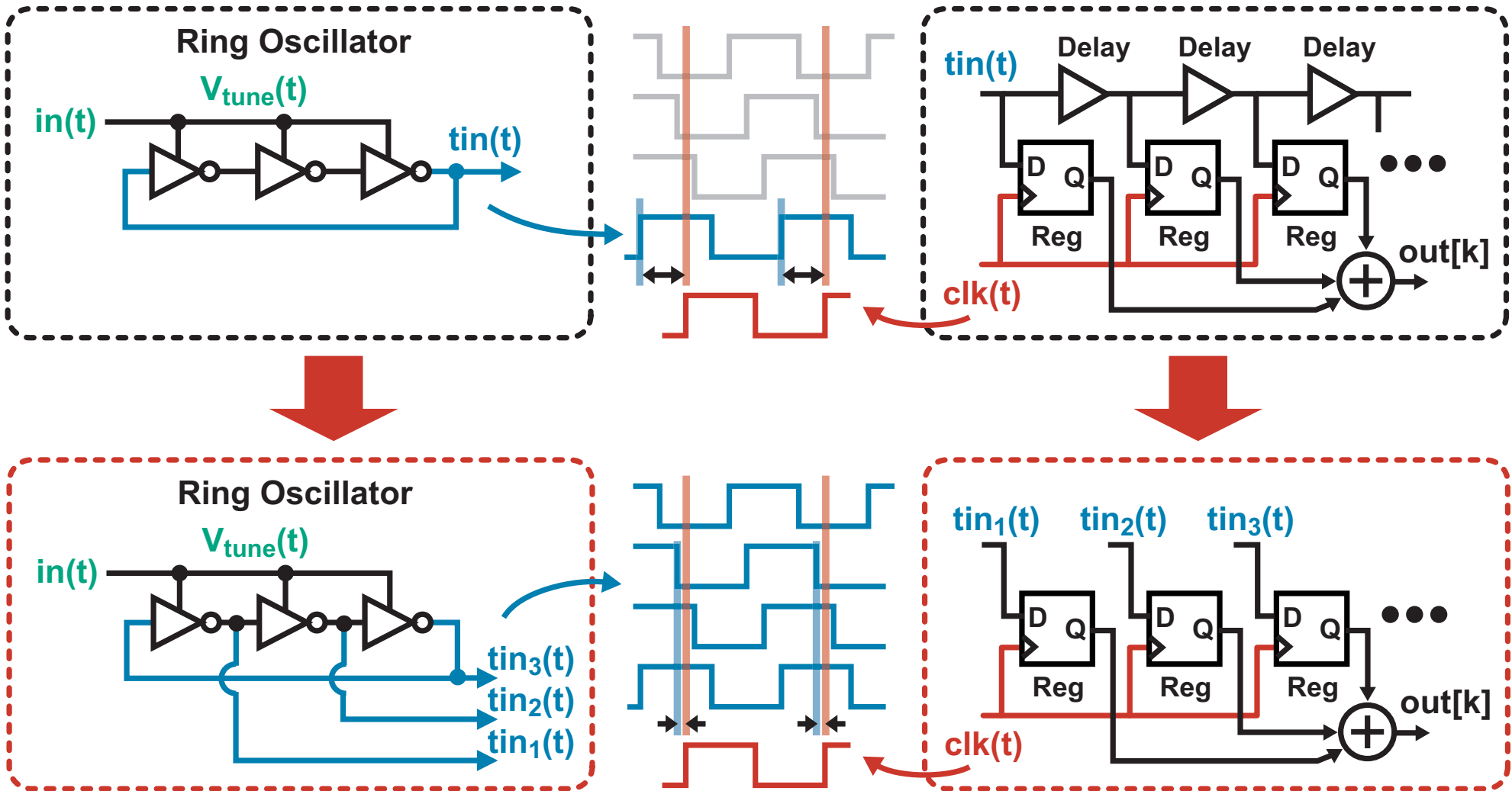
We can further simplify this implementation and lower the impact of non-uniform sampling

Making Use of the Ring Oscillator Delay Cells



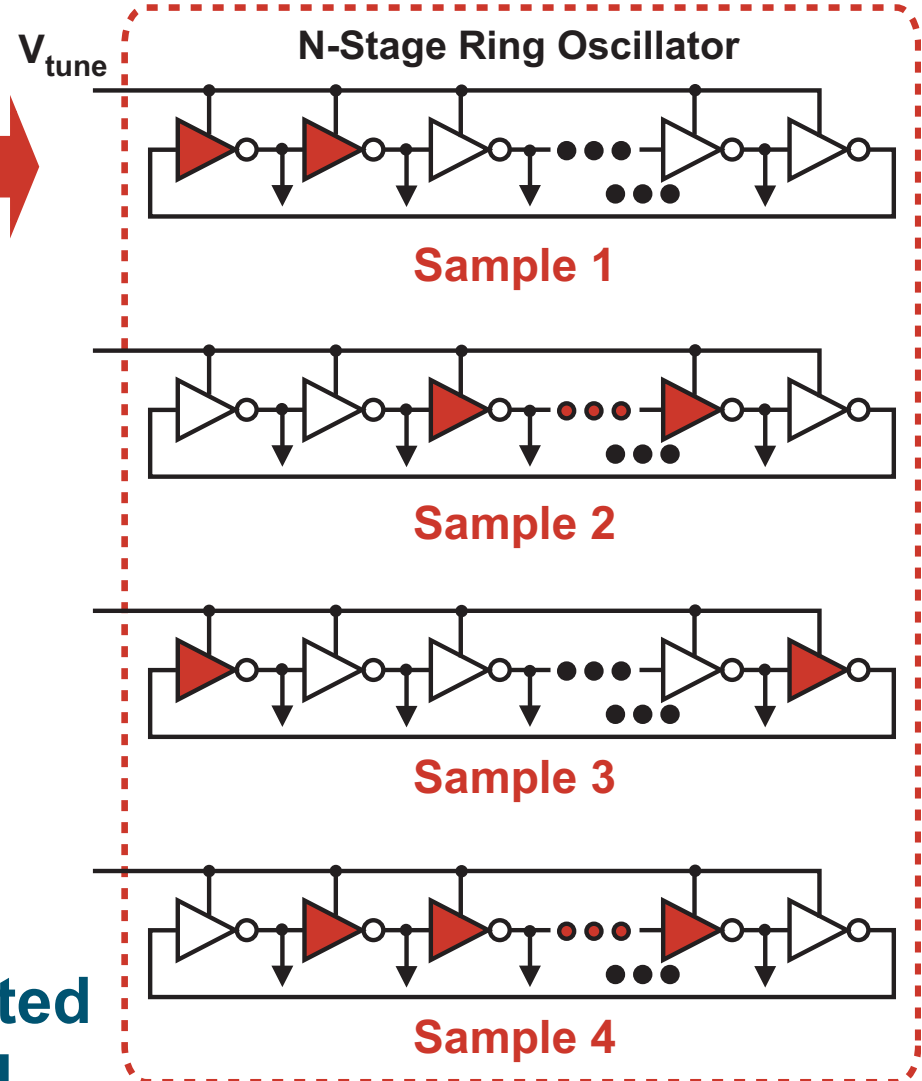
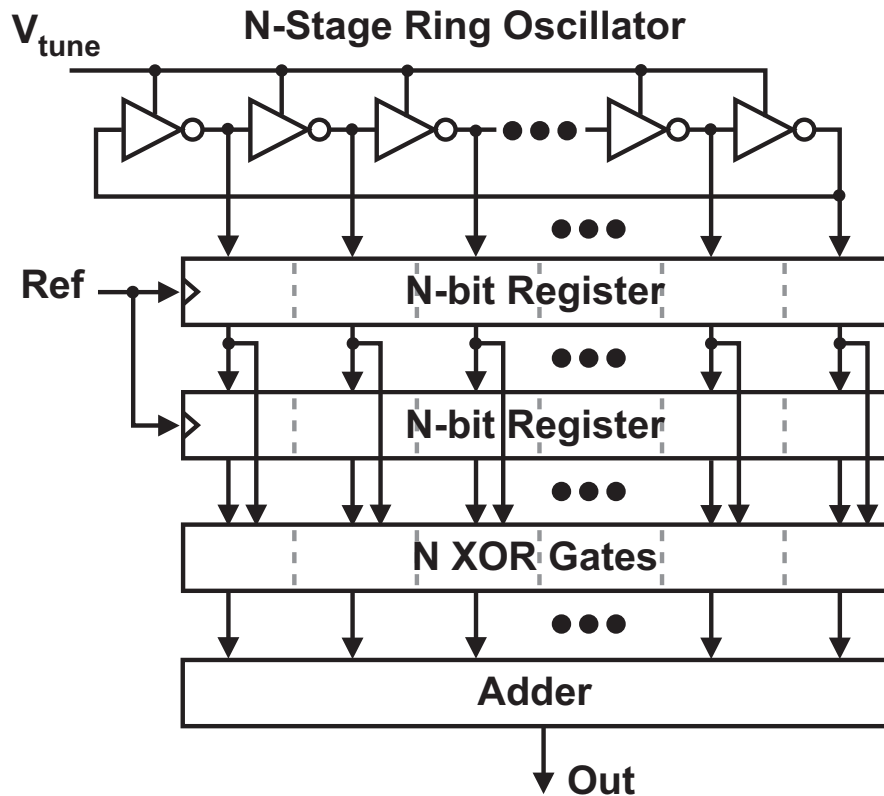
- Utilize all ring oscillator outputs and remove TDC delays
 - Simpler implementation
- TDC output now samples/quantizes phase state of oscillator

Improving Non-Uniform Sampling Behavior



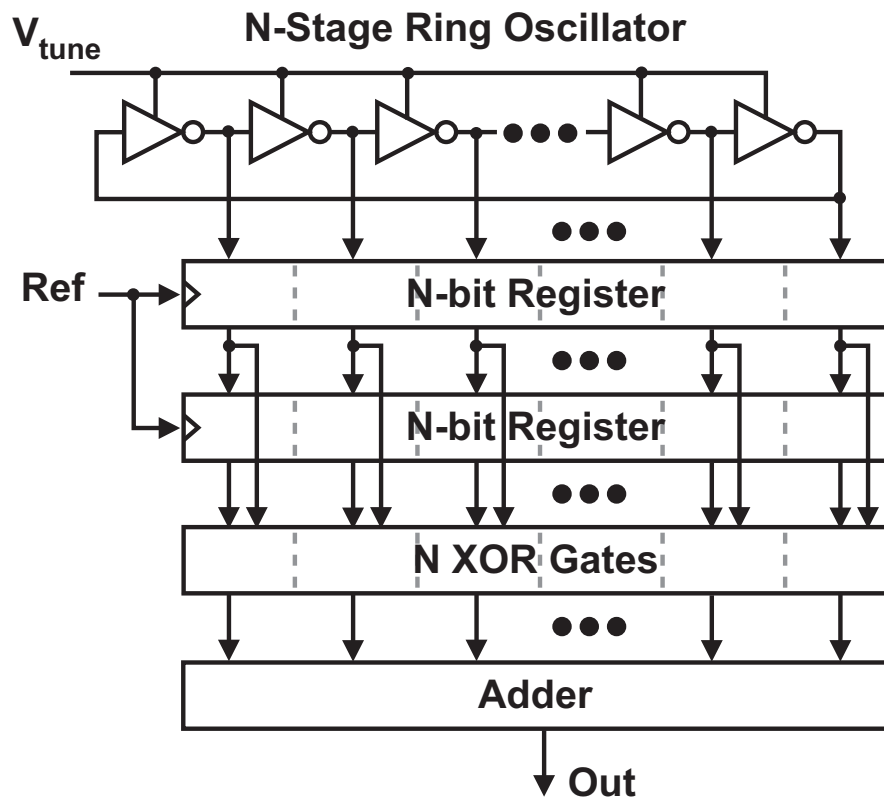
- Oscillator edges correspond to a sample window of the input
- Sampling the oscillator phase state yields sample windows that are much more closely aligned to the TDC clk

Multi-Phase Ring Oscillator Based Quantizer

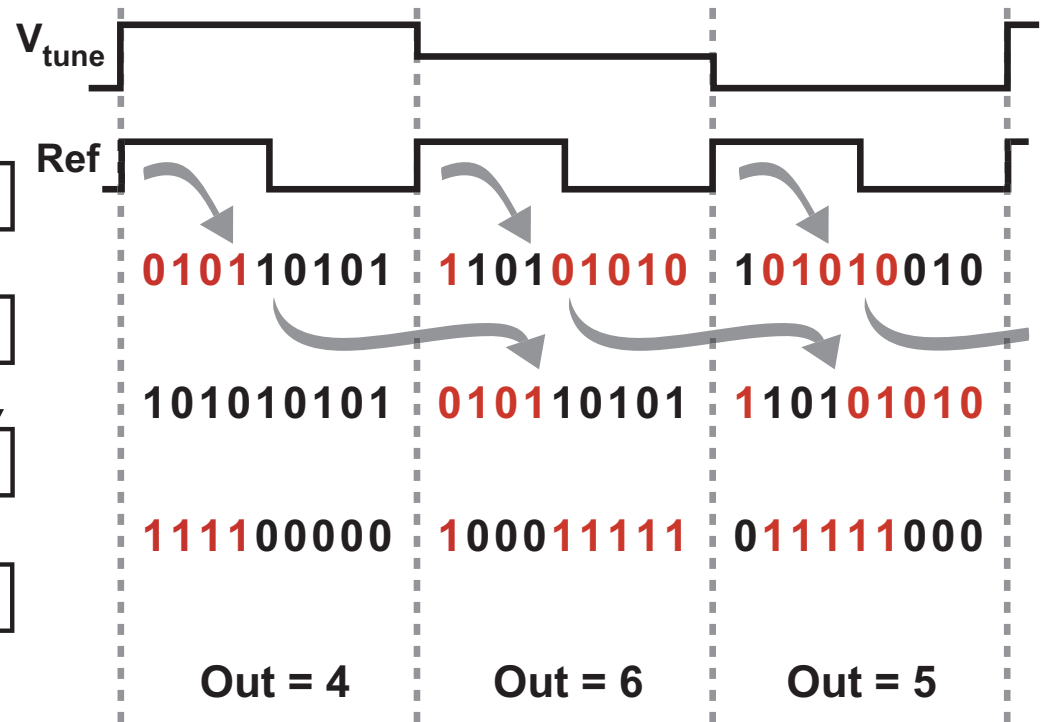


- **Adjustment of V_{tune} changes how many delay cells are visited by edges per Ref clock period**
 - **Quantizer output corresponds to the number of delay cells that experience a transition in a given Ref clock period**

More Details ...

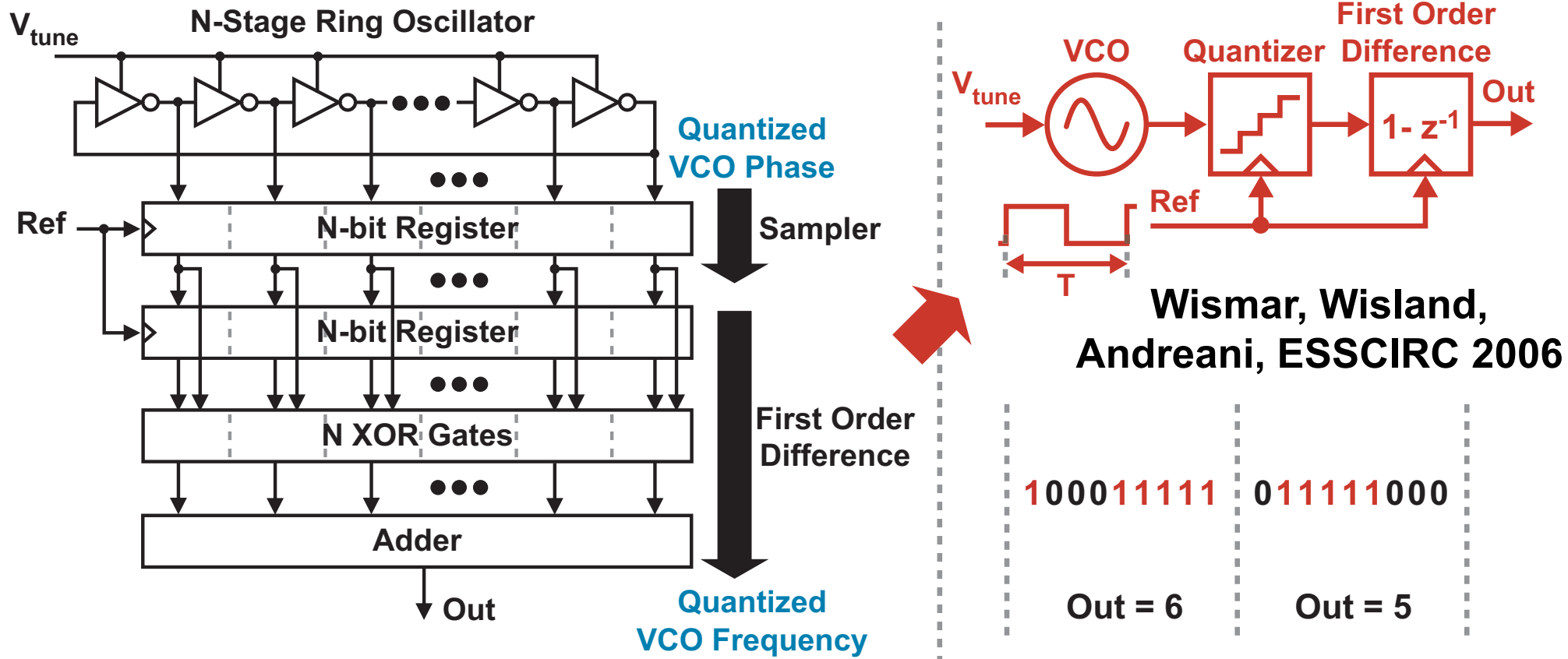


Example: Progression of 9-Stage Ring Oscillator Values



- Choose large enough number of stages, N , such that transitions never cycle through a given stage more than once per Ref clock period
 - Assume a high Ref clock frequency (i.e., 1 GHz)
- XOR operation on current and previous samples provides transition count

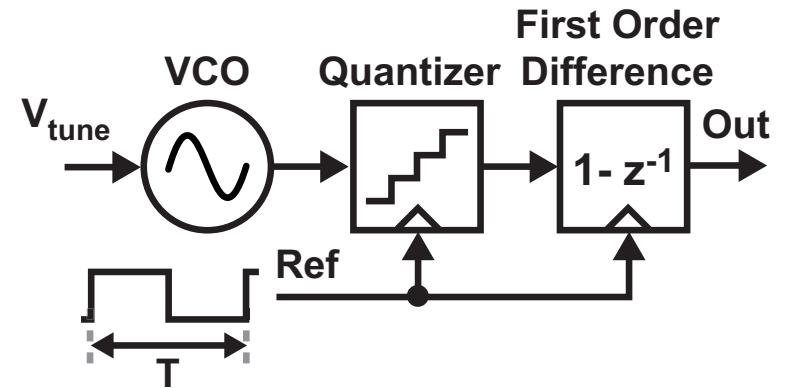
A First Step Toward Modeling



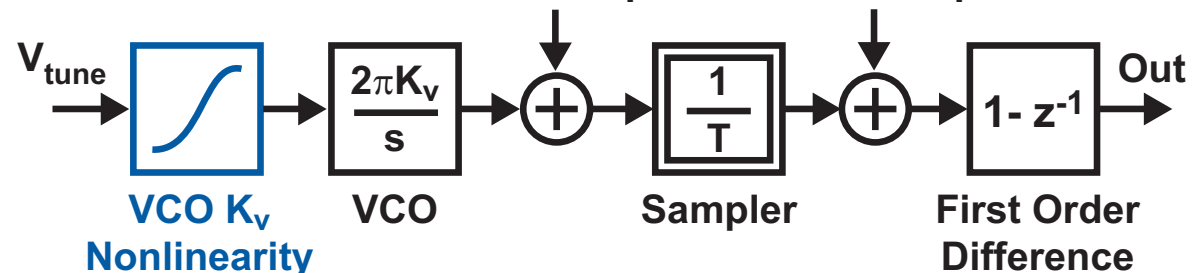
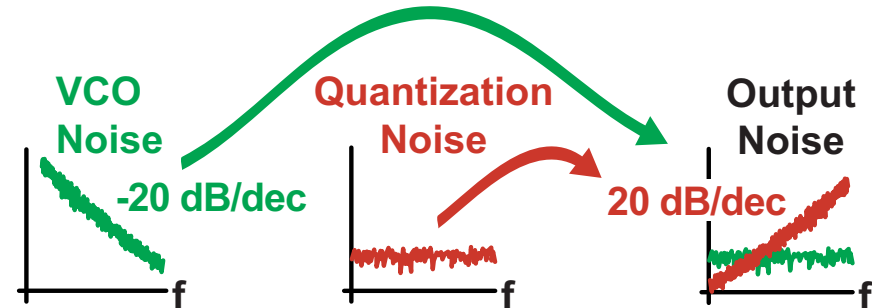
- VCO provides quantization, register provides sampling
 - Model as separate blocks for convenience
- XOR operation on current and previous samples corresponds to a first order difference operation
 - Extracts VCO frequency from the sampled VCO phase signal

Corresponding Frequency Domain Model

- VCO modeled as integrator and K_v nonlinearity
- Sampling of VCO phase modeled as scale factor of $1/T$
- Quantizer modeled as addition of quantization noise

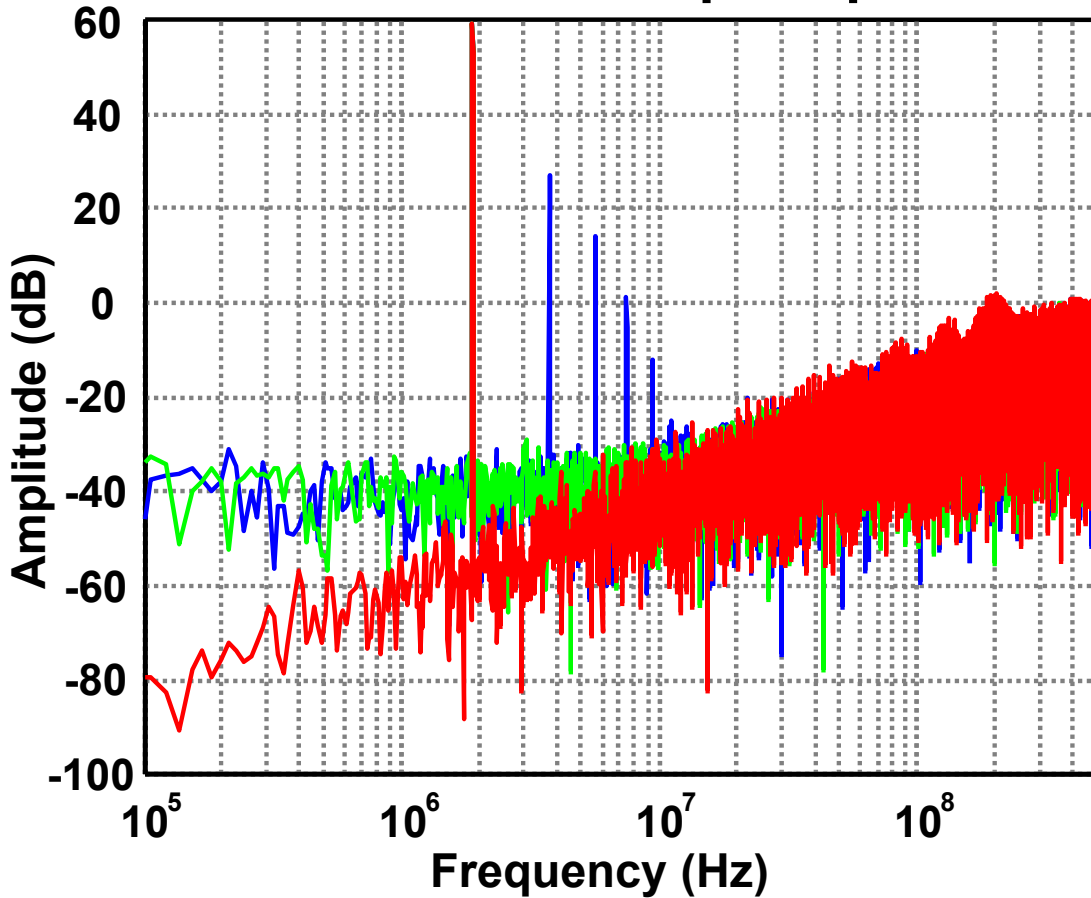


- Key non-idealities:
 - VCO K_v nonlinearity
 - VCO noise
 - Quantization noise

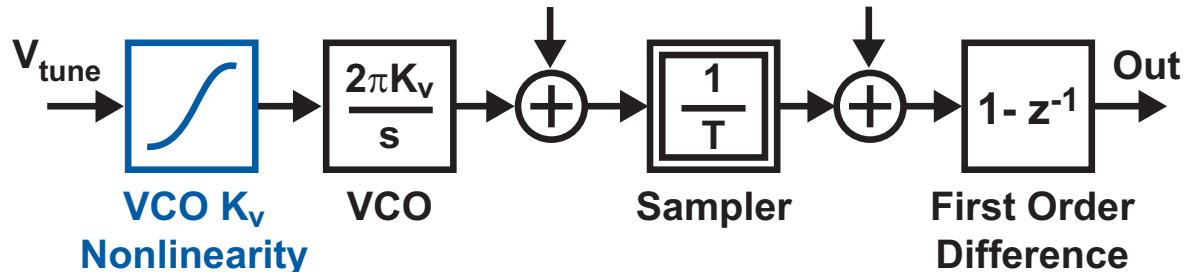
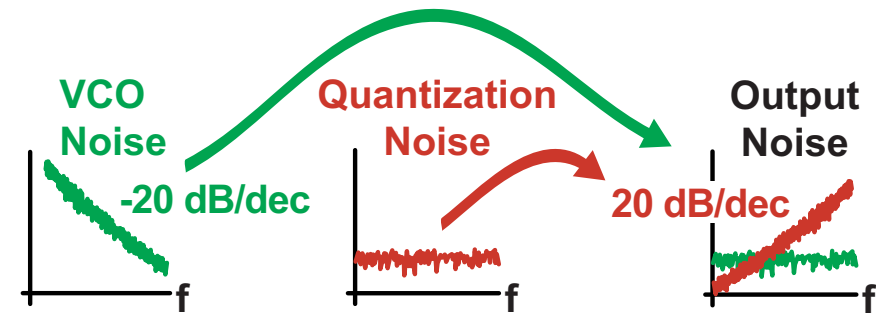


Example Design Point for Illustration

Simulated ADC Output Spectrum

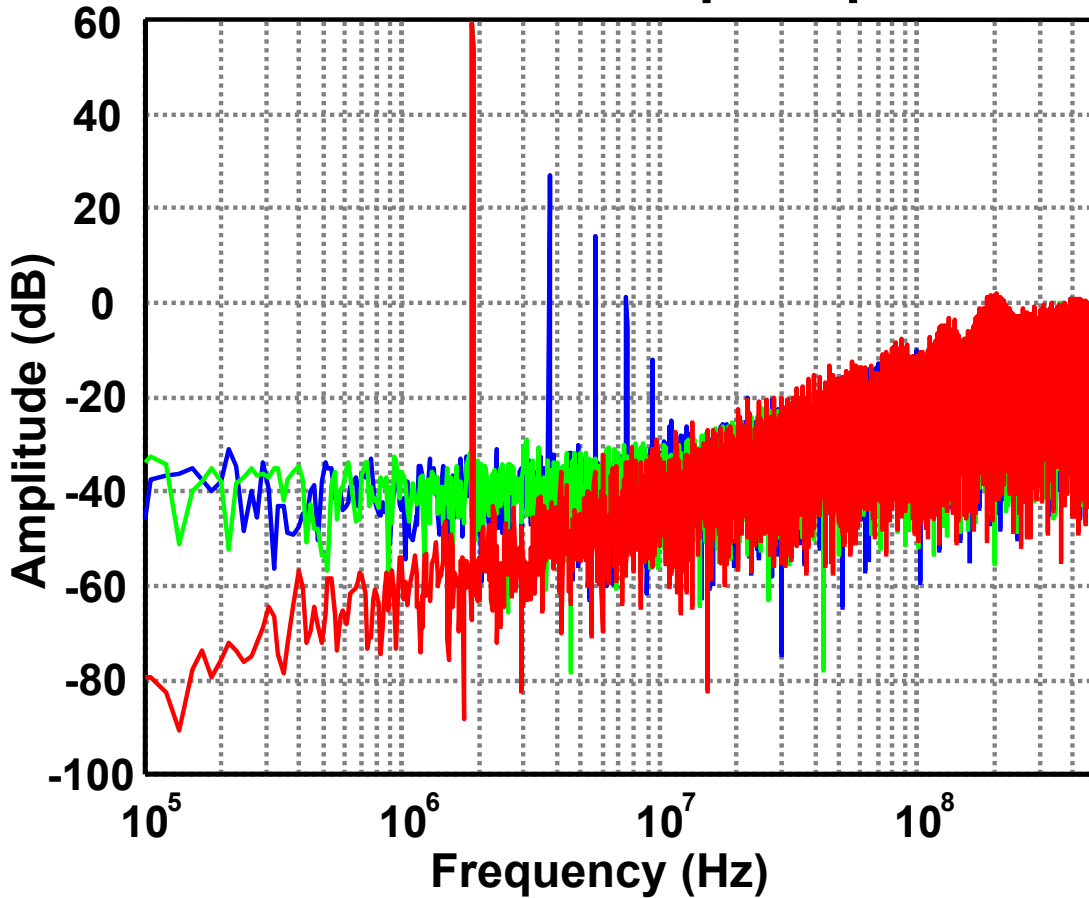


- Ref clk: $1/T = 1$ GHz
- 31 stage ring oscillator
 - Nominal delay per stage: 65 ps
- $K_{VCO} = 500$ MHz/V
 - $\pm 5\%$ linearity
- VCO noise: -100 dBc/Hz at 10 MHz offset

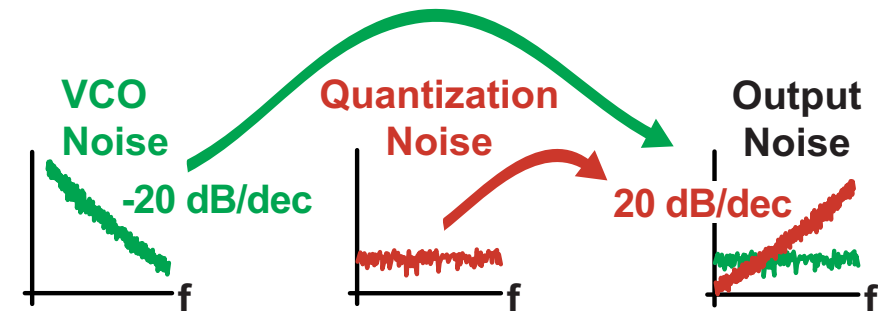


SNR/SNDR Calculations with 20 MHz Bandwidth

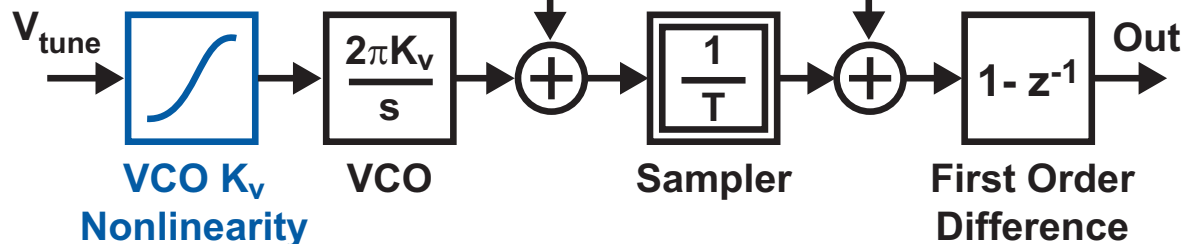
Simulated ADC Output Spectrum



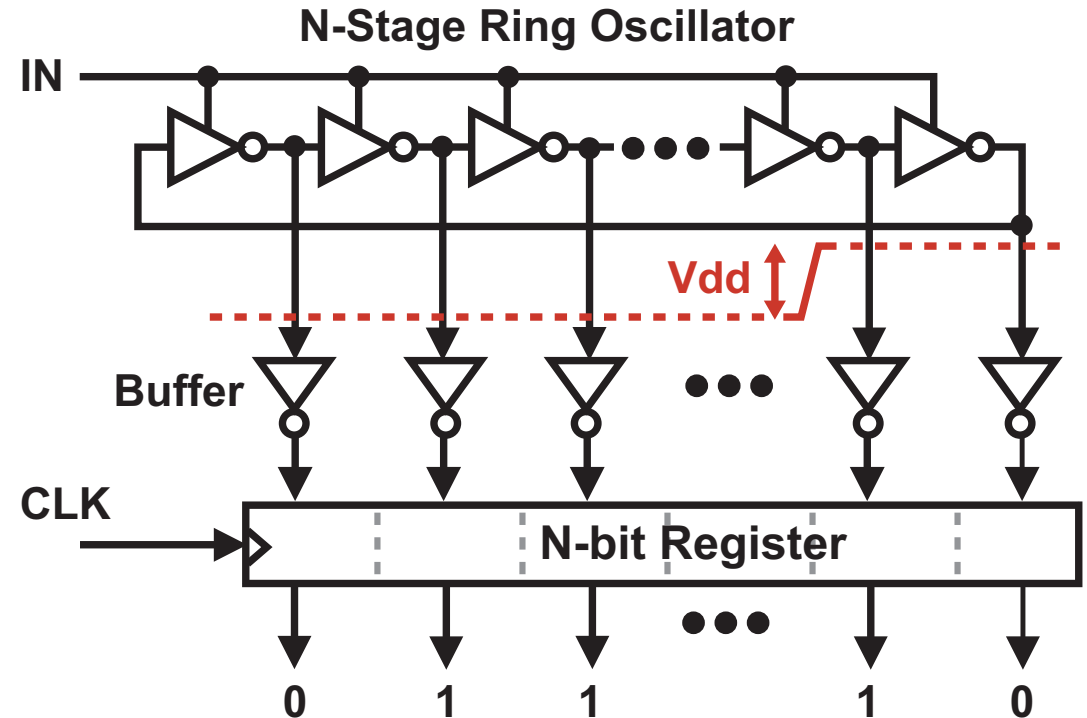
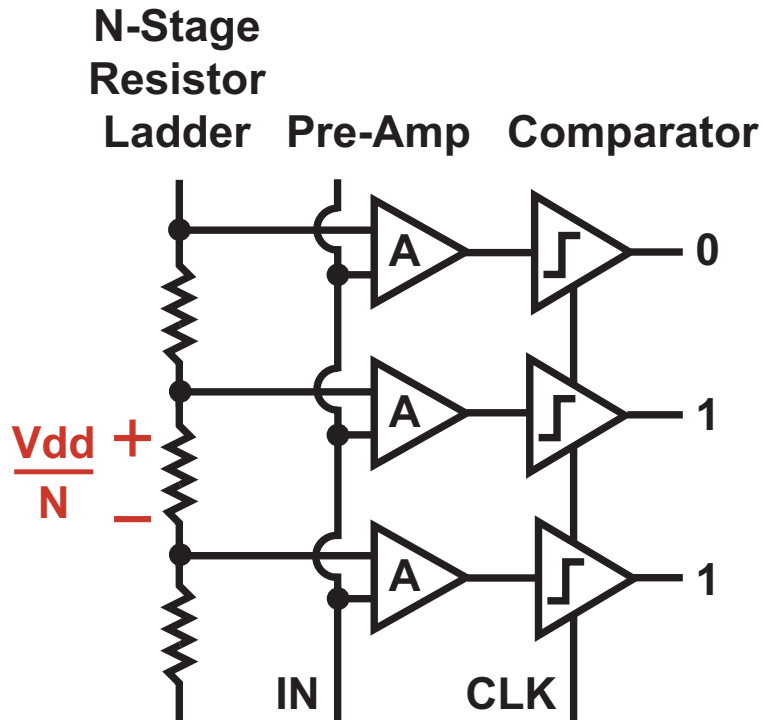
Conditions	SNDR
Ideal	68.2 dB
VCO Thermal Noise	65.4 dB
VCO Thermal + Nonlinearity	32.2 dB



VCO K_v nonlinearity is the key performance bottleneck



Classical Analog Versus VCO-based Quantization

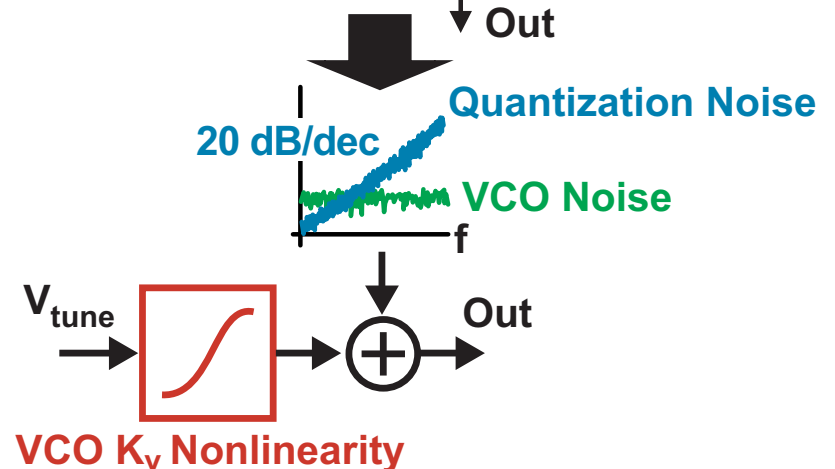
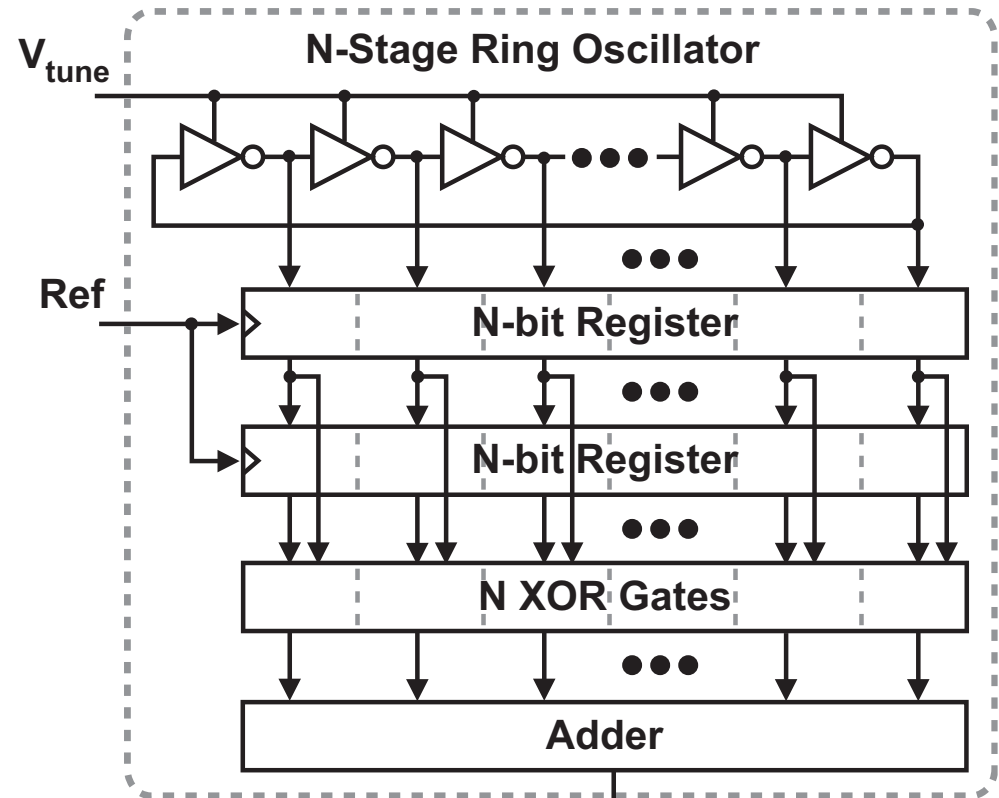


- Much more digital implementation
- Offset and mismatch is not of critical concern
- Metastability behavior is potentially improved
- Improved SNR due to quantization noise shaping

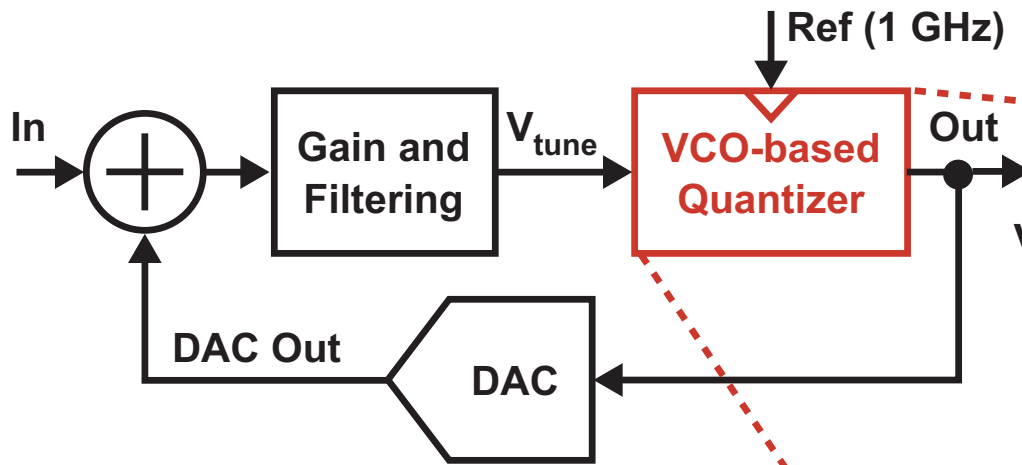
Implementation is high speed, low power, low area

Key Performance Issues: Nonlinearity and Noise

- Very hard to build a simple ring oscillator with linear K_v
- Noise floor set by VCO phase noise is typically higher than for analog amplifiers at same power dissipation

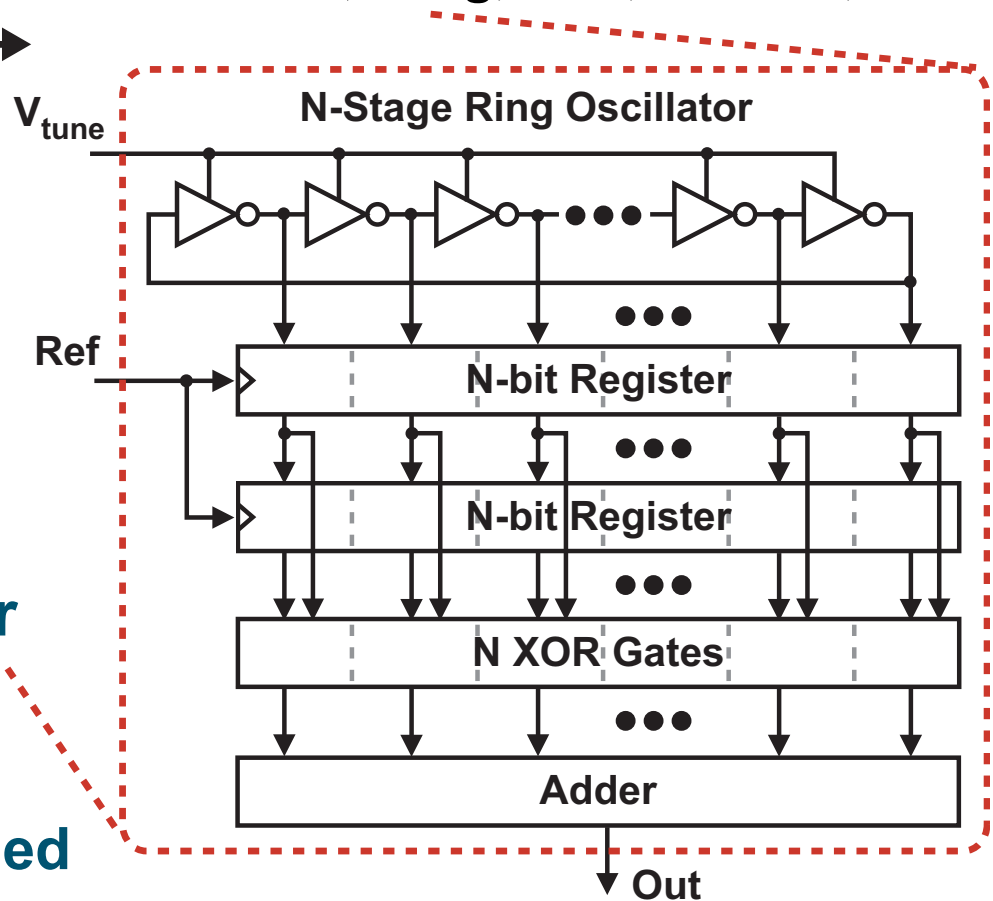


Feedback Is Our Friend



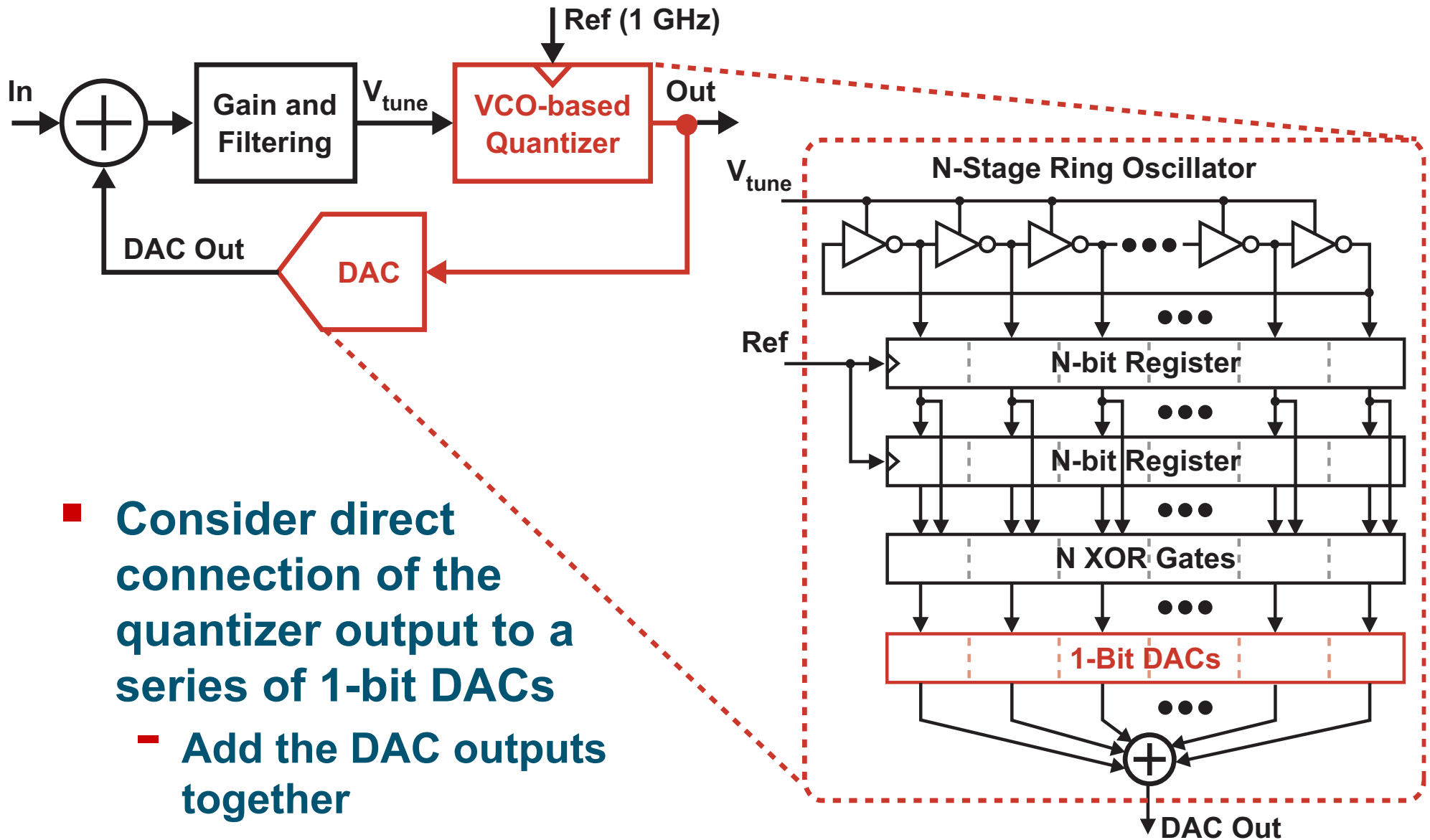
Iwata, Sakimura, TCAS II, 1999
Naiknaware, Tang, Fiez, TCAS II, 2000

- **Combining feedback with front end gain acts to suppress impact of quantizer noise and nonlinearity**
 - Scale factor from input to output is also better controlled
 - Structure is a continuous-time Sigma-Delta ADC



- **Issue: must achieve a highly linear DAC structure**
 - Otherwise, noise folding and other bad things happen ...

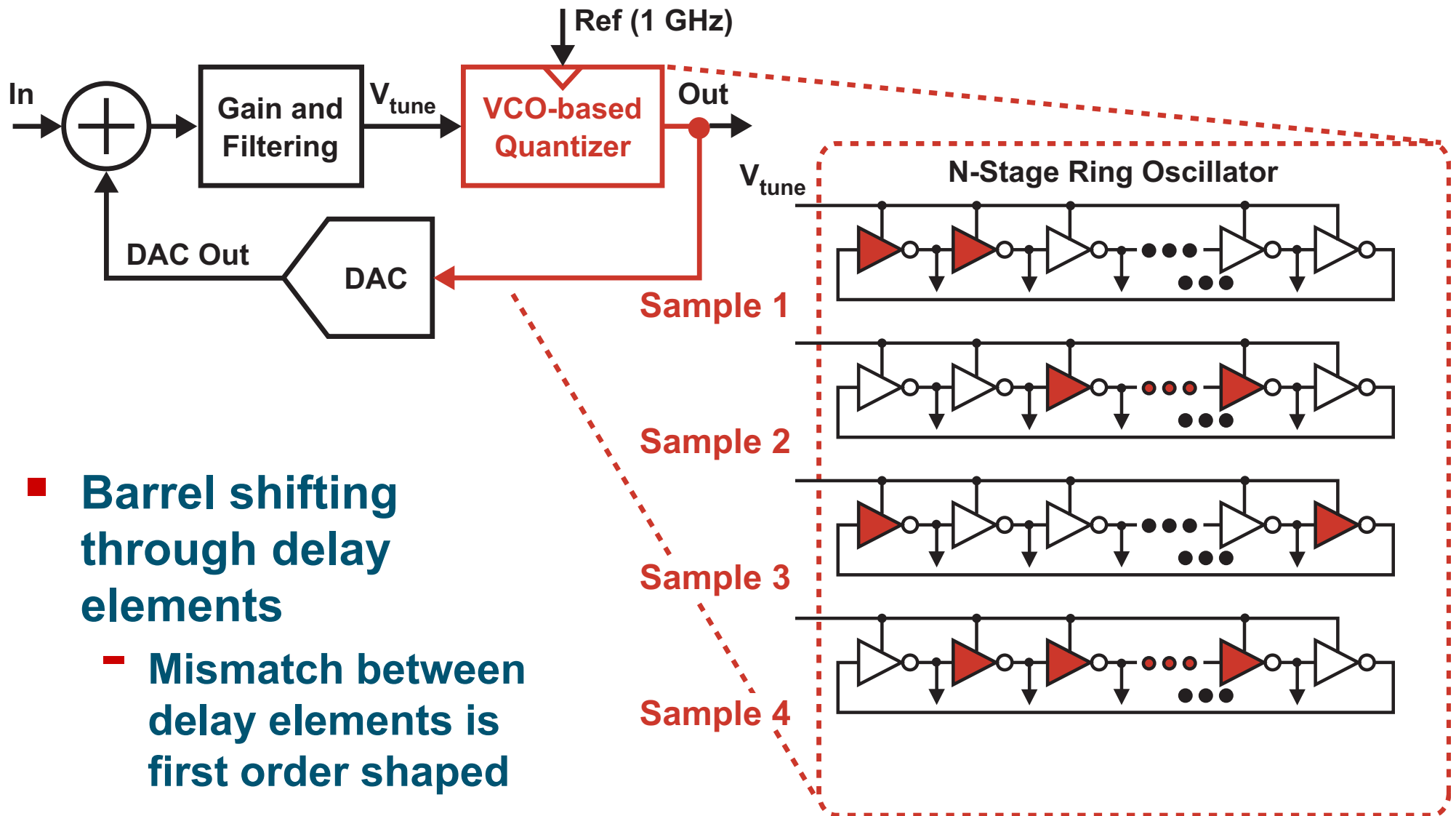
A Closer Look at the DAC Implementation



- Consider direct connection of the quantizer output to a series of 1-bit DACs
 - Add the DAC outputs together

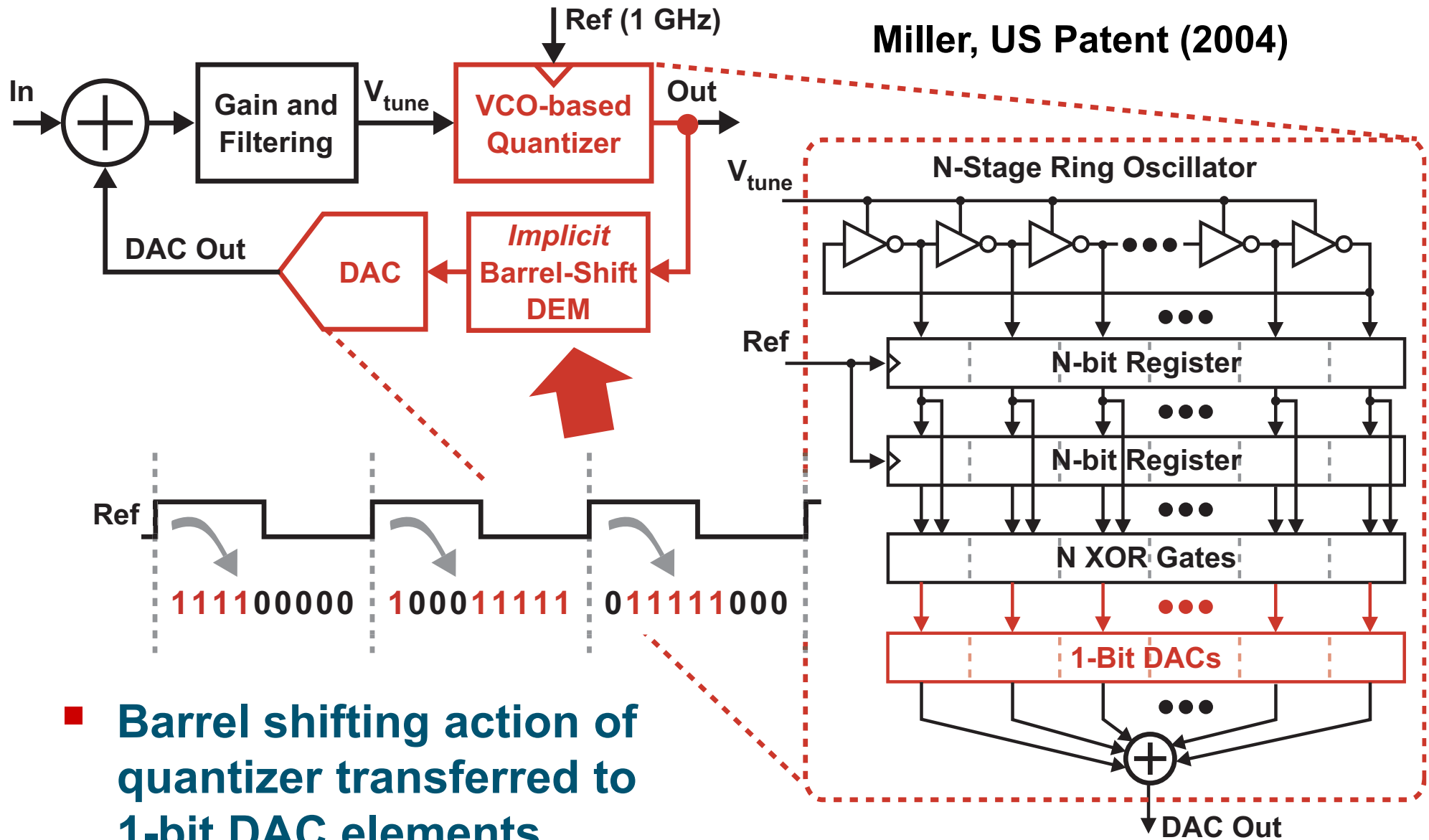
What is so special about doing this?

Recall that Ring Oscillator Offers Implicit Barrel Shifting



- Barrel shifting through delay elements
 - Mismatch between delay elements is first order shaped

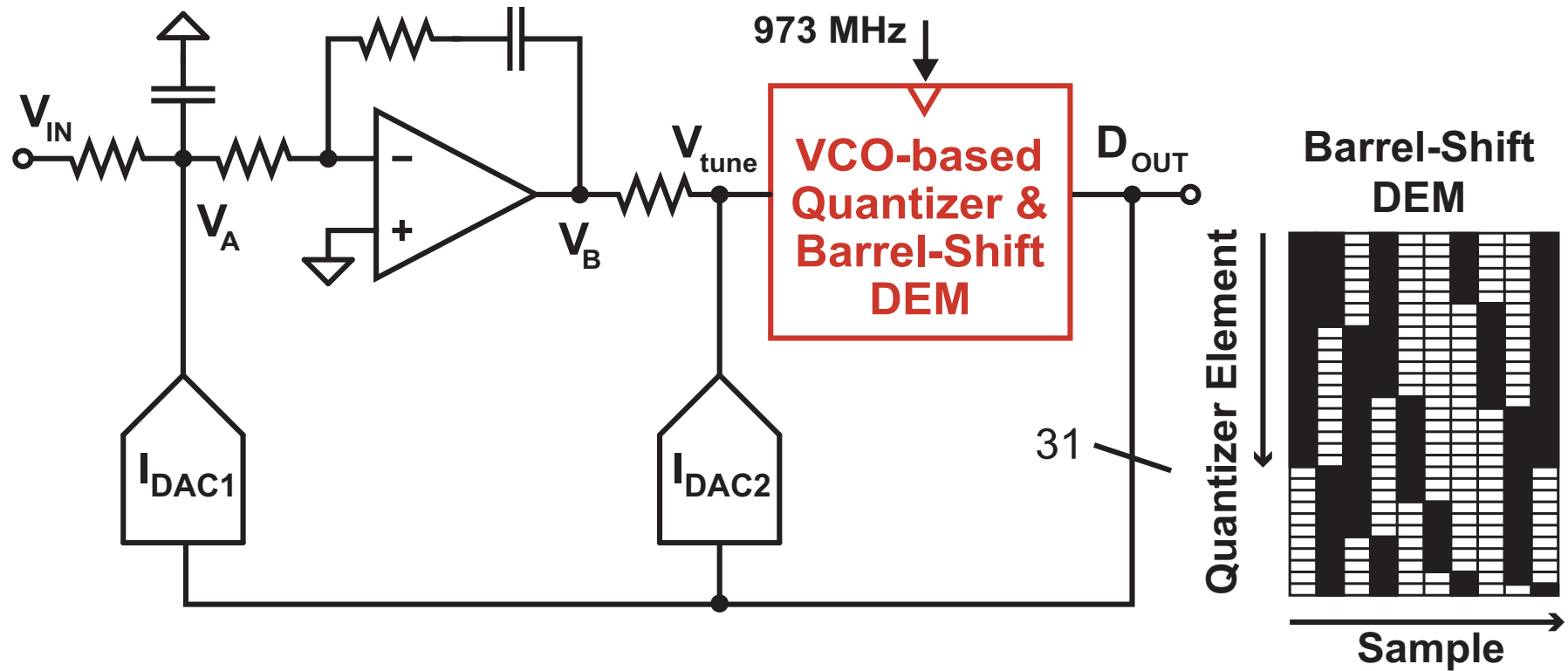
Implicit Barrel Shifting Applied to DAC Elements



- **Barrel shifting action of quantizer transferred to 1-bit DAC elements**

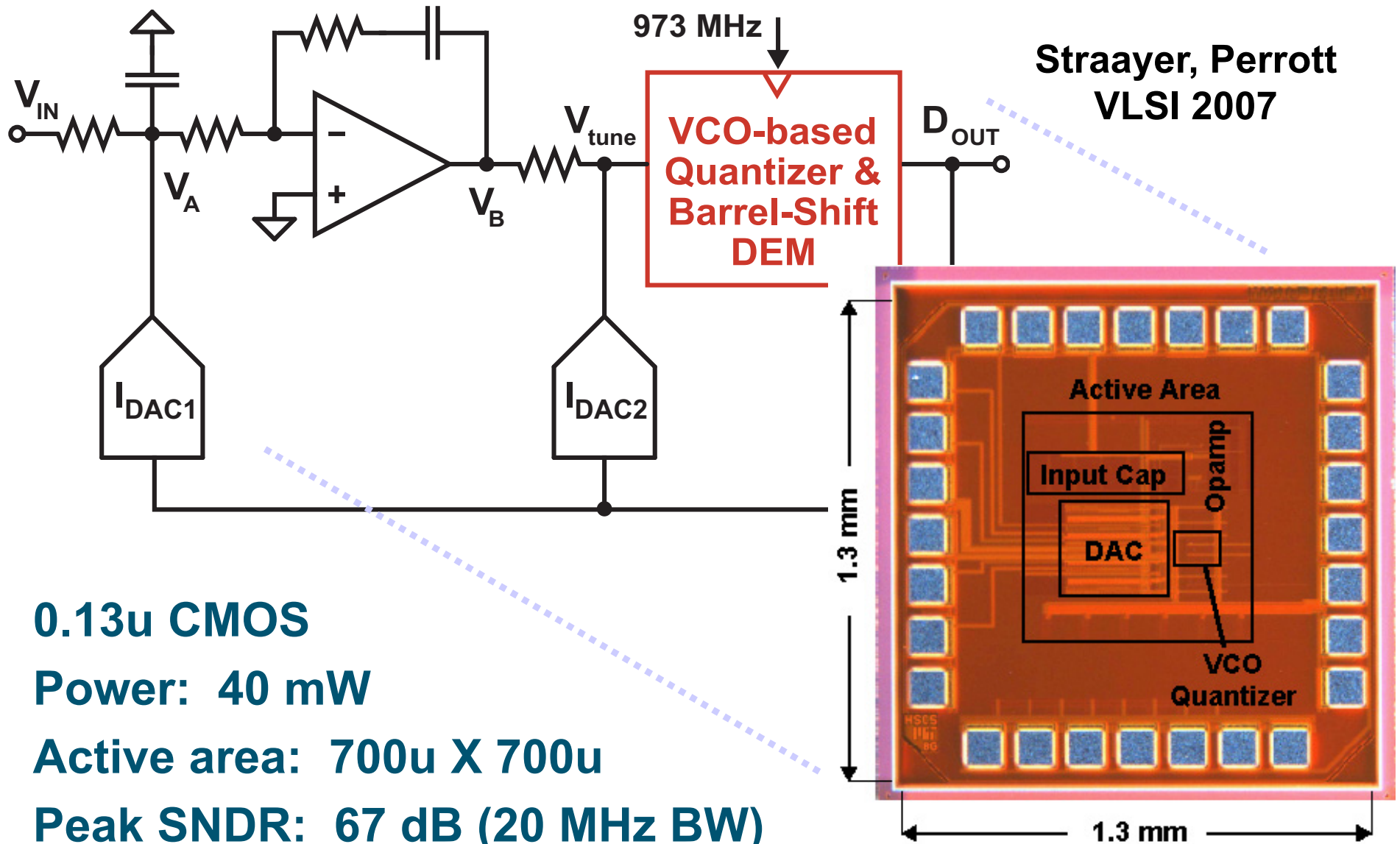
- **Acts to shape DAC mismatch and linearize its behavior**

First Generation Prototype



- **Second order dynamics achieved with only *one* op-amp**
 - Op-amp forms one integrator
 - I_{dac1} and passive network form the other (lossy) integrator
 - Minor loop feedback compensates delay through quantizer
- ***Third order* noise shaping is achieved!**
 - VCO-based quantizer adds an extra order of noise shaping

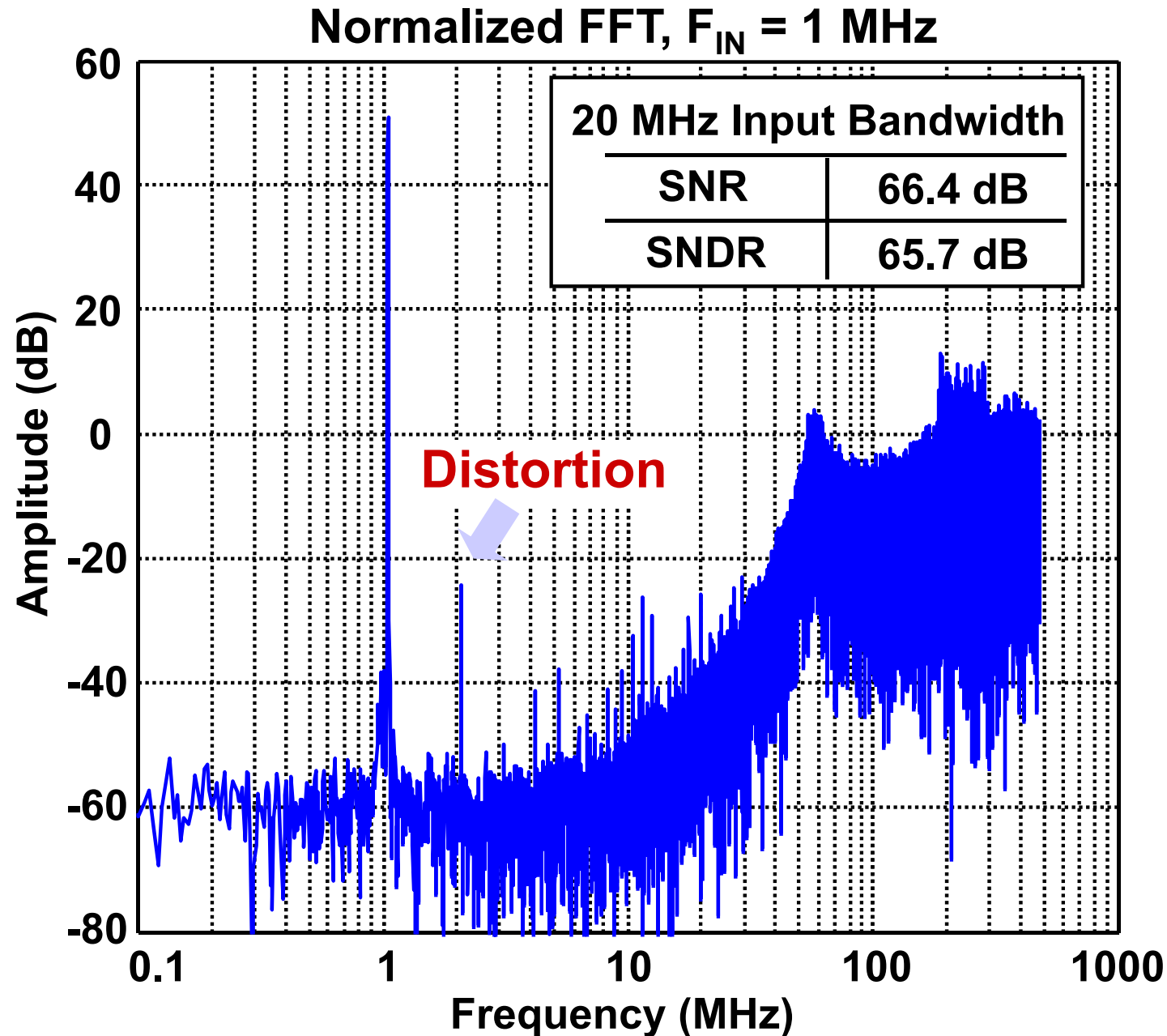
Custom IC Implementing the Prototype



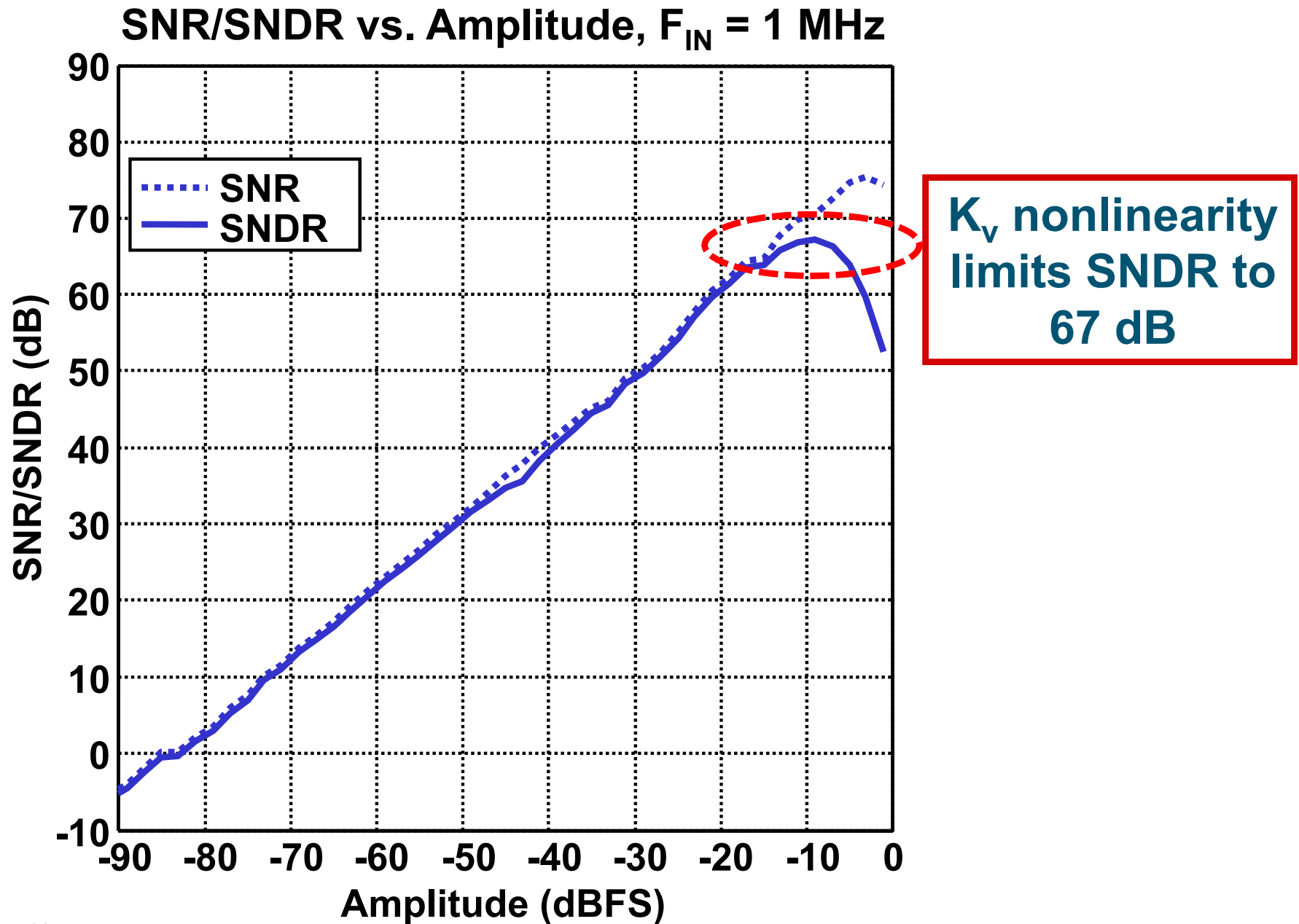
Straayer, Perrott
VLSI 2007

- 0.13u CMOS
- Power: 40 mW
- Active area: 700u X 700u
- Peak SNDR: 67 dB (20 MHz BW)
- Efficiency: 0.5 pJ/conv. step

Measured Spectrum From Prototype



Measured SNR/SNDR Vs. Input Amplitude (20 MHz BW)



Summary

- **ADC design is an active area of research**
 - Many topologies possible
 - Much innovation is still ongoing, especially as new CMOS fabrication processes are introduced
- **Key topologies**
 - Flash
 - SAR
 - Pipeline
 - Sigma-Delta
- **VCO-based ADCs are a new area of interest**
 - Take advantage of high speed of new CMOS processes
 - Leverage digital circuits
 - Can achieve good performance, but innovation still needed