Analysis and Design of Analog Integrated Circuits
Lecture 21

Sampling

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Outline of Lecture

- Basic CMOS sampling structure
- Feedback sampling
- Noise of CMOS sampling structure
The Need for Sample and Hold Circuits

- Analog-to-digital converters (ADC) are key elements in allowing digital processors to interact with “real world” signals in the acoustic, RF, and optical domains.
- Sample and hold circuits are often utilized to keep the input signal into the ADC constant while it is performing its conversion.
  - Key metrics: sampling accuracy, sampling speed, hold time (while maintaining accuracy).
**Track and Hold Versus Sample and Hold**

- Track and hold alternates between following and holding the input value.
- Sample and hold can be created by cascading two track and hold circuits.
  - Similar to digital registers which are created by cascading two latches.
Track and Hold Based on a CMOS Switch

- CMOS transistors make nice switches
  - Much better than bipolar devices since they do not have the issue of base charge storage
- Key performance issues
  - Switch resistance
  - Charge injection
  - Leakage
Accurately following the input by the end of the tracking period is important in order to achieve an accurate hold value.

- Switch resistance, $R_{ch}$, and load capacitance, $C_L$, form a lowpass filter with limited bandwidth.
  - Low $R_{ch}$ is desirable for better tracking behavior.
    - The cutoff frequency of the RC lowpass must be significantly higher than the frequency of $V_{clk}(t)$. 

**Impact of Switch Resistance**

![Circuit Diagram](image-url)
**Calculation of Switch Resistance**

- Assuming that the input and output of the switch are reasonably close in value (i.e., $V_{ds}$ is small), we can assume triode operation of the transistor

\[
R_{ch} \approx \frac{1}{\mu n C_{ox} W/L (V_{gs} - V_{TH})}
\]

- For low $R_{ch}$, we want:
  - Large $W$, Small $L$, Large $V_{gs}$
  - Issue: we need $V_{gs} > V_{TH}$
Impact of Charge Injection

- Charge injection disturbs the tracked value due to charge transfer that occurs from two key sources
  - Overlap capacitance
    - Caused by capacitive coupling of clock edge onto load capacitor, $C_L$
  - Channel charge
    - Caused by expelling the channel charge as device is abruptly turned off
Change in voltage due to overlap capacitance and charge injection (for fast fall time on $V_{clk}(t)$)

$$\Delta V \approx -\frac{C_{ov}}{C_{ov} + C_L}(V_{HI} - V_{LO}) + \frac{q_{ch}}{2} \frac{1}{C_L}$$

where

$$q_{ch} = -C_{ox} WL (V_{gs} - V_{TH})$$

$$= -C_{ox} WL (V_{HI} - V_{in} - V_{TH})$$
Signal Dependence Versus Offset for Charge Injection

- Overall charge injection impact (from previous slide)

\[
\Delta V \approx -\frac{C_{ov}}{C_{ov} + C_L}(V_{HI} - V_{LO}) - \frac{C_{ox}}{2C_L}WL(V_{HI} - V_{in} - V_{TH})
\]

Overlap Capacitance

\[
\Delta V \approx \frac{C_{ox}}{2C_L}WL V_{in} - \frac{C_{ov}}{C_{ov} + C_L}(V_{HI} - V_{LO}) - \frac{C_{ox}}{2C_L}WL(V_{HI} - V_{TH})
\]

Signal Dependent

\[
\Delta V \approx -\frac{C_{ov}}{C_{ov} + C_L}V_{in} - \frac{C_{ox}}{2C_L}WL(V_{HI} - V_{TH})
\]

Offset

- Track and Hold

\[
V_{clk}(t) \quad V_{in}(t) \quad V_{out}(t) \quad \Delta V
\]

\[
V_{HI} \quad V_{LO} \quad \frac{V_{clk}(t)}{2}
\]

\[
V_{out}(t) \quad (desired) \quad V_{out}(t) \quad (actual)
\]
Minimizing Charge Injection

- Lowering the size of the device ($WL$)
- Increasing $C_L$

Each of the above leads to an unacceptable increase in $R_{ch}C_L$
(large L is especially problematic – it should be kept at minimum)

$$\Delta V \approx \frac{C_{ox}}{2C_L}WLV_{in} - \frac{C_{ov}}{C_{ov} + C_L}(V_{HI} - V_{LO}) - \frac{C_{ox}}{2C_L}WL(V_{HI} - V_{TH})$$
Adding a Dummy Device

- Consider adding a dummy device, $M_{\text{dummy}}$, that has half the width of the switching device, $M_1$
  - Use minimum length for both devices
- In theory, both overlap cap impact and charge injection should be cancelled!
  - In practice, this does not work so well due to poor clock edge alignment, variable behavior of $M_1$ charge injection
Using Complementary Switches

- Cancels influence of overlap capacitance to some degree
- Worse for channel charge injection
  - This leads to worse signal dependent charge injection
- Reduces switch resistance (this is very useful)
  - Parallel combination of $R_{chp}$ and $R_{chn}$
    - Worst case: when $V_{in}$ is in the middle of the supply range
Bootstrapped Switches

- Bootstrapping offers several nice benefits
  - Increased gate drive (often above the supply voltage)
    - Reduces $R_{ch}$ while allowing a smaller switch size
  - Constant voltage between the input and clock during the tracking phase
    - Greatly reduces signal dependent charge injection issues
- Bootstrapping backgate is also becoming common with deep N-well processes
  - Recent example: Brunsilus et. al., ISSCC 2011
Buffered Track and Hold Circuit using Opamp

- Provides several benefits
  - Increases settling bandwidth to allow faster sampling frequency
    - Assuming parasitic cap, $C_{\text{par}}$, is less than load cap, $C_L$
    - Issue: we will see that we need a reasonable large sampling capacitor for noise reasons
  - Isolation of sensitive switch output from any perturbations from the ADC (such as kickback from its internal switches)
- Issue: adds additional offset voltage of the opamp
Use Feedback Sampling to Mitigate Opamp Offset

- Uses different placement of the sampling capacitor, $C_s$, between track and hold phases
  - We will see how this can largely eliminate the impact of opamp offset
- Such feedback sampling topologies often require multi-phase clocks
  - Key goal is to achieve non-overlapping ‘On’ times such that current flow does not occur through multiple switches at once
**First Consider Tracking Phase on Sampling Cap $C_1$**

First calculate $V_{\text{out}}$

$$V_{\text{out}} = K(V_{\text{ref}} - (V_{\text{out}} + V_{\text{off}}))$$

$$\Rightarrow V_{\text{out}} = \frac{K}{K + 1}(V_{\text{ref}} - V_{\text{off}}) \approx V_{\text{ref}} - V_{\text{off}}$$

We now calculate $V_{\text{Cs}}$ as

$$V_{\text{Cs}} = V_{\text{in}} - V_{\text{out}} = V_{\text{in}} - (V_{\text{ref}} - V_{\text{off}})$$
Now Consider Hold Phase on Sampling Cap C₁

- Calculate $V_{out}$ as

$$V_{out} = K(V_{ref} - (V_{out} - V_{Cs} + V_{off}))$$

$$\Rightarrow V_{out} = \frac{K}{K + 1}(V_{ref} + V_{Cs} - V_{off}) \approx V_{ref} + V_{Cs} - V_{off}$$

- Recall that $V_{Cs} = V_{in} - V_{ref} + V_{off}$

$$\Rightarrow V_{out} \approx V_{ref} + V_{in} - V_{ref} + V_{off} - V_{off} = V_{in}$$

Impact of opamp offset is cancelled out!
Fully Differential Version of Feedback Sampler

- Helps to cancel out the influence of charge injection
  - Appears as common-mode noise source
Influence of Thermal Noise on Sampling

- CMOS switch adds noise during the tracking phase
  - This noise is sampled as the switch is turned off at the beginning of the hold phase
- Calculation of the variance (i.e. power) of the sampled noise
  - First determine the spectral density of the noise during the tracking phase
  - Integrate the spectral density to obtain the variance of then noise
**Calculation of Noise Spectral Density (Double Sided)**

- **Spectral density at output (double sided):**

\[
S_{V_{\text{out}}}(f) = |H(f)|^2 \quad S_{v_n}(f) = |H(f)|^2 2kT R_{ch}
\]

- Where

\[
H(s) = \frac{1}{1 + sR_{ch}C_s} \quad \Rightarrow \quad H(f) = \frac{1}{1 + jf 2\pi R_{ch}C_s}
\]

- A useful fact

\[
\int_{f=\infty}^{\infty} \left| \frac{1}{1 + jf/f_o} \right|^2 df = \pi f_o
\]
Calculation of Noise Variance

- Calculation of noise variance

\[
P_{V_{out}} = \sigma_{V_{out}}^2 = \int_{-\infty}^{\infty} S_{V_{out}}(f) df = \int_{-\infty}^{\infty} \left| \frac{1}{1 + jf/f_o} \right|^2 2kT R_{ch} df
\]

- Where

\[
f_o = \frac{1}{2\pi R_{ch} C_s}
\]

\[
\Rightarrow \sigma_{V_{out}}^2 = \pi f_o 2kT R_{ch} = \pi \frac{1}{2\pi R_{ch} C_s} 2kT R_{ch} = \frac{kT}{C_s}
\]

Sampled noise variance depends only on the sample cap value!
Summary

- The CMOS sampling circuit is a key element for many systems
  - Analog to digital conversion
  - Switched capacitor filters (to be discussed in MIC513)
- Key issues for sampling circuits are
  - Accuracy (i.e., offset, noise)
    - Key insight: noise set by sample cap value
  - Speed (i.e., setting time)
  - Leakage
- Opamp feedback circuits are often combined with CMOS sampling circuits
  - Provide buffering and isolation of kickback from the circuit that follows
  - Introduce extra offset and noise
    - Clever circuit topologies can largely eliminate opamp offset