Analysis and Design of Analog Integrated Circuits
Lecture 17

Basic Two Stage CMOS Opamp

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Opamps Are Basic Analog Building Blocks

- Enable active filters
  - Can achieve arbitrary pole/zero placement using only capacitor/resistor networks around the opamp
- Allow accurate voltage to current translation
- Provide accurate charge transfer between capacitors
  - Extremely useful for switched capacitor circuits used in analog-to-digital converters and discrete-time analog filters
Key Specifications of Opamps (Open Loop)

- **DC small signal gain:** $K$
- **Unity gain frequency:** $w_0$
- **Dominant pole frequency:** $w_{dom}$
- **Parasitic pole frequencies:** $w_p$ (and higher order poles)
- **Output swing** *(max output range for DC gain > $K_{min}$)*

For Open Loop Characterization

Set $R_{huge} \gg |Z_{out}|$

and $1/(R_{huge}C_{huge}) \ll w_{dom}$
Key Specifications of Opamps (Closed Loop)

- Offset voltage
- Settling time (closed loop bandwidth)
- Input common mode range
- Equivalent Input-Referred Noise
- Common-Mode Rejection Ratio (CMRR)

\[
CMRR = \left( \frac{\delta V_{\text{offset}}}{\delta V_{\text{in}}} \right)^{-1}
\]

- Power Supply Rejection Ratio (PSRR)

\[
PSRR^+ = \left( \frac{\delta V_{\text{offset}}}{\delta V_{\text{dd}}} \right)^{-1} \\
PSRR^- = \left( \frac{\delta V_{\text{offset}}}{\delta V_{\text{ss}}} \right)^{-1}
\]
**Slew Rate Issues for Opamps**

- Output currents of practical opamps have max limits
  - Impacts maximum rate of charging or discharging load capacitance, $C_L$
  - For large step response, this leads to the output lagging behind the ideal response based on linear modeling
    - We refer to this condition as being slew-rate limited

- Where slew-rate is of concern, the output stage of the opamp can be designed to help mitigate this issue
  - Will lead to extra complexity and perhaps other issues
This is a common “workhorse” opamp for medium performance applications

Provides a nice starting point to discuss various CMOS opamp design issues

Starting assumptions: \( W_1/L_1 = W_2/L_2, W_3/L_3 = W_4/L_4 \)
First Stage Analysis

- Derive two port model assuming differential input:

\[
Z_{in1} = \frac{1}{s(C_{gs1}/2)} = \frac{1}{s(C_{gs2}/2)}
\]

\[
G_{m1} = g_{m1} = g_{m2}
\]

\[
R_{out1} = r_{o2}||r_{o4}
\]
**Derivation of** $R_{out1}$ **(Incorrect Approach)**

- Application of Thevenin analysis seems to imply that

\[ R_{out1} = 2r_{o2} || r_{o4} \]

- Why is this incorrect?
**Derivation of \( R_{out1} \) (Correct Approach)**

- **Correct approach includes the impact of the current mirror feedback**

\[
i_{test} = i_1 + i_2 = i_1 + i_1 + \frac{v_{test}}{r_04} = 2\frac{v_{test}}{2r_02} + \frac{v_{test}}{r_04}
\]

\[\Rightarrow R_{out1} = r_02 || r_04\]
Derivation of $G_{m1}$

- For differential input, we can approximate the source of $M_1$ and $M_2$ as being at incremental ground

\[
i_1 = -g_{m1}(-\frac{v_{id}}{2}) = \frac{g_{m1}}{2}v_{id}
\]

\[
i_2 = g_{m2}(\frac{v_{id}}{2}) = \frac{g_{m2}}{2}v_{id} = \frac{g_{m1}}{2}v_{id}
\]

\[
\Rightarrow i_{out} = g_{m1}v_{id} \quad \Rightarrow \quad G_{m1} = g_{m1} = g_{m2}
\]
Derivation of $Z_{in}$

- For differential input, we can simplify the input capacitance calculation through the steps shown at the right.

$$
Z_{in1} = \frac{1}{sC_{gs1}/2} = \frac{1}{sC_{gs2}/2}
$$
Second Stage Analysis

- Two port model derivation is straightforward
  - This is a common source amplifier

\[
Z_{in2} = \frac{1}{sC_{gs6}}
\]

\[
G_{m2} = g_{m6}
\]

\[
R_{out2} = r_{o6} || r_{o7}
\]
Overall Opamp Model

- **Overall transfer function**

\[
H(s) = \frac{v_{out}(s)}{v_{id}(s)} = \frac{K}{(1 + s/w_{p1})(1 + s/w_{p2})}
\]

- **DC gain**

\[
K = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})
\]

- **Poles**

\[
w_{p1} = \frac{1}{(r_{o2}||r_{o4})C_{gs6}}
\]

\[
w_{p2} = \frac{1}{(r_{o6}||r_{o7})C_{L}}
\]

- In general, \(w_{p2} << w_{p1}\) since \(C_L >> C_{gs6}\)
Consider The Dominant Pole To Be $w_{p2}$

20log($g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})$)

At frequencies $\gg w_{p2}$

$$H(s) = \frac{K}{1 + s/w_{p2}} = \frac{g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})}{1 + s(r_{o6}||r_{o7})C_L}$$

We want $w_{p1} > w_0$ for good phase margin with unity gain feedback
Key Issue for Achieving Adequate Phase Margin

- To achieve $w_{p1} > w_0$
  
  $w_{p1} = \frac{1}{(r_{o2}\|r_{o4})C_{gs6}} > w_0 \Rightarrow C_L > g_m1g_m6(r_{o2}\|r_{o4})^2C_{gs6}$

- We need a very large value of $C_L$ relative to $C_{gs6}$
  - This will generally be impractical!

\[
20\log(g_{m1}(r_{o2}\|r_{o4})g_{m6}(r_{o6}\|r_{o7}))
\]

\[
0dB
\]

\[
20\log \left| \frac{V_{out}}{V_{id}} \right|
\]

\[
w_{p2} = \frac{1}{(r_{o6}\|r_{o7})C_L}
\]

\[
w_{p1} = \frac{1}{(r_{o2}\|r_{o4})C_{gs6}}
\]

\[
w_0 \approx \frac{g_{m1}(r_{o2}\|r_{o4})g_{m6}}{C_L}
\]
Consider placing capacitor $C_c$ across the second stage.

- Load capacitance seen by stage 1 becomes roughly

$$C_M = (1 + g_{m6}(r_{o6}||r_{o7}))C_c \approx g_{m6}(r_{o6}||r_{o7})C_c$$

- This large Miller capacitance now causes $w_{p1}$ to become dramatically lower such that it forms the dominant pole

$$w_{p1} \approx \frac{1}{(r_{o2}||r_{o4})C_M} \approx \frac{1}{(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})C_c}$$

- We will see that $w_{p2}$ actually increases in frequency!
Assuming $w_{p1}$ forms the dominant pole, we can approximate $C_c$ as a short when calculating $w_{p2}$

\[
R_{th \_CL} \approx \frac{1}{g_{m6}}
\]

\[
\Rightarrow \quad w_{p2} \approx \frac{1}{\left(1/g_{m6}\right)\left(C_{gs6} + C_L\right)} = \frac{g_{m6}}{C_{gs6} + C_L}
\]

- Note: we must have $C_c \gg C_{gs6}$ for this to be accurate

The inclusion of capacitor $C_c$ has led to $w_{p2}$ increasing in frequency
**Impact of Pole Splitting using Compensation Cap**

- Pole splitting allows the dominant pole frequency to be dramatically decreased and the main parasitic pole to be dramatically increased.
  - We can achieve higher unity gain frequency with improved phase margin and with reasonable area.
Unity Gain Frequency with Compensation Cap

20\log \left( g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7}) \right)

\begin{align*}
\frac{w_{p1}}{w_{p2}} &= \frac{1}{g_{m6}(r_{o6}||r_{o7})C_c} \\
\frac{w_{p1}}{w_{p2}} &= \frac{g_{m6}}{C_{gs6}+C_L}
\end{align*}

\[ H(s) = \frac{K}{1 + s/w_{p1}} = \frac{g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})}{1 + s(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})C_c} \]

- At frequencies \( >> w_{p1} \)

\[ H(s) \approx \frac{g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})}{s(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})C_c} \quad \Rightarrow \quad w_o \approx \frac{g_{m1}}{C_c} \]

We want \( w_{p2} > w_0 \) for good phase margin with unity gain feedback.
Key Constraints for Achieving Adequate Phase Margin

- To achieve $w_{p2} > w_0$

$$w_{p2} = \frac{g_{m6}}{C_{gs6} + C_L} > w_0 \Rightarrow C_c > \frac{g_{m1}}{g_{m6}} (C_{gs6} + C_L)$$

- Note: we must have $C_c >> C_{gs6}$ for this to be accurate
More Accurate Calculations Related to Phase Margin

To achieve \( w_{p2} > w_0 \)

\[
wp2 > wo \Rightarrow C_c > \frac{gm1}{gm6} \left( \frac{C_{gs6}C_L}{C_c} + C_{gs6} + C_L \right)
\]
A More Accurate Transfer Function Model

\[ H(s) = \frac{v_{out}(s)}{v_{id}(s)} = \frac{K(1 + s/w_z)}{(1 + s/w_{p1})(1 + s/w_{p2})} \]

\[ K = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7}) \]

\[ w_{p1} = \frac{1}{(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})C_c} \]

\[ w_{p2} = \frac{g_{m6}C_c}{C_{gs6}C_L + C_c(C_{gs6} + C_L)} \]

\[ w_z = -\left( \frac{g_{m6}}{C_c} \right) \]

Right half plane (RHP) zero causes potential stability issues
Plotting the Magnitude of a RHP Zero

- Plot the magnitude response of right half plane $w_z$

$$20 \log |A_z(w)| = 20 \log \left| 1 - j\frac{w}{w_z} \right|$$

- For $w \ll |w_z|$: $20 \log |A_z(w)| \approx 20 \log |1| = 0$

- For $w \gg |w_z|$: $20 \log |A_z(w)| \approx 20 \log \left| \frac{w}{w_z} \right|$

Magnitude response is the same as for left half plane zero
Plotting the Phase of a RHP Zero

- Plot the phase response of right half plane $w_z$

$$\angle A_z(w) = \angle (1 - jw/w_z) = \arctan (-w/w_z)$$

- For $w \ll |w_z|$: $$\angle A_z(w) \approx \arctan (0) = 0^\circ$$

- For $w = |w_z|$: $$\angle A_z(w) \approx \arctan (-1) = -45^\circ$$

- For $w \gg |w_z|$: $$\angle A_z(w) \approx \arctan (-\infty) = -90^\circ$$

Phase response is negative rather than positive (similar to pole)
Phase Margin Degradation Due to RHP Zero

- Since the RHP zero adds negative phase (similar to pole), it reduces phase margin
  - We want:
    \[ |w_z| \gg w_0 \Rightarrow g_{m6} \gg g_{m1} \]
  - This is not a desirable constraint
Adding a Compensation Resistor

\[ H(s) = \frac{v_{\text{out}}(s)}{v_{\text{id}}(s)} = \frac{K(1 + s/w_z)}{(1 + s/w_{p1})(1 + s/w_{p2})} \]

\[ K = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7}) \]

\[ w_{p1} = \frac{1}{(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})C_c} \]

\[ w_{p2} = \frac{g_{m6}C_c}{C_{gs6}C_L + C_c(C_{gs6} + C_L)} \]

\[ w_z = -\left( \frac{g_{m6}}{C_c} \right) \frac{1}{1 - g_{m6}R_c} \]

- RHP zero effectively removed if \( R_c = 1/g_{m6} \)
- Improved phase margin possible with \( R_c > 1/g_{m6} \)

- See Johns&Martin, pp. 242-244
Implementing $R_c$ with a Triode Device

- More compact implementation than a poly resistor
- Triode channel resistance can somewhat track $1/g_{m6}$ across process and temperature variations
- Key issue: supply sensitivity
  - See pp. 246-248 of Johns&Martin for solutions to this issue
Calculations for Triode Compensation Resistor

- Triode resistance calculated as

\[
R_c = \frac{1}{\mu_n C_{ox} \left( \frac{W_9}{L_9} \right) \left( V_{gs9} - V_{TH} \right)}
\]

\[
= \frac{1}{\mu_n C_{ox} \left( \frac{W_9}{L_9} \right) \left( V_{dd} - V_{gs6} - V_{TH} \right)}
\]

- Assuming square law, \(1/gm_6\) is calculated as

\[
\frac{1}{g_{m6}} = \frac{1}{\mu_n C_{ox} \left( \frac{W_6}{L_6} \right) \left( V_{gs6} - V_{TH} \right)}
\]

Depending on \(V_{dd}\), \(R_c\) can track \(1/gm_6\) across process/temp
Summary

- Basic two-stage CMOS opamp is a workhorse for many moderate performance analog applications
  - Relatively simple structure with reasonable performance
- Key issue: two-stages lead to two poles that are relatively close to each other
  - This leads to very poor phase margin unless very large $C_L$ is used
- Inclusion of a compensation capacitor across the second stage leads to pole splitting such that stable performance can be achieved with reasonable area
  - A compensation resistor is also desirable to help eliminate the impact of a RHP zero that occurs due to compensation

We will use the basic two stage CMOS opamp structure to explore various opamp specifications in the next lecture